RD74VT1G245

Bus Transceiver with 3–state Output / Dual Supply Voltage Translator

REJ03D0494–0100
Rev.1.00
Jan. 13, 2005

Description

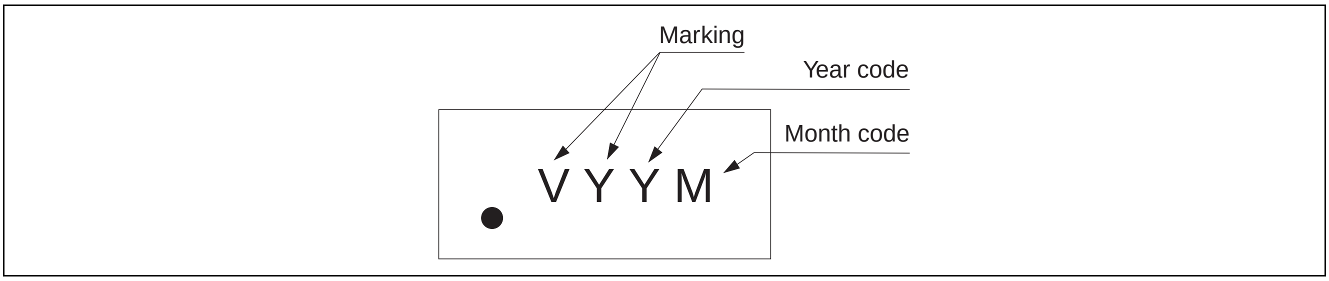
The RD74VT1G245 has one buffer in a 6 pin package. When DIR is high, data is transferred from the A inputs to the B outputs, and when DIR is low, data is transferred from the B inputs to the A outputs. And this product has two terminals (V_{CCA}, V_{CCB}), V_{CCA} is connected with control input and A bus side V_{CCB} is connected with B bus side. V_{CCA} and V_{CCB} are isolated. The A port is designed to track V_{CCA}, which accepts voltages from 1.2V to 3.6V, and the B port is designed to track V_{CCB}, which operation at 1.2V to 3.6V. Therefore, Bidirectional board voltage conversion is possible. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- This product function as level shift transceiver that change V_{CCA} input level to V_{CCB} output level, V_{CCB} input level to V_{CCA} output level by providing different supply voltage to V_{CCA} and V_{CCB}.
- Supply voltage range: V_{CCA} = 1.2 to 3.6 V
  V_{CCB} = 1.2 to 3.6 V
- Operating temperature range: –40 to +85°C
- Control input $V_{I(max)}$ = 3.6 V (@V_{CCA} = 0 to 3.6 V)
- A bus side input outputs $V_{I/O\ (max)}$ = 3.6 V (@V_{CCA} = 0 V or Output off state)
- B bus side input outputs $V_{I/O\ (max)}$ = 3.6 V (@V_{CCB} = 0 V or Output off state)
- High output current
  A bus side: ±2 mA (@V_{CCA} = 1.2 V)
  ±4 mA (@V_{CCA} = 1.5±0.1 V)
  ±6 mA (@V_{CCA} = 1.8±0.15 V)
  ±18 mA (@V_{CCA} = 2.5±0.2 V)
  ±24 mA (@V_{CCA} = 3.3±0.3 V)
  B bus side: ±2 mA (@V_{CCB} = 1.2 V)
  ±4 mA (@V_{CCB} = 1.5±0.1 V)
  ±6 mA (@V_{CCB} = 1.8±0.15 V)
  ±18 mA (@V_{CCB} = 2.5±0.2 V)
  ±24 mA (@V_{CCB} = 3.3±0.3 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
RD74VT1G245CLE	WCSP–6 pin	TBS–6AV	CL	E (3,000 pcs/reel)

Article Indication



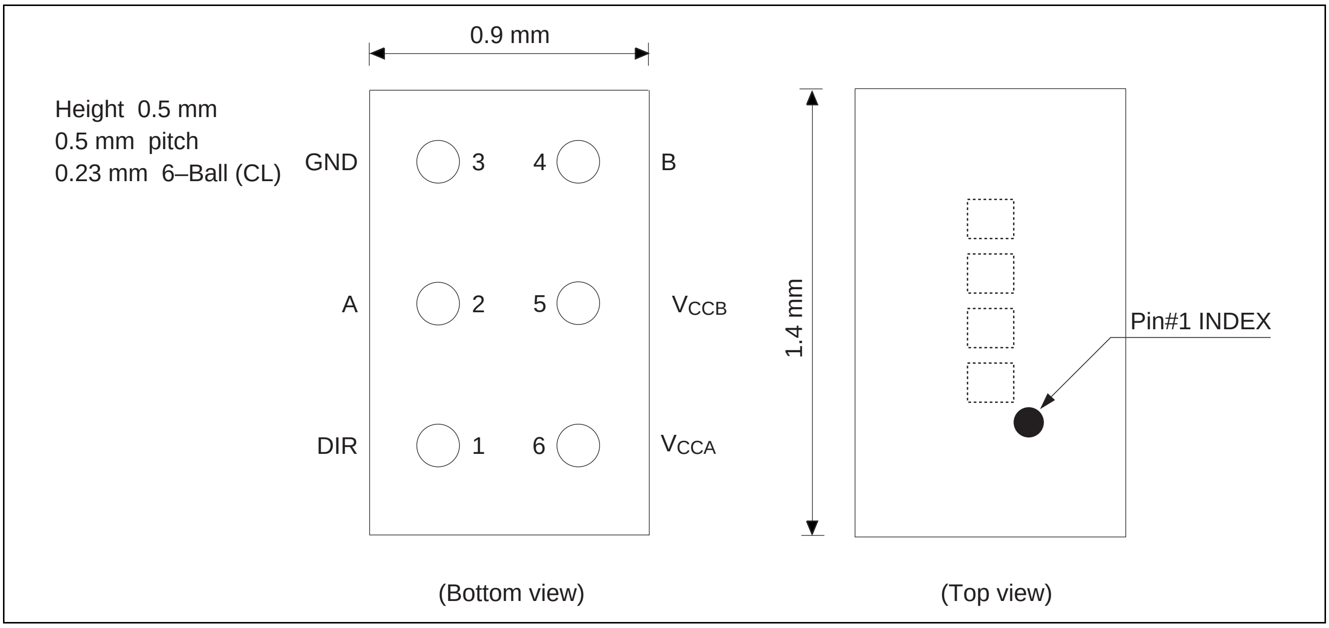
Function Table

Inputs	Operation
DIR	
L	B → A
H	A → B

H: High level

L: Low level

Pin Arrangement



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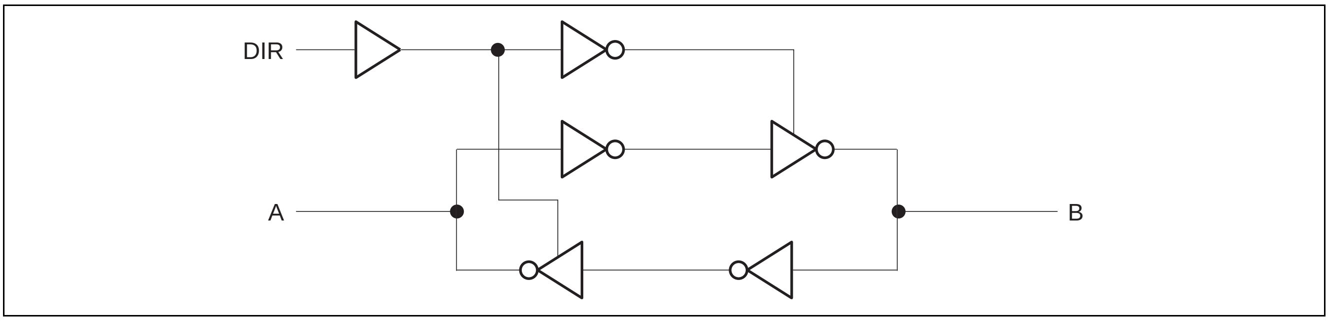
Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CCA}, V_{CCB}	–0.5 to 4.6	V	
Input voltage range [*1]	V_I	–0.5 to 4.6	V	DIR
Input/output voltage range [*1, 2]	$V_{I/O}$	–0.5 to V_{CCA}+0.5	V	A port output: “H” or “L”
		–0.5 to 4.6		A port output: “Z” or V_{CCA}: OFF
		–0.5 to V_{CCB}+0.5		B port output: “H” or “L”
		–0.5 to 4.6		B port output: “Z” or V_{CCB}: OFF
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	–50	mA	$V_O < 0$
		50		$V_O > V_{CC}+0.5$
Continuous output current	I_O	±50	mA	
Continuous output current V_{CC} or GND	I_{CCA}, I_{CCB}, I_{GND}	±100	mA	
Package Thermal impedance	θ_{ja}	123	°C/W	
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CCA}	1.2 to 3.6	V	
	V_{CCB}	1.2 to 3.6		
Input/Output voltage	V_I	0 to 3.6	V	DIR
	$V_{I/O}$	0 to 3.6	V	A port output: "H" or "L"
		0 to V_{CCA}		A port output: "Z" or V_{CCA}: OFF
		0 to 3.6		B port output: "H" or "L"
		0 to V_{CCB}		B port output: "Z" or V_{CCB}: OFF
Output current	I_{OHA}	–2	mA	V_{CCA} = 1.2 V
		–4		V_{CCA} = 1.5±0.1 V
		–6		V_{CCA} = 1.8±0.15 V
		–18		V_{CCA} = 2.5±0.2 V
		–24		V_{CCA} = 3.3±0.3 V
	I_{OHB}	–2	mA	V_{CCB} = 1.2 V
		–4		V_{CCB} = 1.5±0.1 V
		–6		V_{CCB} = 1.8±0.15 V
		–18		V_{CCB} = 2.5±0.2 V
		–24		V_{CCB} = 3.3±0.3 V
	I_{OLA}	2	mA	V_{CCA} = 1.2 V
		4		V_{CCA} = 1.5±0.1 V
		6		V_{CCA} = 1.8±0.15 V
		18		V_{CCA} = 2.5±0.2 V
		24		V_{CCA} = 3.3±0.3 V
	I_{OLB}	2	mA	V_{CCB} = 1.2 V
		4		V_{CCB} = 1.5±0.1 V
		6		V_{CCB} = 1.8±0.15 V
		18		V_{CCB} = 2.5±0.2 V
		24		V_{CCB} = 3.3±0.3 V
Input transition rise or fall time	$\Delta t / \Delta v$	10	ns / V	
Operation free-air temperature	Ta	–40 to 85	°C	

Electrical Characteristics

(Ta = –40 to 85°C)

Item	Symbol	V_{CCA} (V) *	V_{CCB} (V) *	Min	Typ	Max	Unit	Test conditions
Input voltage	V_{IHA}	1.2	1.2 to 3.6	V_{CCA}×0.75	—	—	V	A port Control input
		1.5±0.1		V_{CCA}×0.70	—	—		
		1.8±0.15		V_{CCA}×0.65	—	—		
		2.5±0.2		1.6	—	—		
		3.3±0.3		2.0	—	—		
	V_{IHB}	1.2 to 3.6	1.2	V_{CCB}×0.75	—	—	V	B port
			1.5±0.1	V_{CCB}×0.70	—	—		
			1.8±0.15	V_{CCB}×0.65	—	—		
			2.5±0.2	1.6	—	—		
			3.3±0.3	2.0	—	—		
	V_{ILA}	1.2	1.2 to 3.6	—	—	V_{CCA}×0.25	V	A port Control input
		1.5±0.1		—	—	V_{CCA}×0.30		
		1.8±0.15		—	—	V_{CCA}×0.35		
		2.5±0.2		—	—	0.7		
		3.3±0.3		—	—	0.8		
	V_{ILB}	1.2 to 3.6	1.2	—	—	V_{CCB}×0.25	V	B port
			1.5±0.1	—	—	V_{CCB}×0.30		
			1.8±0.15	—	—	V_{CCB}×0.35		
			2.5±0.2	—	—	0.7		
			3.3±0.3	—	—	0.8		
Output voltage	V_{OH}	1.2 to 3.6	1.2 to 3.6	V_{CC}–0.2	—	—	V	I_{OH} = –100 μA
		1.2	1.2	0.9	—	—		I_{OH} = –2 mA
		1.5±0.1	1.5±0.1	1.1	—	—		I_{OH} = –4 mA
		1.8±0.15	1.8±0.15	1.25	—	—		I_{OH} = –6 mA
		2.5±0.2	2.5±0.2	1.7	—	—		I_{OH} = –18 mA
		3.3±0.3	3.3±0.3	2.2	—	—		I_{OH} = –24 mA
	V_{OL}	1.2 to 3.6	1.2 to 3.6	—	—	0.2	V	I_{OL} = 100 μA
		1.2	1.2	—	—	0.3		I_{OL} = 2 mA
		1.5±0.1	1.5±0.1	—	—	0.3		I_{OL} = 4 mA
		1.8±0.15	1.8±0.15	—	—	0.3		I_{OL} = 6 mA
		2.5±0.2	2.5±0.2	—	—	0.6		I_{OL} = 18 mA
		3.3±0.3	3.3±0.3	—	—	0.55		I_{OL} = 24 mA
Input current	I_{IN}	3.6	3.6	–1.5	—	1.5	μA	V_{IN} = GND or V_{CCA} control input
Off state output current	I_{OZ}	3.6	3.6	–1.5	—	1.5	μA	V_{IN} = V_{IH} or V_{IL}
Output leakage current	I_{OFF}	0	0	—	—	1.5	μA	V_{IN}, V_{OUT} = 0 to 3.6 V
Quiescent supply current	I_{CCA}	1.2 to 3.6	1.2 to 3.6	–3.0	—	3.0	μA	$I_{O(A\ port)}$ = 0 V_{IN} = V_{CCB} or GND
	I_{CCB}	1.2 to 3.6	1.2 to 3.6	–3.0	—	3.0		$I_{O(B\ port)}$ = 0 V_{IN} = V_{CCA} or GND
Increase in ICC per input	ΔI_{CCA}	3.6	3.6	—	—	250	μA	A port or control V_{CCA}–0.6 (1 input)
	ΔI_{CCB}	3.6	3.6	—	—	250		B port V_{CCB}–0.6 (1 input)
Input capacitance	C_{IN}	3.3	3.3	—	3.5	—	pF	V_{IN} = V_{CC} or GND
Input/output capacitance	$C_{I/O}$	3.3	3.3	—	6.0	—	pF	V_O = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

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Switching Characteristics

V_{CCA} = 3.3±0.3 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C									Unit	Test conditions
				V_{CCB}= 1.2 V	V_{CCB}= 1.5±0.1 V		V_{CCB}= 1.8±0.15 V		V_{CCB}= 2.5±0.2 V		V_{CCB}= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max		
Propagation delay time	t_{PLH}	A	B	9.1	2.0	8.8	1.5	5.8	1.0	4.0	1.0	3.2	ns	C_L = 15pF R_L = 2.0kΩ
	t_{PHL}			9.1	2.0	8.8	1.5	5.8	1.0	4.0	1.0	3.2		
	t_{PLH}	B	A	4.0	1.0	4.2	1.0	3.8	1.0	3.4	1.0	3.2		
	t_{PHL}			4.0	1.0	4.2	1.0	3.8	1.0	3.4	1.0	3.2		
Output Disable time	t_{HZ}	DIR	A	4.0	1.0	4.5	1.0	4.5	1.0	4.5	1.0	4.5	ns	C_L = 15pF R_L = 2.0kΩ
	t_{LZ}			4.0	1.0	4.5	1.0	4.5	1.0	4.5	1.0	4.5		
	t_{HZ}	DIR	B	11.2	2.0	10.2	1.5	8.0	1.0	6.0	1.0	5.5		
	t_{LZ}			11.2	2.0	10.2	1.5	8.0	1.0	6.0	1.0	5.5		
Output Enable time	t_{ZH} [*1]	DIR	A	15.2	—	14.4	—	11.8	—	9.4	—	8.7	ns	C_L = 15pF R_L = 2.0kΩ
	t_{ZL} [*1]			15.2	—	14.4	—	11.8	—	9.4	—	8.7		
	t_{ZH} [*1]	DIR	B	13.1	—	13.3	—	10.3	—	8.5	—	7.7		
	t_{ZL} [*1]			13.1	—	13.3	—	10.3	—	8.5	—	7.7		

Note: 1. The enable time is a calculated value, derived using the formula shown in the section entitled enable times on page 12.

V_{CCA} = 2.5±0.2 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C									Unit	Test conditions
				V_{CCB}= 1.2 V	V_{CCB}= 1.5±0.1 V		V_{CCB}= 1.8±0.15 V		V_{CCB}= 2.5±0.2 V		V_{CCB}= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max		
Propagation delay time	t_{PLH}	A	B	9.5	2.0	9.2	1.5	6.0	1.0	4.2	1.0	3.4	ns	C_L = 15pF R_L = 2.0kΩ
	t_{PHL}			9.5	2.0	9.2	1.5	6.0	1.0	4.2	1.0	3.4		
	t_{PLH}	B	A	4.7	1.0	4.8	1.0	4.6	1.0	4.2	1.0	4.0		
	t_{PHL}			4.7	1.0	4.8	1.0	4.6	1.0	4.2	1.0	4.0		
Output Disable time	t_{HZ}	DIR	A	4.2	1.0	4.7	1.0	4.7	1.0	4.7	1.0	4.7	ns	C_L = 15pF R_L = 2.0kΩ
	t_{LZ}			4.2	1.0	4.7	1.0	4.7	1.0	4.7	1.0	4.7		
	t_{HZ}	DIR	B	11.2	2.0	10.6	1.5	8.4	1.0	6.0	1.0	6.0		
	t_{LZ}			11.2	2.0	10.6	1.5	8.4	1.0	6.0	1.0	6.0		
Output Enable time	t_{ZH} [*1]	DIR	A	15.9	—	15.4	—	13.0	—	10.2	—	10.0	ns	C_L = 15pF R_L = 2.0kΩ
	t_{ZL} [*1]			15.9	—	15.4	—	13.0	—	10.2	—	10.0		
	t_{ZH} [*1]	DIR	B	13.7	—	13.9	—	10.7	—	8.9	—	8.1		
	t_{ZL} [*1]			13.7	—	13.9	—	10.7	—	8.9	—	8.1		

Note: 1. The enable time is a calculated value, derived using the formula shown in the section entitled enable times on page 12.

Switching Characteristics (Cont.)

V_{CCA} = 1.8±0.15 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C									Unit	Test conditions
				V_{CCB}= 1.2 V	V_{CCB}= 1.5±0.1 V		V_{CCB}= 1.8±0.15 V		V_{CCB}= 2.5±0.2 V		V_{CCB}= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max		
Propagation delay time	t_{PLH}	A	B	9.8	2.0	9.6	1.5	6.5	1.0	4.6	1.0	3.8	ns	C_L = 15pF R_L = 2.0kΩ
	t_{PHL}			9.8	2.0	9.6	1.5	6.5	1.0	4.6	1.0	3.8		
	t_{PLH}	B	A	6.4	1.5	7.2	1.5	6.5	1.5	6.0	1.5	5.8		
	t_{PHL}			6.4	1.5	7.2	1.5	6.5	1.5	6.0	1.5	5.8		
Output Disable time	t_{HZ}	DIR	A	5.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5	ns	C_L = 15pF R_L = 2.0kΩ
	t_{LZ}			5.5	1.5	7.5	1.5	7.5	1.5	7.5	1.5	7.5		
	t_{HZ}	DIR	B	12.0	2.0	11.5	1.5	9.2	1.0	7.2	1.0	7.0		
	t_{LZ}			12.0	2.0	11.5	1.5	9.2	1.0	7.2	1.0	7.0		
Output Enable time	t_{ZH} *1	DIR	A	18.4	—	18.7	—	15.7	—	13.2	—	12.8	ns	C_L = 15pF R_L = 2.0kΩ
	t_{ZL} *1			18.4	—	18.7	—	15.7	—	13.2	—	12.8		
	t_{ZH} *1	DIR	B	15.3	—	17.1	—	14.0	—	12.1	—	11.3		
	t_{ZL} *1			15.3	—	17.1	—	14.0	—	12.1	—	11.3		

Note: 1. The enable time is a calculated value, derived using the formula shown in the section entitled enable times on page 12.

V_{CCA} = 1.5±0.1 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C									Unit	Test conditions
				V_{CCB}= 1.2 V	V_{CCB}= 1.5±0.1 V		V_{CCB}= 1.8±0.15 V		V_{CCB}= 2.5±0.2 V		V_{CCB}= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max		
Propagation delay time	t_{PLH}	A	B	10.0	2.0	10.5	1.5	7.2	1.0	4.8	1.0	4.2	ns	C_L = 15pF R_L = 2.0kΩ
	t_{PHL}			10.0	2.0	10.5	1.5	7.2	1.0	4.8	1.0	4.2		
	t_{PLH}	B	A	8.0	2.0	10.5	2.0	9.6	2.0	9.2	2.0	8.8		
	t_{PHL}			8.0	2.0	10.5	2.0	9.6	2.0	9.2	2.0	8.8		
Output Disable time	t_{HZ}	DIR	A	6.0	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns	C_L = 15pF R_L = 2.0kΩ
	t_{LZ}			6.0	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0		
	t_{HZ}	DIR	B	12.5	2.0	12.7	1.5	12.0	1.0	10.7	1.0	7.5		
	t_{LZ}			12.5	2.0	12.7	1.5	12.0	1.0	10.7	1.0	7.5		
Output Enable time	t_{ZH} *1	DIR	A	20.5	—	23.2	—	21.6	—	19.9	—	16.3	ns	C_L = 15pF R_L = 2.0kΩ
	t_{ZL} *1			20.5	—	23.2	—	21.6	—	19.9	—	16.3		
	t_{ZH} *1	DIR	B	16.0	—	20.5	—	17.2	—	14.8	—	14.2		
	t_{ZL} *1			16.0	—	20.5	—	17.2	—	14.8	—	14.2		

Note: 1. The enable time is a calculated value, derived using the formula shown in the section entitled enable times on page 12.

Switching Characteristics (Cont.)

V_{CCA} = 1.2 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C					Unit	Test conditions
				V_{CCB}= 1.2 V	V_{CCB}= 1.5±0.1 V	V_{CCB}= 1.8±0.15 V	V_{CCB}= 2.5±0.2 V	V_{CCB}= 3.3±0.3 V		
				Typ	Typ	Typ	Typ	Typ		
Propagation delay time	t_{PLH}	A	B	10.5	8.0	6.4	4.7	4.0	ns	C_L = 15pF R_L = 2.0kΩ
	t_{PHL}			10.5	8.0	6.4	4.7	4.0		
	t_{PLH}	B	A	10.5	10.0	9.8	9.5	9.1		
	t_{PHL}			10.5	10.0	9.8	9.5	9.1		
Output Disable time	t_{HZ}	DIR	A	8.0	8.0	8.0	8.0	8.0	ns	C_L = 15pF R_L = 2.0kΩ
	t_{LZ}			8.0	8.0	8.0	8.0	8.0		
	t_{HZ}	DIR	B	13.5	10.5	9.5	7.5	7.5		
	t_{LZ}			13.5	10.5	9.5	7.5	7.5		
Output Enable time	t_{ZH} *1	DIR	A	24.0	20.5	19.3	17.0	16.6	ns	C_L = 15pF R_L = 2.0kΩ
	t_{ZL} *1			24.0	20.5	19.3	17.0	16.6		
	t_{ZH} *1	DIR	B	18.5	16.0	14.4	12.7	12.0		
	t_{ZL} *1			18.5	16.0	14.4	12.7	12.0		

Note: 1. The enable time is a calculated value, derived using the formula shown in the section entitled enable times on page 12.

Operating Characteristics

Ta = 25°C

Item	Symbol	V_{CCA} (V)	V_{CCB} (V)	Min	Typ	Max	Unit	Test conditions
Power dissipation capacitance	C_{PD}	3.3	3.3	—	12	—	pF	f = 10 MHz C_L = 0

Power–up considerations

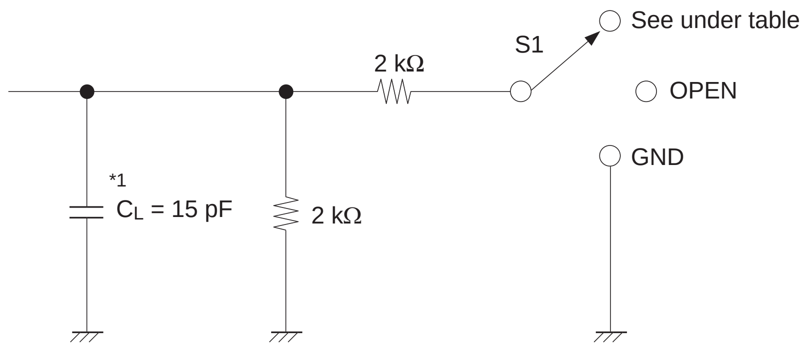
Level–translation devices offer an opportunity for successful mixed–voltage signal design.

A proper power–up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins.

Take these precautions to guard against such power–up problems.

1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device. (Power up of V_{CCA} is first. Next power up is V_{CCB})
3. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, DIR low is needed (B data to A bus), ramp it with GND.

Test Circuit

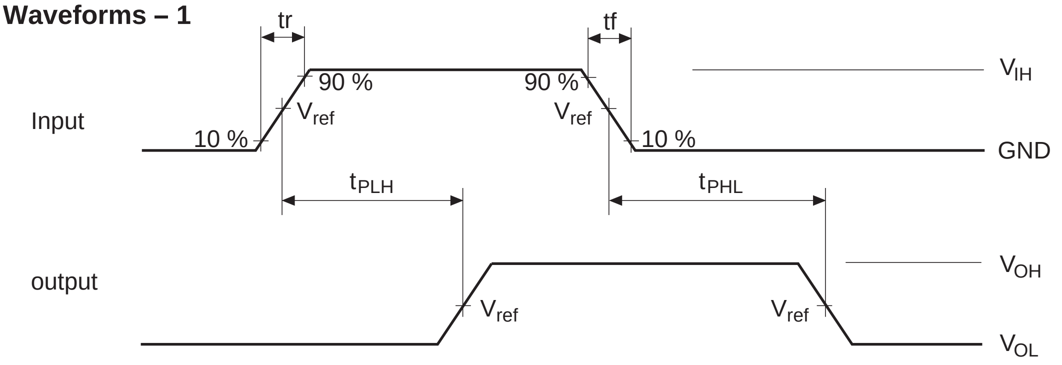


Load circuit for outputs

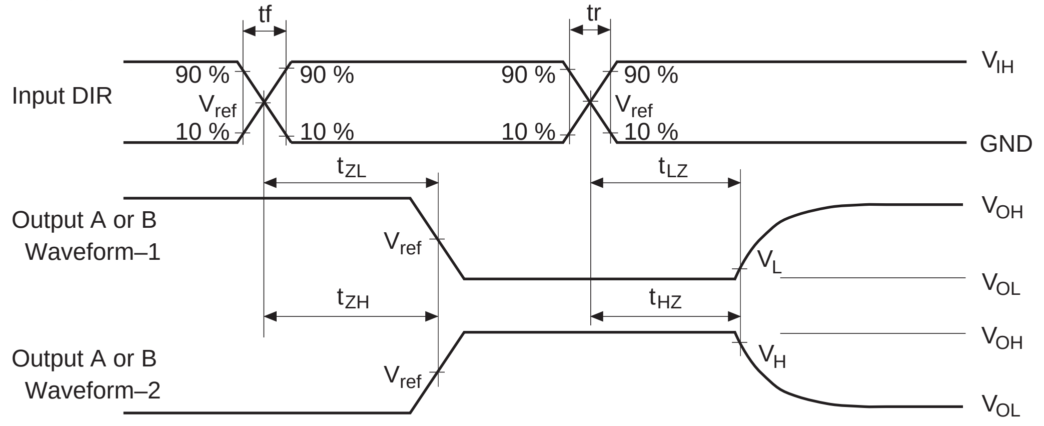
Symbol	S1
t_{PLH} / t_{PHL}	OPEN
t_{ZH} / t_{HZ}	GND
t_{ZL} / t_{LZ}	$2 \times V_{CC}$

Note: 1. C_L includes probe and jig capacitance.

• Waveforms – 1



• Waveforms – 2



Symbol	V_{CC} = 1.2 V, 1.5±0.1 V	V_{CC} = 1.8±0.15 V	V_{CC} = 2.5±0.2 V	V_{CC} = 3.3±0.3 V
t_r / t_f	2.0 ns	2.0 ns	2.0 ns	2.0 ns
V_{IH}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{ref}	1/2 V_{CC}	1/2 V_{CC}	1/2 V_{CC}	1/2 V_{CC}
V_H / V_L	$V_H = V_{OH}$-0.1 V $V_L = V_{OL}$+0.1 V	$V_H = V_{OH}$-0.15 V $V_L = V_{OL}$+0.15 V	$V_H = V_{OH}$-0.15 V $V_L = V_{OL}$+0.15 V	$V_H = V_{OH}$-0.3 V $V_L = V_{OL}$+0.3 V

Notes:
1. Input waveform : PRR ≤ 10 MHz, Zo = 50 Ω, duty cycle 50%.
2. Waveform – 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform – 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

Application Information

Figure 1 is an example circuit of the RD74VT1G245 being used in a bidirectional logic level–shifting application.

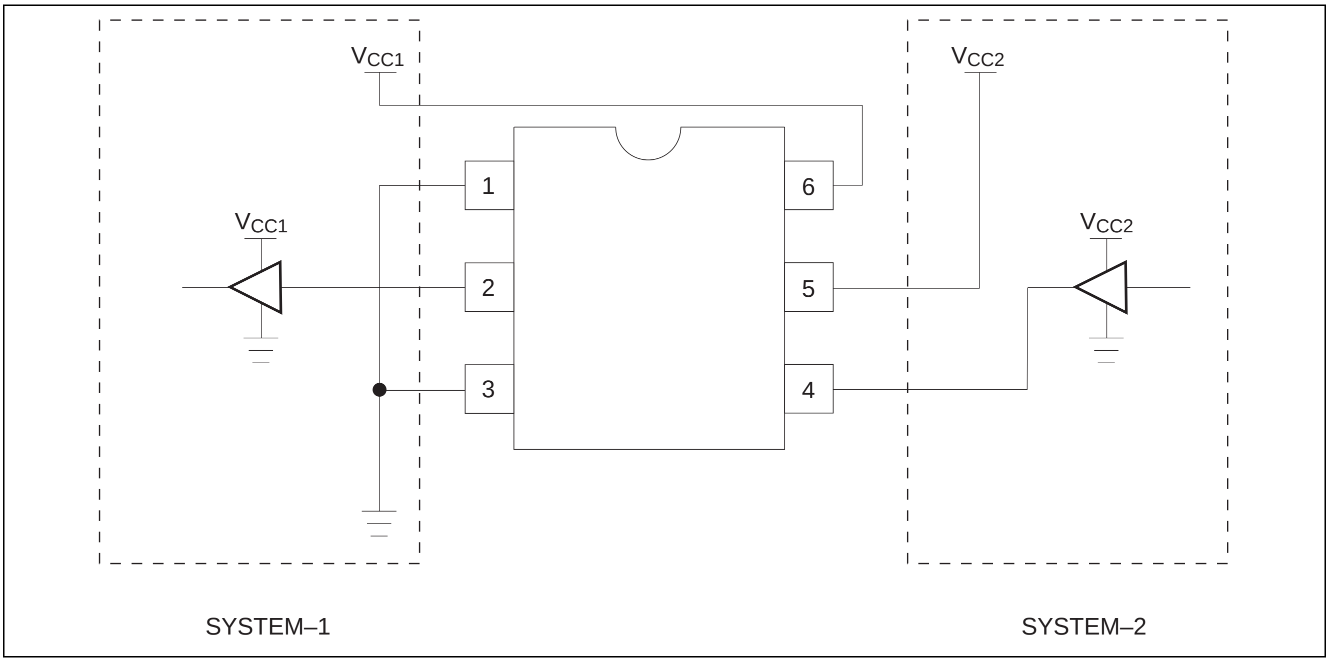


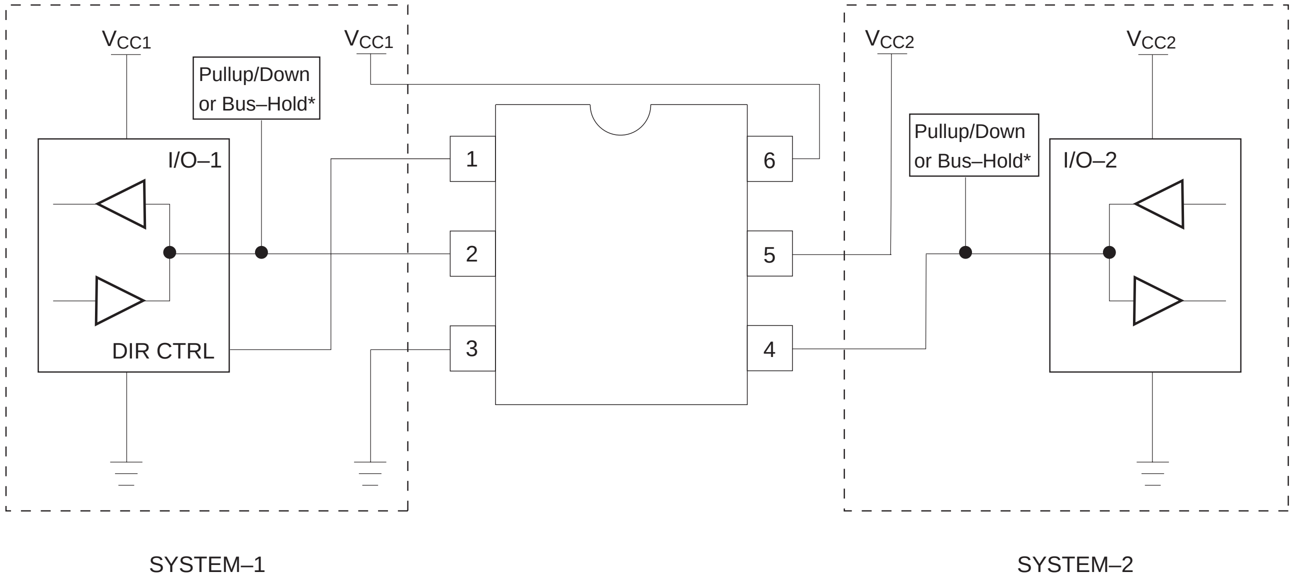
Figure 1. Bidirectional Logic Level–Shifting Application

Pin Description

PIN	NAME	FUNCTION	DESCRIPTION
1	DIR	DIR	The GND (low–level) determines B–port to A–port direction
2	A	OUT	Output level depends on V_{CC1} voltage
3	GND	GND	Device GND
4	B	IN	Input threshold value depends on V_{CC2} voltage
5	V_{CCB}	V_{CC2}	SYSTEM–2 supply voltage (1.2V to 3.6V)
6	V_{CCA}	V_{CC1}	SYSTEM–1 supply voltage (1.2V to 3.6V)

Application Information (Cont.)

Figure 2 shows the RD74VT1G245 used in a bidirectional logic level–shifting application. Since the RD74VT1G245 does not have an output enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM–1 and SYSTEM–2 when changing directions.



Notes: Following is a sequence that illustrates data transmission from SYSTEM–1 to SYSTEM–2 and then from SYSTEM–2 to SYSTEM–1.

STATE	DIR CTRL	I/O–1	I/O–2	DESCRIPTION
1	H	IN	OUT	SYSTEM–1 data to SYSTEM–2
2	H	HI–Z	HI–Z	SYSTEM–2 is getting ready to send data to SYSTEM–1. I/O–1 and I/O–2 are disabled. The bus–line state depends on Pull–up or Down.*
3	L	HI–Z	HI–Z	DIR bit is flipped. I/O–1 and I/O–2 are atill disabled. The bus–line state depends on Pull–up or Down.*
4	L	OUT	IN	SYSTEM–2 data to SYSTEM–1

*: SYSTEM–1 and SYSTEM–2 must use same conditions, i.e., both pull–up or both pull–down.

Figure 2. Bidirectional Logic Level-Shifting Application

Calculate the enable times for the RD74VT1G245 using the following formulas:

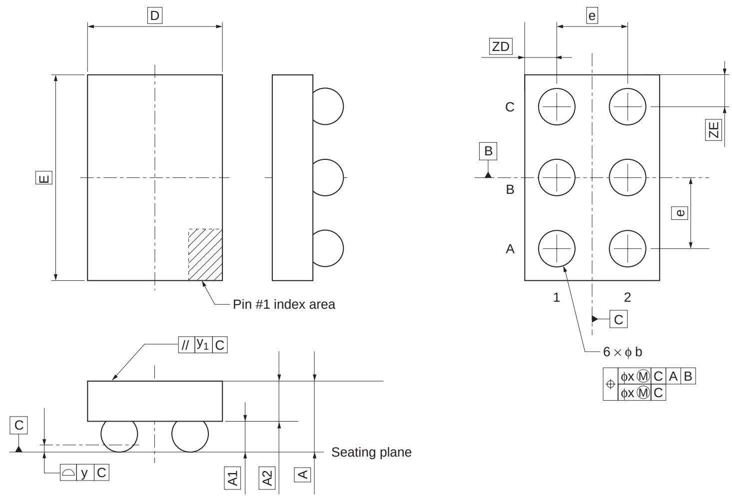
1. t_{ZH} (DIR to A) = t_{LZ} (DIR to B) + t_{PLH} (B to A)
2. t_{ZL} (DIR to A) = t_{HZ} (DIR to B) + t_{PHL} (B to A)
3. t_{ZH} (DIR to B) = t_{LZ} (DIR to A) + t_{PLH} (A to B)
4. t_{ZL} (DIR to B) = t_{HZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the RD74VT1G245 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

Package Dimensions

TBS-6AV

EIAJ Package Code	JEDEC Code	Mass (g)	Lead Material
—	—	0.001	—



*Reference value.

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	———	———	0.50
A_1	0.155	———	0.185
A_2	———	———	(0.315)*
b	0.20	———	0.25
D	———	0.90	———
E	———	1.40	———
e	———	0.50	———
x	———	———	0.05
y	———	———	0.05
y_1	———	———	0.20
ZD	———	0.20	———
ZE	———	0.20	———

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