

Features

- Precision supply-voltage monitor
 - 4.63V (PT7A7511, 7521, 7531)
 - 4.38V (PT7A7512, 7522, 7532)
 - 3.08V (PT7A7513, 7523, 7533)
 - 2.93V (PT7A7514, 7524, 7534)
 - 2.63V (PT7A7515, 7525, 7535)
 - 2.32V (PT7A7516, 7526, 7536)
 - 2.20V (PT7A7517, 7527, 7537)
- 200ms reset pulse width
- Debounced TTL/CMOS-compatible manual-reset input
- Independent watchdog timer 1.6sec time-out (not available for PT7A7531 - 7537)
- Reset output signal:
 - Active-low only (PT7A7511 - 7517)
 - Active-high only (PT7A7521 - 7527)
 - Active-high and active-low (PT7A7531 - 7537)
- Voltage monitor for power-fail or low battery warning
- Guaranteed $\overline{\text{RESET}}/\text{RESET}$ valid at $V_{\text{CC}} = 1.2\text{V}$

Introduction

The PT7A751X/752X/753X family microprocessor (μP) supervisory circuits are targeted to improve reliability and accuracy of power-supply circuitry in μP systems. These devices reduce the complexity and number of components required to monitor power-supply and battery functions.

The main functions are:

1. Asserting reset output during power-μp, power-down and brownout conditions for μP system;
2. Detecting power failure or low-battery conditions with a 1.25V threshold detector;
3. Watchdog functions (not for PT7A753x).

Applications

- Power-supply circuitry in μP systems

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Block Diagram

Figure 1. Block Diagram of PT7A7511-7517/7521-7527

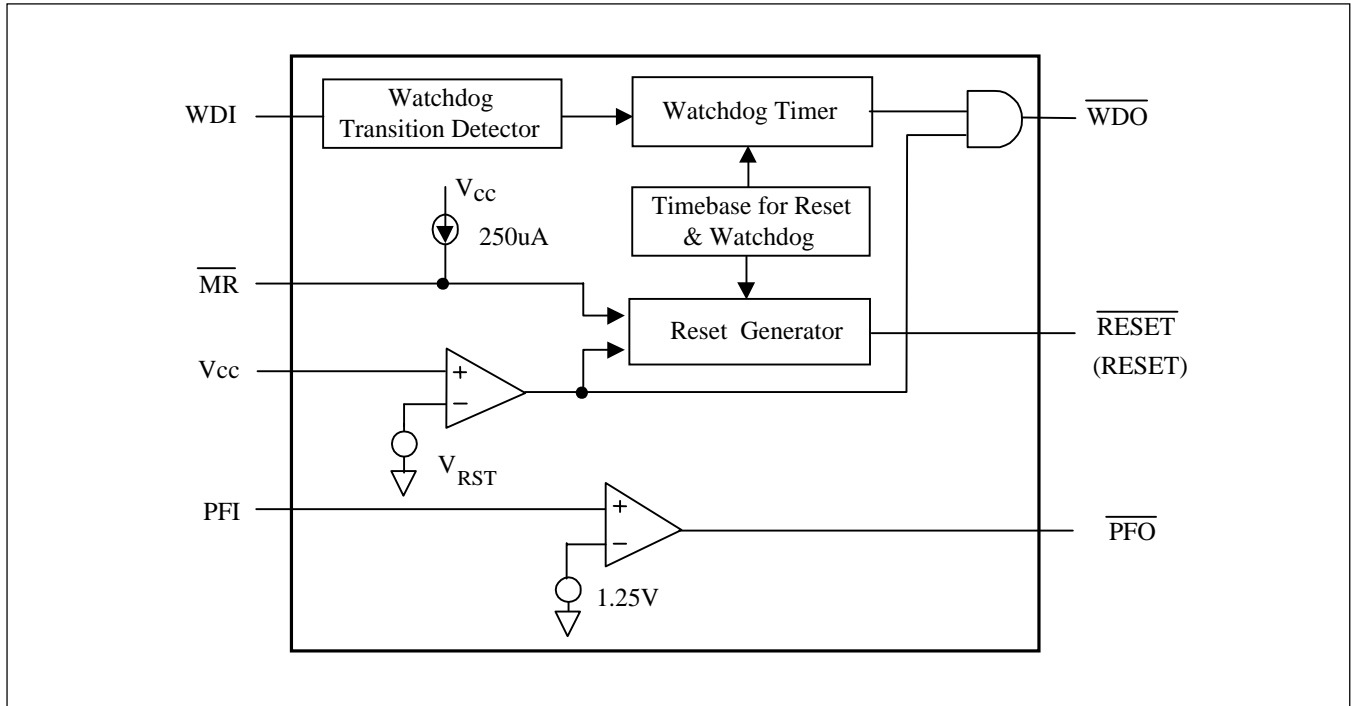
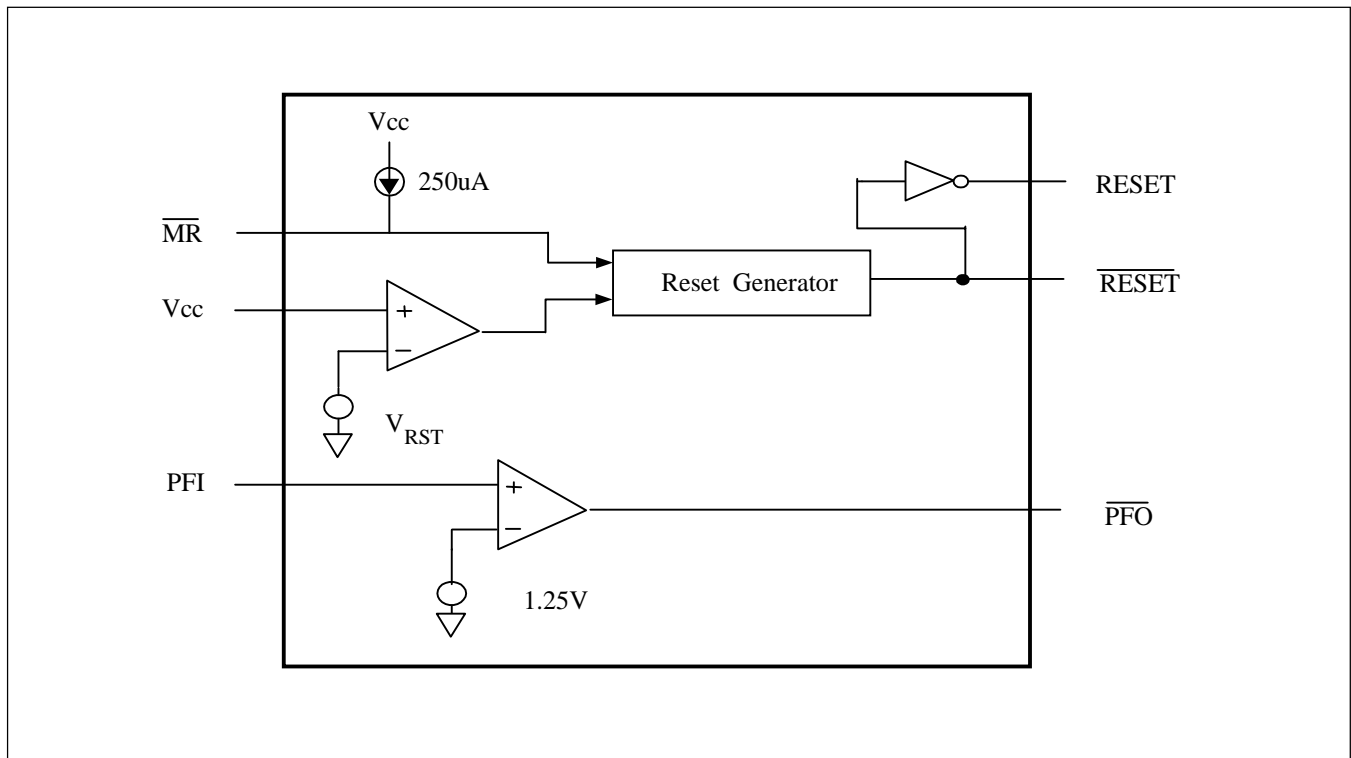


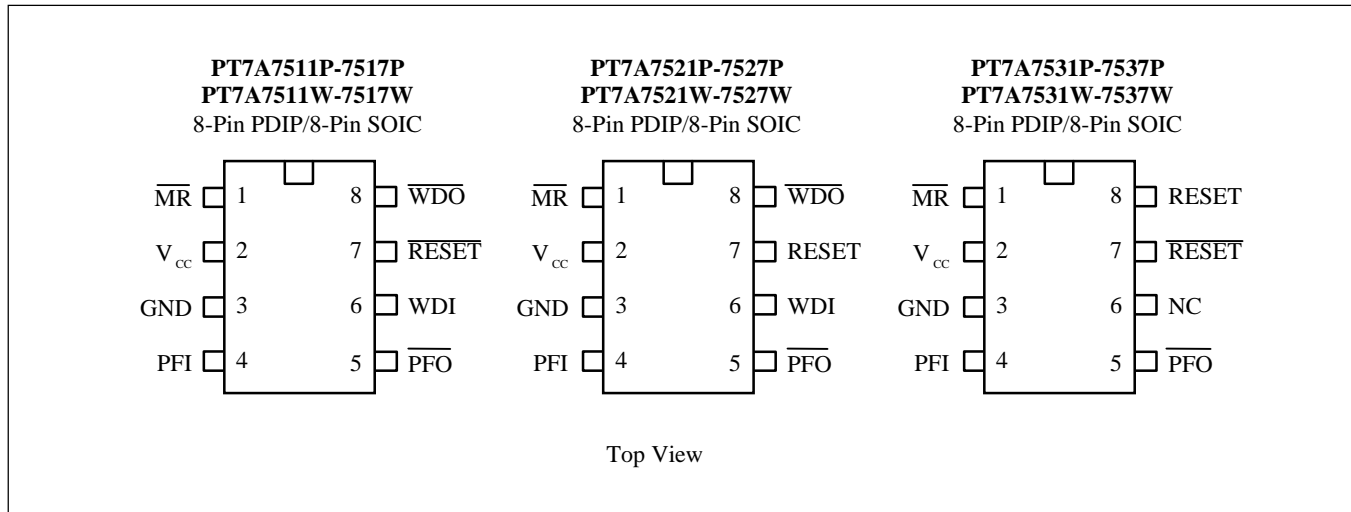
Figure 2. Block Diagram of PT7A7531-7537



Pin Information

Pin Configuration

Figure 3. Pin Configuration



Pin Description

Table 1. Pin Description

Pin Name	Type	Description
$\overline{\text{MR}}$	I	Manual-Reset: triggers a reset pulse when pulled below 0.8V, active low. It has an internal 250μA pull-up current and be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
V _{cc}	Power	Power Supply
GND	Ground	Ground Reference for all signals
PFI	I	Power-Fail Voltage Monitor Input: When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND or V _{cc} when not used.
$\overline{\text{PFO}}$	O	Power-Fail Output: it gets low and sinks current when PFI is less than 1.25V; otherwise $\overline{\text{PFO}}$ stays high.
WDI	I	Watchdog Input: If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and $\overline{\text{WDO}}$ goes low. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted. WDI is three-stated, or WDI sees a rising or falling edge.
NC		No Connect
$\overline{\text{RESET}}$	O	Reset Output pulses: low for 200ms when triggered, and stays low whenever V _{cc} is below the reset threshold. It remains low for 200ms after V _{cc} rises above the reset threshold or $\overline{\text{MR}}$ goes from low to high. A watchdog timeout will not trigger $\overline{\text{RESET}}$ unless $\overline{\text{WDO}}$ is connected to $\overline{\text{MR}}$.
$\overline{\text{WDO}}$	O	Watchdog Output: pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{\text{WDO}}$ also goes low during low-line conditions. Whenever V _{cc} is below the reset threshold, $\overline{\text{WDO}}$ stays low; however, unlike $\overline{\text{RESET}}$, $\overline{\text{WDO}}$ does not have minimum pulse width. As soon as V _{cc} rises above the reset threshold, $\overline{\text{WDO}}$ goes high with no delay.
RESET	O	The inverse of $\overline{\text{RESET}}$: active high. Whenever $\overline{\text{RESET}}$ is high, RESET is low.

Functional Description

The PT75xx family can assert reset output during power-up, power-down and brownout conditions for uP system, detect power failure or low-battery conditions with a 1.25V threshold detector and have watchdog functions. Refer to Table 2 for their individual features. The typical application see Figure 4.

Reset Output

The supervisory circuits can assert reset for a microprocessor during power-up, power-down and brownout to prevent code execution errors.

On power-up, once V_{CC} reaches about 1.2V, \overline{RESET} is a guaranteed logic low of 0.4V or less. As V_{CC} rises, \overline{RESET} stays low. When V_{CC} rises above the reset threshold, an internal timer releases \overline{RESET} after about 200ms. \overline{RESET} pulses low whenever V_{CC} drops below the reset threshold (brownout condition). If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms.

On power-down, once V_{CC} falls below the reset threshold, \overline{RESET} stays low and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The PT7A752x and PT7A753x active-high RESET output is simply the complement of the \overline{RESET} output, and is guaranteed to be valid with V_{CC} down to 1.2V. Some μPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The watchdog circuit monitors the μP's activity. If the μP does not toggle the watchdog input (WDI) within 1.6sec and WDI is not in high impedance, \overline{WDO} goes low. As long as \overline{RESET} is asserted or the WDI input is in high impedance, the watchdog timer will stay cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, \overline{WDO} will be connected to the non-maskable interrupt input (NMI) of a μP. When V_{CC} drops below the reset threshold, \overline{WDO} will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but \overline{RESET} goes low simultaneously, and thus overrides the NMI interrupt. If WDI is left unconnected, \overline{WDO} can be used as a low-line output. Since floating WDI disables the internal timer, \overline{WDO} goes low only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

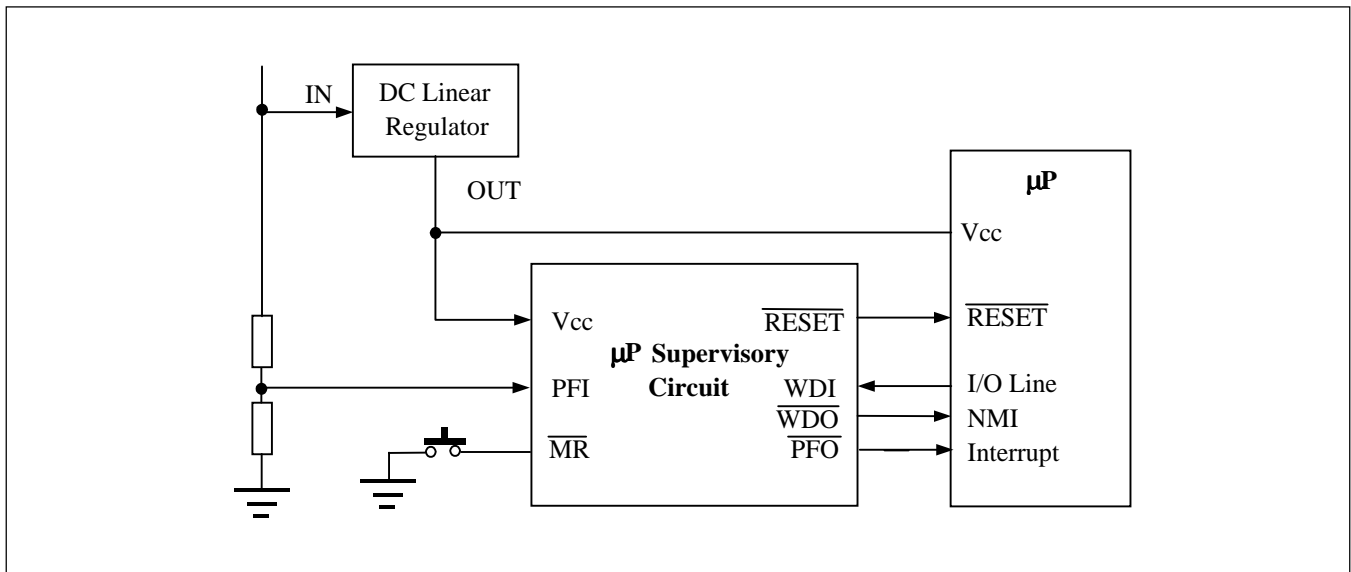
Manual Reset

The manual-reset input (\overline{MR}) allows reset to be triggered by a push-button switch. The switch is effectively debounced by the 140ms minimum reset pulse width. \overline{MR} is TTL/CMOS logic compatible, so it can be driven by any logic reset output.

Power-Fail Comparator

The power-fail comparator will send out a Low signal once detects a voltage lowered than 1.25V. It can be used for various purposes because its output and non-inverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

Figure 4. Typical Application Circuit



Function Reference Table

Table 2. Function Table of PT7A75xx Family

Part No.	Reset Threshold	Reset Active Low or High	Nom. Reset Time (ms), t_{RS}	Nom. Watch dog Time (sec), t_{WD}	Power Fail Comp.	Manual Reset Input
PT7A7511	4.63V	LOW	200	1.6	1.25V detector	Yes
PT7A7521	4.63V	HIGH	200	1.6	1.25V detector	Yes
PT7A7531	4.63V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7512	4.38V	LOW	200	1.6	1.25V detector	Yes
PT7A7522	4.38V	HIGH	200	1.6	1.25V detector	Yes
PT7A7532	4.38V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7513	3.08V	LOW	200	1.6	1.25V detector	Yes
PT7A7523	3.08V	HIGH	200	1.6	1.25V detector	Yes
PT7A7533	3.08V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7514	2.93V	LOW	200	1.6	1.25V detector	Yes
PT7A7524	2.93V	HIGH	200	1.6	1.25V detector	Yes
PT7A7534	2.93V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7515	2.63V	LOW	200	1.6	1.25V detector	Yes
PT7A7525	2.63V	HIGH	200	1.6	1.25V detector	Yes
PT7A7535	2.63V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A3516	2.32V	LOW	200	1.6	1.25V detector	Yes
PT7A3526	2.32V	HIGH	200	1.6	1.25V detector	Yes
PT7A3536	2.32V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7517	2.20V	LOW	200	1.6	1.25V detector	Yes
PT7A7527	2.20V	HIGH	200	1.6	1.25V detector	Yes
PT7A7537	2.20V	LOW, HIGH	200	unavailable	1.25V detector	Yes

Detailed Specifications

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C	Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
Ambient Temperature with Power Applied	-40°C to +85°C	
Supply Voltage to Ground Potential (V _{CC} to GND)	-0.3V to +7.0V	
DC Input Voltage (All inputs except V _{CC} and GND)	-0.3V to V _{CC} +0.3V	
DC Output Current (All outputs)	20mA	
Power Dissipation	500mW	
	(Depend on package)	

Recommended Operation Condition

Table 3. DC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V _{CC}	Supply Voltage for 75x1, 75x2		4.5	5.0	5.5	V
	Supply Voltage for 75x3, 75x4		3.0	3.3	5.5	V
	Supply Voltage for 75x5, 75x6, 75x7		2.7	3.0	5.5	V
V _{IH1}	\overline{MR} Input High Voltage	V _{CC} > 4.0V	2.0	2.4		V
		V _{CC} ≤ 4.0V	0.7V _{CC}			V
V _{IH2}	WDI Input High Voltage		0.7V _{CC}			V
V _{IL1}	\overline{MR} Input Low Voltage	V _{CC} > 4.0V			0.8	V
		V _{CC} ≤ 4.0V			0.2V _{CC}	V
V _{IL2}	WDI Input Low Voltage				0.3V _{CC}	V
T _A	Operating Temperature		-40		85	°C

DC Electrical Characteristics

Table 4. DC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Unit		
I_{CC}	Operational Power Supply Current	T7A75x1/75x2 $V_{CC} = 5V$ PT7A75x3/75x4 $V_{CC} = 3.3V$ PT7A75x5 $V_{CC} = 3.0V$ PT7A75x6/75x7 $V_{CC} = 2.5V$ Left WDI un-connected (No output load)		30	200	μA		
V_{RST}	Reset Threshold Voltage *	$T_A = 25^\circ C$	$V_{RN} - 1.5\%$	V_{RN}	$V_{RN} + 1.5\%$	V		
		PT7A75x1	4.560	4.630	4.699			
		PT7A75x2	4.314	4.380	4.446			
		PT7A75x3	3.034	3.080	3.126			
		PT7A75x4	2.886	2.930	2.974			
		PT7A75x5	2.590	2.630	2.669			
		PT7A75x6	2.285	2.320	2.355			
V_{RTH}	Reset Threshold Hysteresis *	V_{CC} varies between $V_{RN} - 5\%$		70		mV		
		V_{OH}	Output HIGH Voltage	$V_{CC} > 4.5V$ $I_{source} = 800\mu A$	$V_{CC} - 1.5$		V	
				$V_{CC} > 2.7V$ $I_{source} = 500\mu A$	$0.8V_{CC}$			
				$V_{CC} > 1.8V$ $I_{source} = 150\mu A$	$0.8V_{CC}$			
		V_{OL}	Output LOW Voltage	$V_{CC} > 4.5V$ $I_{sink} = 3.2mA$			0.4	V
				$V_{CC} > 2.7V$ $I_{sink} = 1.2mA$			0.3	
				$V_{CC} > 1.2V$ $I_{sink} = 100\mu A$			0.3	
V_{PFI}	PFI Input Threshold	V_{PFI} varies from 1.0V to 1.5V ($T_A = 25^\circ C$)	1.23	1.25	1.27	V		
		V_{PFI} varies from 1.0V to 1.5V	1.20	1.25	1.30	V		
I_{PFI}	PFI Input Current	PFI connected to V_{CC}			2.00	μA		
		PFI connected to GND	-2.00					
I_{WDI}	Average WDI Input Current**	WDI connected to V_{CC}		30	100	μA		
		WDI connected to GND	-100	-30				
I_{MR}	\overline{MR} Input Current	$\overline{MR} = 0, V_{CC} = 5V$	-600	-250	-100	μA		

* Valid for both \overline{RESET} and RESET. V_{RN} is nominal reset threshold voltage.

** WDI is internally serviced within the watchdog period if WDI is left unconnected.

AC Electrical Characteristics

Table 5. AC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{RS}	Reset Pulse Width	\overline{MR} from low to High	140	200	280	ms
t_{WD}	Watchdog Timeout Period	WDI and \overline{MR} tied to V_{CC} , $V_{CC} > V_{RN} + 5\%$	1.0	1.6	2.25	s
t_{MR}	\overline{MR} Pulse Width		150			ns
t_{MD}	\overline{MR} to RESET Delay	$V_{CC} = 5.0V$			250	ns
t_{WP}	WDI Pulse Width		50			ns

Figure 5. Watchdog Timing Diagram

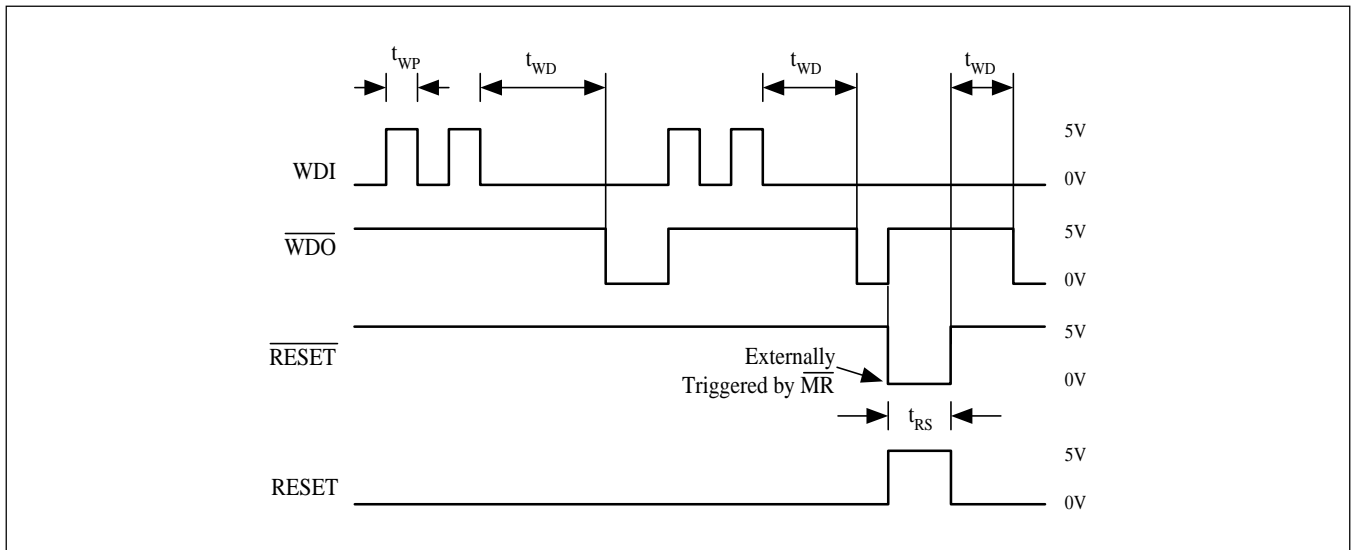
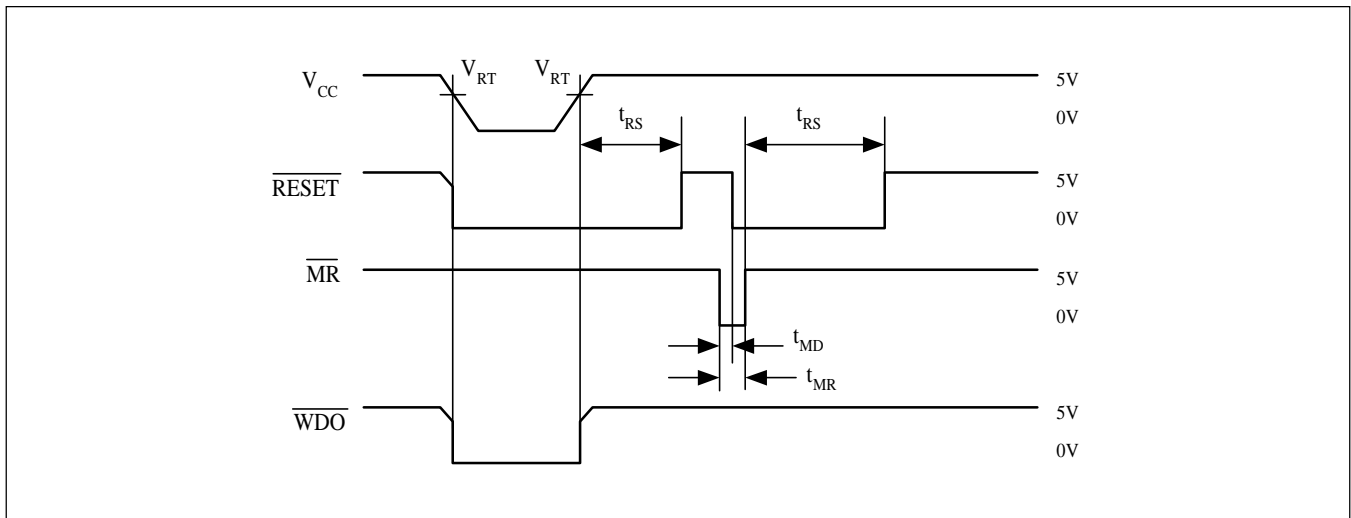


Figure 6. Watchdog Timing Diagram

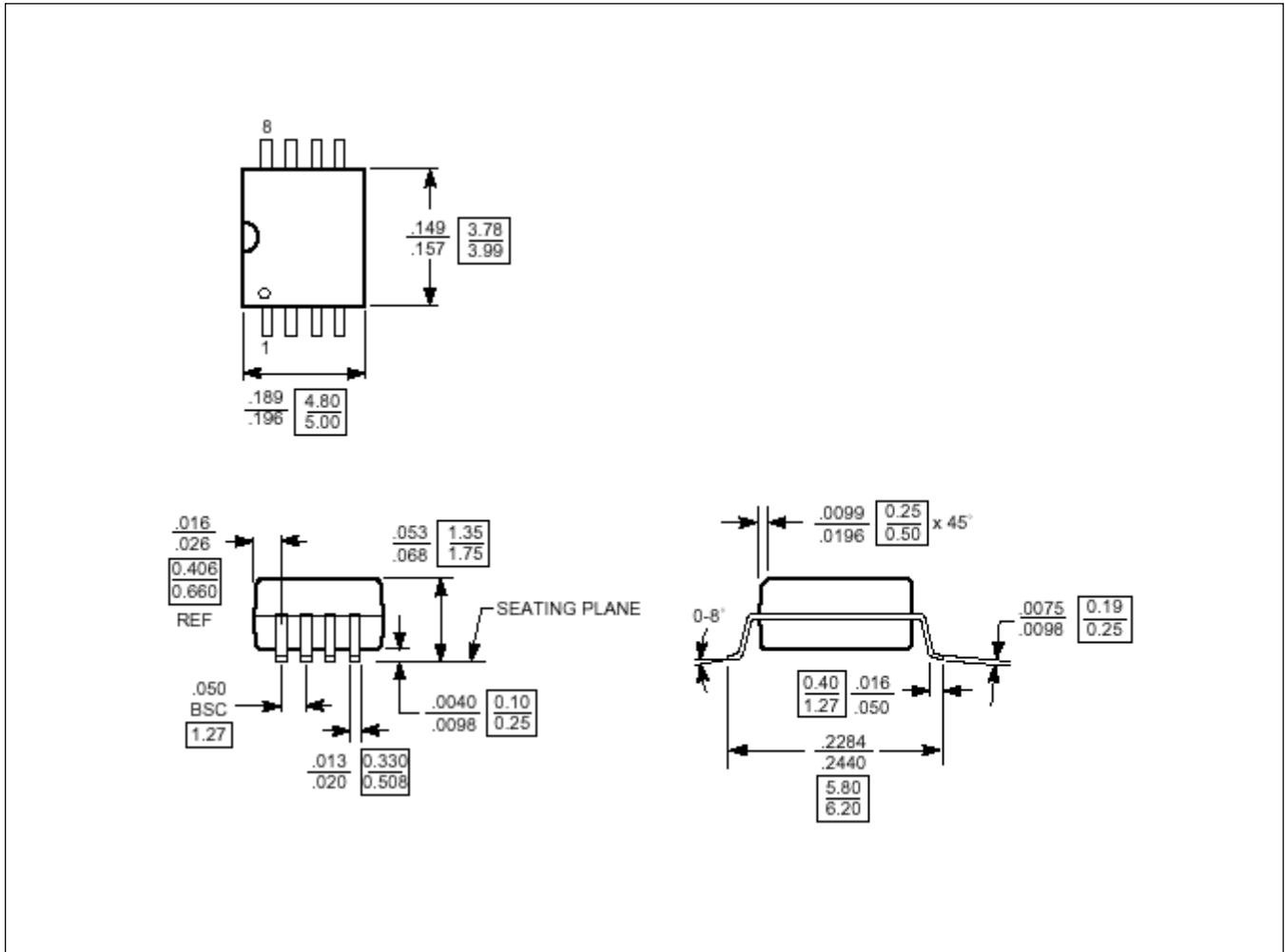


Ordering Information

Part No.	Reset Threshold	Package	Part No.	Reset Threshold	Package
PT7A7511P	4.63V	PDIP-8	PT7A7511W	4.63V	SOIC-8 (150mil)
PT7A7521P	4.63V	PDIP-8	PT7A7521W	4.63V	SOIC-8 (150mil)
PT7A7531P	4.63V	PDIP-8	PT7A7531W	4.63V	SOIC-8 (150mil)
PT7A7512P	4.38V	PDIP-8	PT7A7512W	4.38V	SOIC-8 (150mil)
PT7A7522P	4.38V	PDIP-8	PT7A7522W	4.38V	SOIC-8 (150mil)
PT7A7532P	4.38V	PDIP-8	PT7A7532W	4.38V	SOIC-8 (150mil)
PT7A7513P	3.08V	PDIP-8	PT7A7513W	3.08V	SOIC-8 (150mil)
PT7A7523P	3.08V	PDIP-8	PT7A7523W	3.08V	SOIC-8 (150mil)
PT7A7533P	3.08V	PDIP-8	PT7A7533W	3.08V	SOIC-8 (150mil)
PT7A7514P	2.93V	PDIP-8	PT7A7514W	2.93V	SOIC-8 (150mil)
PT7A7524P	2.93V	PDIP-8	PT7A7524W	2.93V	SOIC-8 (150mil)
PT7A7534P	2.93V	PDIP-8	PT7A7534W	2.93V	SOIC-8 (150mil)
PT7A7515P	2.63V	PDIP-8	PT7A7515W	2.63V	SOIC-8 (150mil)
PT7A7525P	2.63V	PDIP-8	PT7A7525W	2.63V	SOIC-8 (150mil)
PT7A7535P	2.63V	PDIP-8	PT7A7535W	2.63V	SOIC-8 (150mil)
PT7A7516P	2.32	PDIP-8	PT7A7516W	2.32	SOIC-8 (150mil)
PT7A7526P	2.32	PDIP-8	PT7A7526W	2.32	SOIC-8 (150mil)
PT7A7536P	2.32	PDIP-8	PT7A7536W	2.32	SOIC-8 (150mil)
PT7A7517P	2.20	PDIP-8	PT7A7517W	2.20	SOIC-8 (150mil)
PT7A7527P	2.20	PDIP-8	PT7A7527W	2.20	SOIC-8 (150mil)
PT7A7537P	2.20	PDIP-8	PT7A7537W	2.20	SOIC-8 (150mil)

Mechanical Information

Figure 7. 8-Pin SOIC



Notes

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