HD74AC74/HD74ACT74 • Dual D-Type Positive Edge-Triggered Flip-Flop

Description

The HD74AC74/HD74ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

Low input to $\overline{S}_D$ (Set) sets Q to High level

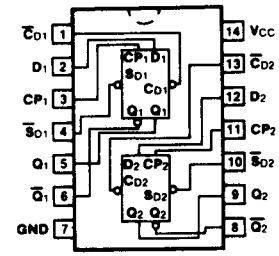
Low input to $\overline{C}_D$ (Clear) sets Q to Low level

Clear and Set are independent of clock

Simultaneous Low on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ High

- Outputs Source/Sink 24 mA
- HD74ACT74 has TTL-Compatible Inputs

Pin Assignment



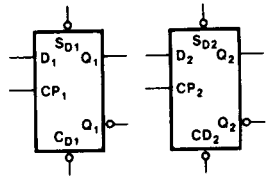
(Top View)

Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
⌐ = Low-to-High Clock Transition
$Q_0(\overline{Q}_0)$ = Previous Q($\overline{Q}$) before Low-to-High Transition of Clock

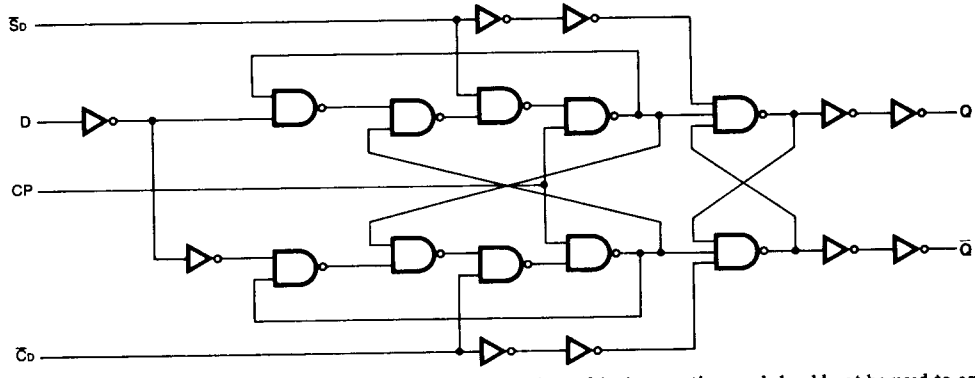
Logic Symbol



Pin Names

D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	40	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5$ V, Ta=Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	$V_{IN}=V_{CC}$ or Ground, $V_{CC}=5.5$ V, Ta=25°C
I_{CCT}	Maximum Additional Icc/Input (HD74ACT74)	1.5	mA	$V_{IN}=V_{CC}-2.1$ V, $V_{CC}=5.5$ V, Ta=Worst Case

AC Characteristics: HD74AC74

Symbol	Parameter	V_{CC}* (V)	Ta=+25°C, C_L=50 pF			Ta=−40°C to +85°C, C_L=50 pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	3.3 5.0	100 140	125 160		95 125		MHz
t_{PLH}	Propagation Delay $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to Q_n or $\overline{Q_n}$	3.3 5.0	1.0 1.0	8.0 6.0	12.0 9.0	1.0 1.0	13.0 10.0	ns
t_{PHL}	Propagation Delay $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to Q_n or $\overline{Q_n}$	3.3 5.0	1.0 1.0	10.5 8.0	12.0 9.5	1.0 1.0	13.5 10.5	ns
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q_n}$	3.3 5.0	1.0 1.0	8.0 6.0	13.5 10.0	1.0 1.0	16.0 10.5	ns
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q_n}$	3.3 5.0	1.0 1.0	8.0 6.0	14.0 10.0	1.0 1.0	14.5 10.5	ns

*Voltage Range 3.3 is 3.3 V±0.3 V
Voltage Range 5.0 is 5.0 V±0.5 V

AC Operating Requirements: HD74AC74

Symbol	Parameter	V_{CC}* (V)	Ta=+25°C, C_L=50 pF		Ta=−40°C to +85°C, C_L=50 pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Set-up Time, HIGH or LOW D_n to CP_n	3.3 5.0	1.5 1.0	4.0 3.0	4.5 3.0	ns
t_h	Hold Time, HIGH or LOW D_n to CP_n	3.3 5.0	−2.0 −1.5	0 0	0 0	ns
t_w	CP_n or $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5	7.0 5.0	ns
t_{rec}	Recovery Time $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to CP	3.3 5.0	−2.5 −2.0	0 0	0 0	ns

*Voltage Range 3.3 is 3.3 V±0.3 V
Voltage Range 5.0 is 5.0 V±0.5 V

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AC Characteristics: HD74ACT74

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50 pF			Ta = −40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	5.0	145	210		125		MHz
t_{PLH}	Propagation Delay $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to Q_n or $\overline{Q_n}$	5.0	1.0	5.5	9.5	1.0	10.5	ns
t_{PHL}	Propagation Delay $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to Q_n or $\overline{Q_n}$	5.0	1.0	6.0	10.0	1.0	11.5	ns
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q_n}$	5.0	1.0	7.5	11.0	1.0	13.0	ns
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q_n}$	5.0	1.0	6.0	10.0	1.0	11.5	ns

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT74

Symbol	Parameter	V_{CC}* (V)	Ta = +25°C, C_L = 50 pF		Ta = −40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
t_{su}	Set-up Time, HIGH or LOW D_n to CP_n	5.0	1.0	3.0	3.5	ns
t_h	Hold Time, HIGH or LOW D_n to CP_n	5.0	−0.5	1.0	1.0	ns
t_w	CP_n or $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ Pulse Width	5.0	3.0	5.0	6.0	ns
t_{rec}	Recovery Time $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to CP	5.0	−2.5	0	0	ns

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5 V
C_{PD}	Power Dissipation Capacitance	35.0	pF	V_{CC} = 5.0 V

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Package Information

In the HD74AC series of Advanced CMOS logic, either plastic DIP and small outline packages can be selected.
To order, please refer to the following package code.

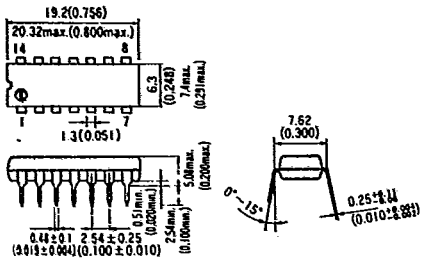
• Package code of Advanced CMOS Logic

HD74AC XXXX P

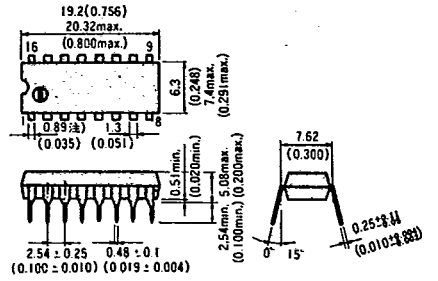
- Package code
  - P: Plastic DIP,
  - FP: Small outline package
- Individual device code
- 74AC: Commercial FACT
- 74ACT: Commercial TTL-Compatible Advanced CMOS
- Initial cad of Hitachi digital IC

Plastic DIP Package [Unit: mm (inch)]

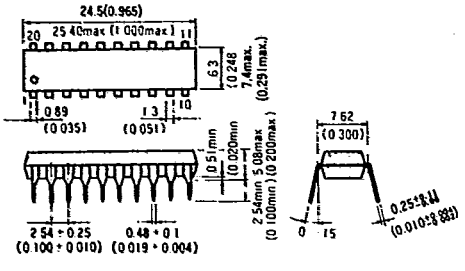
14 Pin type



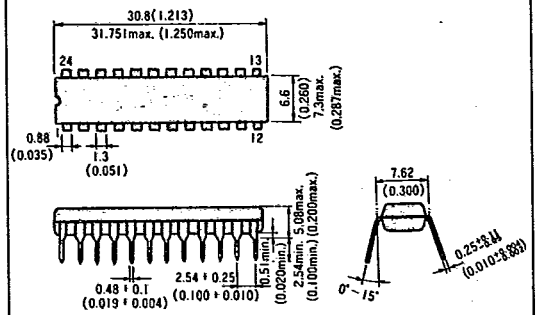
16 Pin type



20 Pin type



24 Pin type



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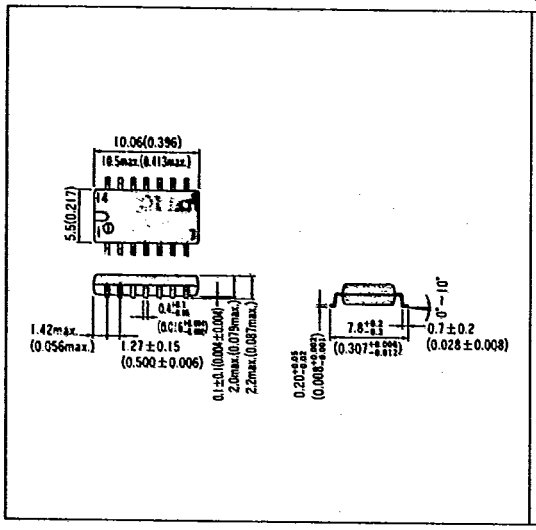
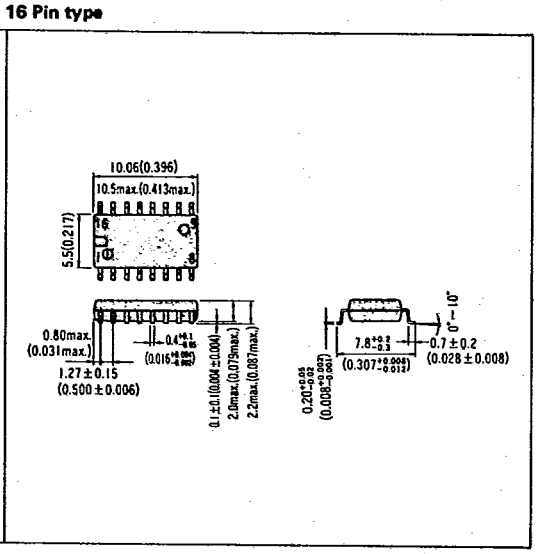
Package Information

Small Outline Package [Unit: mm (inch)]

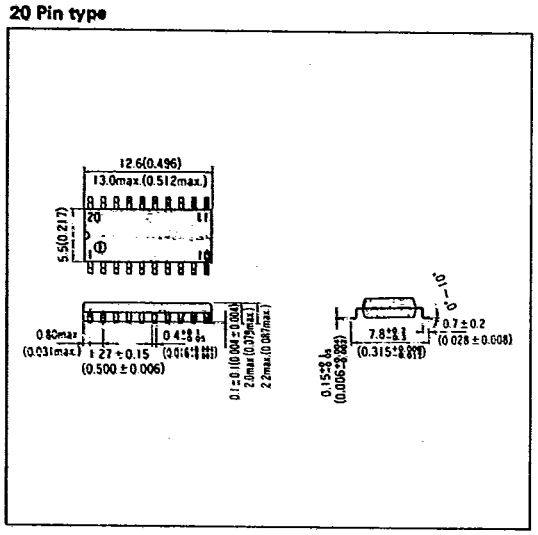
14 Pin type



16 Pin type



20 Pin type



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