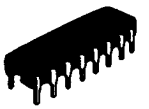
HD44270P/CP Series

Single Chip CODEC/Filter Combo LSI

HD44271P/HD44272P



(DP-16A)

HD44271CP/HD44272CP

(CP-18)

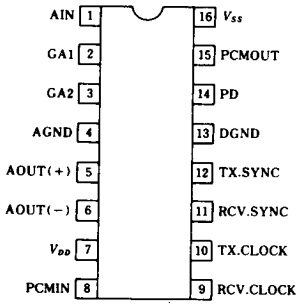
■FEATURES

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package and 18-pins PLCC package.
- Power Supply Voltage ±5V±5%, Low Power Dissipation.
- Follows μ-Law (HD44272P) or A-Law (HD44271P).
- Extremely Low Cost for the Digital PBX Terminal or Digital Handset Application.
- Internal Clock Generator.
- Anti-Aliasing Filter (2nd order CR Active Filter).
- Voltage Reference (Internal-Trimmed).
- Input Amplifier with Uncommitted Plus/Minus Terminals.
- Auto-Zero Cancel Circuit without External Component.
- Push/Pull Analog Output.

Type	Original Versions	Comp. Law	Power (Typ.)	Clock			Input Amp	Output Amp	
				Internal clock	Sync/Async Operation	PCM bit clock rate		Type	Min load
HD44271P	HD44247C	A	70mW	PLL Included	Both	64-2048kHz	Fully Uncommited Op-amp	Push-Pull	600Ω
HD44272P	HD44248C	μ	70mW						
HD44273P	HD44233C	A	50mW	Divider Included		1536/1544/2048 kHz		Single Ended	
HD44274P	HD44234C	μ	50mW						
HD44277P	HD44237C	A	50mW	PLL Included		64-2048kHz			
HD44278P	HD44238C	μ	50mW						

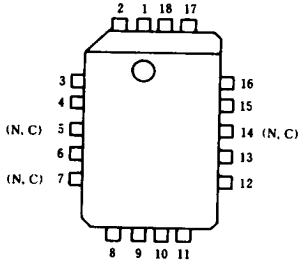
■ PIN ARRANGEMENT

●HD44271P/272P



(Top View)

●HD44271CP/272CP



(Top View)

■ PIN DESCRIPTIONS

No. P	No. CP	Symbol	Function	Remarks
1	1	AIN	Analog input	
2	2	GAI	Gain adjust 1	Feed-back input
3	3	GA2	Gain adjust 2	10kΩ < R_L, C_L < 100pF
4	4	AGND	Analog ground	
5	6	AOUT(+)	Analog output	R_L > 600Ω, C_L < 100pF
6	7	AOUT(−)		R_L > 600Ω, C_L < 100pF
7	8	V_{DD}	Positive pow. sup.	5V ± 5%
8	9	PCMIN	PCM data input	(TTL)
9	10	RCV. CLK	PCM bit clock	(TTL) 64kHz to 2048kHz
10	11	TX. CLK		
11	12	RCV. SYNC	Synchronization	(TTL) 8kHz
12	13	TX. SYNC		
13	15	DGND	Digital ground	
14	16	PD	Power down	(TTL) "0" = down
15	17	PCMOUT	PCM data output	Open drain
16	18	V_{SS}	Negative pow. sup.	−5V ± 5%
—	5, 14	N.C.	—	Open

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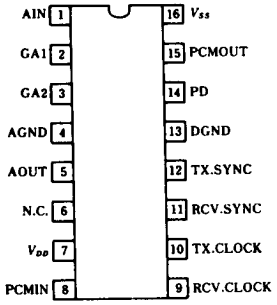
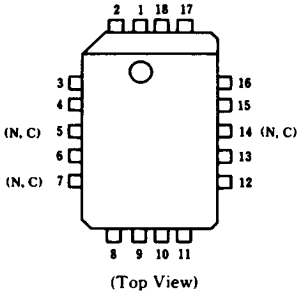
■PIN ARRANGEMENT

● HD44273P/274P



(Top View)

● HD44273CP/274CP

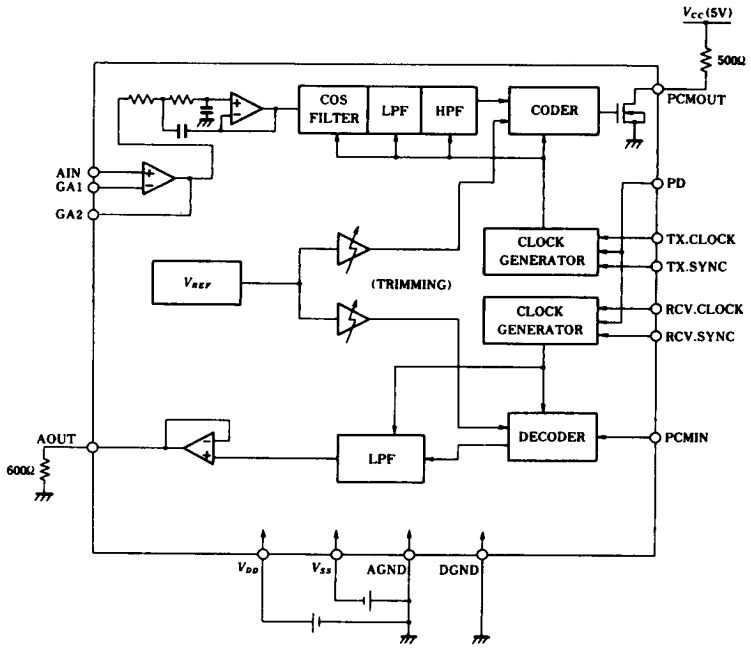


(Top View)

■PIN DESCRIPTIONS

No.		Symbol	Function	Remarks
P	CP			
1	1	AIN	Analog input	
2	2	GA1	Gain adjust 1	Feed-back input
3	3	GA2	Gain adjust 2	10kΩ < R_L C_L < 100pF
4	4	AGND	Analog ground	
5	6	AOUT	Analog output	R_L > 600Ω, C_L < 100pF
7	8	V_{DD}	Positive pow. sup.	5V ± 5%
8	9	PCMIN	PCM data imput	(TTL)
9	10	RCV. CLK	PCM bit clock	(TTL) 2048/1544/ 1536kHz
10	11	TX. CLK		
11	12	RCV. SYNC	Synchronization	(TTL) 8kHz
12	13	TX. SYNC		
13	15	DGND	Digital ground	
14	16	PD	Power down	(TTL) "0" = down
15	17	PCMOUT	PCM data output	Open drain
16	18	V_{SS}	Negative pow. sup.	−5V ± 5%
6	5, 7, 14	N.C.	—	Open

■BLOCK DIAGRAM



*ONLY FOR HD44271, 272P/CP

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■PIN/FUNCTION DESCRIPTIONS

HD44271P/CP, HD44272P/CP, HD44277P/CP, HD44278P/CP

Pin	No		Descriptions
	P	CP	
TX. CLOCK RCV. CLOCK	9 10	10 11	Any of 64kHz to 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX. SYNC/RCV. SYNC respectively.
TX. SYNC RCV. SYNC	11 12	12 13	These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK/RCV. CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	17	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK. TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC. TX/SYNC. RCV. SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV. CLOCK.
AIN GA1 GA2	1 2 3	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device The input stage can be connected as a unity gain amplifier, with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10k Ω or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT(+)	5	6	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100pF.
V_{DD} V_{SS} AGND DGND	7 16 4 13	8 18 4 15	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	16	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
AOUT(−)*	6	7	This is the inverted output of pin 5 signal output to drive the 600 Ω transformer as the push-pull operation. $R_L < 600\Omega$, $C_L < 100$pF.

*ONLY FOR HD44271, 272P/CP

■PIN/FUNCTION DESCRIPTIONS

HD44273P/CP, HD44274P/CP

Pin	No		Descriptions
	P	CP	
TX. CLOCK RCV. CLOCK	9 10	10 11	One of 1.536, 1.544 and 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX. SYNC/RCV. SYNC respectively.
TX. SYNC RCV. SYNC	11 12	12 13	These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK/RCV. CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	17	This is a LS-TTL compatible open-drain output. It is active only during transmisson of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX/SYNC. RCV. SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	9	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV. CLOCK.
AIN GA1 GA2	1 2 3	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. The input stage can be connected as a unity gain amplifier, with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10k Ω or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT	5	6	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100pF.
V_{DD} V_{SS} AGND DGND	7 16 4 13	8 18 4 15	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	16	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.

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■ABSOLUTE MAXIMUM RATINGS

Item	Rating
V_{DD}	−0.3 to +7V
V_{SS}	+0.3 to −7V
Storage temperature	−55°C to +125°C
Power dissipation	0.5W
Digital input/output voltage	$-0.3V < V_{IN} < V_{DD}+0.3V$
Analog input/output voltage	$V_{SS}-0.3V < V_{IN} < V_{DD}+0.3V$

■ELECTRICAL CHARACTERISTICS

●STATIC CHARACTERISTICS ($V_{DD}=5\pm0.25V$, $V_{SS}=-5\pm0.25V$, $V_{CC}=5\pm0.25V$, $T_a=0$ to $+70°C$)

Descriptions	Symbol	Pin	min	typ	max	Note/conditions	Unit
V_{DD} current (ope.)	I_{DD}	7	−	8.0	13.5	Note 1 AIN=0V PCMIN = +0 code R_L (GA2)=10kΩ R_L (AOUT)=600Ω	mA
V_{SS} current (ope.)	I_{SS}	16	−13.0	−7.5	−		
V_{DD} current (st.by.)	I_{DDST}	7	−	0.4	1.0		
V_{SS} current (st.by.)	I_{SSST}	16	−0.2	−	−		
Leak current	I_L	1, 2, 8 9, 10 14	−10.0	−	10.0	$V_M=0.8V$	μA
			−10.0	−	10.0	$V_M=2.0V$	μA
			−	−	10.0	$V_{DD}=V_M=5.25V$	μA
Pull up current	I_{PL}	11, 12	−100	−	0		μA
Leak current	I_{DL}	15	−	−	10.0	$V_{DD}=V_M=5.25V$	μA
Analog input cap.	C_{AIN1}	1	−	−	10	at 1MHz Vbias=0	pF
Analog input cap.	C_{AIN2}	2	−	−	10	at 1MHz Vbias=0	pF
Input capacitance	C_{DIN}	8,9,10,11,12,14	−	−	10	at 1MHz Vbias=0	pF
AOUT resistance	R_{OUTA}	5, 6	−	1	20		Ω
GA2 resistance	R_{OUTG}	3	−	−	50	Note 1	Ω
GA2 output swing	V_{GSW}	3	−3.0	−	3.0	$R_L=10k\Omega$	V
Analog offset input	V_{OFFIN}	1	−200	−	200	Note 1	mV
GA2 offset output	V_{OFFG}	3	−50	−	50	Note 1	mV
AOUT offset output	V_{OFFA}	5, 6	−100	−	100	PCMIN = +0−code	mV
PCMOUT capacitance	C_{DOUT}	15	−	−	15.0	at 1MHz,Vbias=0V	pF
PCMOUT low voltage	V_{OL}	15	−	−	0.4	$R_L=500\Omega$, $+I_{OL}=0.8mA$	V
PCMOUT high voltage	V_{OH}	15	$V_{CC}-0.3$	−	−	$I_{OH}=-150\mu A$	V
Digital input high voltage	V_{IH}	8,9,10,11,12,14	2.0	−	−		V
Digital input low voltage	V_{IL}	8,9,10,11,12,14	−	−	0.8		V

Note 1) Analog input amplifier gain = 0 dB (GA1 is connected to GA2)
( ) : Only for HD44271, 272P/CP

●DYNAMIC-CHARACTERISTICS (V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C)

Descriptions	Symbol	Note	min	typ	max	Unit
Synchronization rate	F_S		–	8	–	kHz
PCM bit clock rate	F_C		64	–	2048	kHz
Clock pulse width	t_{wc}		200	–	–	ns
Sync pulse high width	t_{wSH}		200	–	–	ns
Sync pulse low width	t_{wSL}		8	–	–	ns
Logic input rise time	t_r		5	–	50	ns
Logic input fall time	t_f		5	–	50	ns
Previous clock to Sync delay	t_{HCS}	Note 1	40	–	–	ns
Clock to sync delay	t_{cs}	Note 1, 3	–	–	100	ns
Clock to PCM MSB delay	t_{cdd}	Note 1, 2, 4	–	–	170	ns
Sync to PCM MSB delay	t_{sd}	Note 1, 2, 4	–	–	170	ns
Clock to PCM OUT delay	t_{cd}	Note 1, 2, 5	–	–	180	ns
PCMIN setup time	t_{su}	Note 1	65	–	–	ns
PCMIN hold time	t_{hd}	Note 1	120	–	–	ns

Note 1) t_r, t_f of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT load condition: 500 Ω + 165pF + two LS-TTL Equivalent (I_{IL} = 0.8mA, I_{IH} = −150μA) Threshold level (V_{IH} = 2.4V, V_{IL} = 0.4V)
3) Positive value shows SYNC delay from CLOCK.
4) t_{cdd}, t_{sd} are specified by CLOCK or SYNC which has slower rise time.
5) t_{cd} specification is valid for the data except MSB.

●SYSTEM RELATED CHARACTERISTICS

(V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C, INPUT AMPLIFIER GAIN = 0dB, ANALOG OUT PUT = AOUT(−), GA2 LOAD = 10k Ω, AOUT LOAD = 600 Ω, Synchronous operation. fc (PCM BIT CLOCK) = 2048kHz)

A-law (HD44271P/CP, HD44273P/CP, HD44277P/CP)

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	820Hz tone	−45dBm0	23	–	–	dB	p-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain track. (A to A)	GTA	820Hz tone Relative to −10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10,0,3	−0.3	–	0.3		
Freq. response. (A to D)(Loss)	FRX	Relative to 820Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq. response.(D to A)(Loss)	FRR	Relative to 820Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level variation	AIL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	−80	dBm0P	
Idle ch. noise	ICNR	D to A	PCMIN = +0−Code	–	–	−80	dBm0P	
AIN to AOUT crosstalk	XTKA	820Hz	0dBm0	–	–	−65	dB	
PCMIN to PCMOUT	XTKD	820Hz	0dBm0	–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

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Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	−80	dBm0P	
Idle ch. noise	ICNR	D to A	PCMIN = +0−code	–	–	−80	dBm0P	
AIN to AOUT crosstalk	XTKA	820Hz	0 dBm 0	–	–	−65	dB	
PCMIN to PCMOUT crosstalk	XTKD	820Hz	0 dBm 0	–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

μ-law (HD44272P/CP, HD44274P/CP, HD44278P/CP)

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	1020Hz tone	−45dBm0	23	–	–	dB	c-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain Tracking(A to A)	GTA	1020Hz tone relative to −10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10,0,3	−0.3	–	0.3		
Freq.Response.(A to D)(Loss)	FRX	Relative to 1020Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq.Response.(D to A)(Loss)	FRR	Relative to 1020Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level	AIL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	16	dBrnC0	
Idle ch. noise	ICNR	D to A	PCMIN = +0−code	–	–	10	dBrnC0	
AIN to AOUT crosstalk	XTKA	1020Hz 0dBm0		–	–	−65	dB	
PCMIN to PCMOUT crosstalk	XTKD	1020Hz 0dBm0		–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

■TIMING CHART