REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-07-30

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 4K X 8/9 RADIATION-HARDENED DUAL-PORT STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-96845**

SHEET 1 OF 31

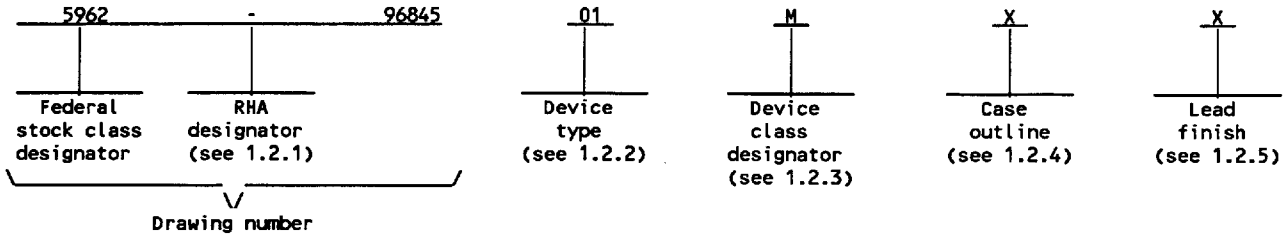
DESC FORM 193
JUL 94

5962-E476-96

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Data retention	Access time
01	7C138C45	4K X 8 Dual port SRAM	Yes	45 ns
02	7C139C45	4K X 9 Dual port SRAM	Yes	45 ns
03	7C138C55	4K X 8 Dual port SRAM	Yes	55 ns
04	7C139C55	4K X 9 Dual port SRAM	Yes	55 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	68	Pin grid array
Y	See figure 1	68	Quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Short circuit output current	90 mA
Maximum power dissipation (P_D)	2.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	3.3°C/W 4/
Maximum junction temperature (T_J)	+175°C 5/
DC input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc 6/
DC output voltage range	-0.5 V dc to V_{CC} + 0.5 V dc 6/
Output voltage applied in high Z state	-0.5 V dc to V_{CC} + 0.5 V dc

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage range (V_{IH})	0.7 V_{CC} to 6.0 V dc
Low level input voltage range (V_{IL})	-0.5 V dc to +0.3 V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 (see 6.6.2 herein).
2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltages referenced to GND unless otherwise specified.
4/ Measured per MIL-STD-883, Method 1012, infinite heat sink.
5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
6/ Negative undershoots to a minimum of -3.0 V are allowed with a maximum of 20 ns pulse width.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 AC test circuit and waveforms. The ac test circuit and waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.2.6 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output low voltage (TTL)	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA,	1, 2, 3	All		0.4	V
		M,D,L,R,F,G,H	1 1/			2/	
Output low voltage (CMOS)	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 200µA,	1, 2, 3	All		0.05	V
		M,D,L,R,F,G,H	1 1/			2/	
Output high voltage (TTL)	V_{OH}	V_{CC} = 4.5 V, I_{OL} = -4mA,	1, 2, 3	All	2.4		V
		M,D,L,R,F,G,H	1 1/		2/		
Output high voltage (CMOS)	V_{OH}	V_{CC} = 4.5 V, I_{OL} = -200µA,	1, 2, 3	All	4.45		V
		M,D,L,R,F,G,H	1 1/		2/		
Low-level input voltage (CMOS)	V_{IL}		1, 2, 3	All		0.3 V_{CC}	V
		M,D,L,R,F,G,H	1 1/			2/	
High-level input voltage (CMOS)	V_{IH}		1, 2, 3	All	0.7 V_{CC}		V
		M,D,L,R,F,G,H	1 1/		2/		
Input leakage current	I_{LI}	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	1, 2, 3	All	-10	10	µA
		M,D,L,R,F,G,H	1 1/		2/	2/	
Three-state output leakage current	I_{LO}	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}, V_{OUT} = 0 V to V_{CC}	1, 2, 3	All	-10	10	µA
		M,D,L,R,F,G,H	1 1/		2/	2/	
Short-circuit output current 3/ 4/	I_{OS}	V_O = V_{CC}, V_{CC} = 5.5 V	1, 2, 3	All		90	mA
		M,D,L,R,F,G,H	1 1/			2/	
		V_{CC} = 5.5 V, V_O = 0V	1, 2, 3	All	-90		mA
		M,D,L,R,F,G,H	1 1/		2/		
Operating supply current (both ports active) 5/	I_{CC1}	CMOS inputs (I_{OUT} = 0) V_{CC} = 5.5 V, f = 22.2 Mhz V_{IH} = 5.5 V, V_{IL} = 0 V,	1, 2, 3	01,02		300	mA
		M,D,L,R,F,G,H	1 1/			2/	
Operating supply current (one port active) 6/	I_{CC2}	CMOS inputs (I_{OUT} = 0) V_{CC} = 5.5 V, f = 22.2 Mhz V_{IH} = 5.5 V, V_{IL} = 0 V,	1, 2, 3	01,02		150	mA
		M,D,L,R,F,G,H	1 1/			2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Operating supply current (both ports active) 5/	I_{CC3}	CMOS inputs (I_{OUT} = 0) V_{CC} = 5.5 V, f = 18.2 Mhz V_{IH} = 5.5 V, V_{IL} = 0 V	1, 2, 3	All		275	mA
		M,D,L,R,F,G,H	1 1/			2/	
Operating supply current (one port active) 6/	I_{CC4}	CMOS inputs (I_{OUT} = 0) V_{CC} = 5.5 V, f = 18.2 MHz V_{IH} = 5.5 V, V_{IL} = 0 V	1, 2, 3	All		138	mA
		M,D,L,R,F,G,H	1 1/			2/	
Full standby current	I_{CC5}	V_{CC} = 5.5 V, $\overline{CE}$ = V_{CC}-0.5 CMOS inputs (I_{OUT} = 0) V_{IH} = V_{CC}-0.5 V, V_{IL} = +0.5 V,	1, 2, 3	All		1	mA
		M,D,L,R,F,G,H	1 1/			2/	
Input capacitance 7/	C_{IN}	V_{IN} = 0 V, V_{CC} = 5.0 V, f = 1MHz, T_A = 25°C, see 4.4.1e	4	All		25	pF
Bidirectional input/output capacitance 7/	$C_{I/O}$	V_{OUT} = 0 V, V_{CC} = 5.0 V, f = 1MHz, T_A = 25°C, see 4.4.1e	4	All		25	pF
Functional testing		See 4.4.1c	7, 8A, 8B	All			
		M,D,L,R,F,G,H	7 1/		2/		
Data retention voltage	V_{DR}	$\overline{CE} \ge V_{CC}$ - 0.2 V, $V_{IN} \ge V_{CC}$ - 0.2 V or $\le$ 0.2 V	1, 2, 3	All	2.5		V
		M,D,L,R,F,G,H	1 1/		2/		
Data retention current	I_{CCR}	V_{CC} = 2.5 V, $\overline{CE}$ = V_{DR}, All other inputs = V_{DR} or V_{SS}	1, 2, 3	All		400	µA
		M,D,L,R,F,G,H	1 1/			2/	
Chip deselect to data retention time 8/	t_{EFR}	See figures 4 and 5 9/ 10/	9, 10, 11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Operation recovery time 8/	t_R	$\overline{CE}$ = V_{DR}, All other inputs = V_{DR} or V_{SS}	9, 10, 11	All	t_{RC}		ns
		M,D,L,R,F,G,H	9 1/		2/		
Read cycle time	t_{RC}	See figures 4 and 5 9/ 10/	9, 10, 11	03,04	55		ns
				01,02	45		
		M,D,L,R,F,G,H	9 1/		2/		
Address access time	t_{AA}		9, 10, 11	03,04		55	ns
				01,02		45	
		M,D,L,R,F,G,H	9 1/			2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable access time	t_{ACE}	See figures 4 and 5 9/ 10/	9, 10, 11	03,04		55	ns
				01,02		45	
		M,D,L,R,F,G,H	9 1/			2/	
Output enable access time	t_{DOE}		9, 10, 11	All		20	ns
		M,D,L,R,F,G,H	9 1/			2/	
Output hold from address change	t_{OHA}		9, 10, 11	All	5		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output enable to output active	t_{LZOE}		9, 10, 11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output disable to output inactive	t_{HZOE}		9, 10, 11	All		20	ns
		M,D,L,R,F,G,H	9 1/			2/	
Chip enable to output active	t_{LZCE}		9, 10, 11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Chip disable to output inactive	t_{HZCE}		9, 10, 11	All		20	ns
		M,D,L,R,F,G,H	9 1/			2/	
Write cycle time	t_{WC}		9, 10, 11	03,04	55		ns
				01,02	45		
		M,D,L,R,F,G,H	9 1/		2/		
Address valid to end of write	t_{AW}		9, 10, 11	03,04	50		ns
				01,02	40		
		M,D,L,R,F,G,H	9 1/		2/		
Write pulse width	t_{PWE}		9, 10, 11	03,04	50		ns
				01,02	40		
		M,D,L,R,F,G,H	9 1/		2/		
Chip enable to end of write	t_{SCE}		9, 10, 11	03,04	50		ns
				01,02	40		
		M,D,L,R,F,G,H	9 1/		2/		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address set-up time	t_{SA}	See figures 4 and 5 9/ 10/	9, 10, 11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Write recovery time	t_{HA}		9, 10, 11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Data valid to end of write	t_{SD}		9, 10, 11	03,04	50		ns
				01,02	40		
		M,D,L,R,F,G,H	9 1/		2/		
Data hold time	t_{HD}		9, 10, 11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
$\overline{R/W}$ LOW to high Z	t_{HZWE}		9, 10, 11	All		20	ns
		M,D,L,R,F,G,H	9 1/			2/	
$\overline{R/W}$ HIGH to low Z	t_{LZWE}		9, 10, 11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Write pulse to data delay	t_{WDD}		9, 10, 11	03,04	105		ns
				01,02	95		
		M,D,L,R,F,G,H	9 1/		2/		
Write data valid to read data valid	t_{DDD}		9, 10, 11	03,04	105		ns
				01,02	95		
		M,D,L,R,F,G,H	9 1/		2/		
Write disable time	t_{WHWL}		9, 10, 11	All	5		ns
		M,D,L,R,F,G,H	9 1/		2/		
$\overline{BUSY}$ access time from address match	t_{BLA}		9, 10, 11	03,04		30	ns
				01,02		25	
		M,D,L,R,F,G,H	9 1/			2/	
$\overline{BUSY}$ disable time from address not matched	t_{BZA}		9, 10, 11	03,04		30	ns
				01,02		25	
		M,D,L,R,F,G,H	9 1/			2/	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{BUSY}$ access time from chip enable low	t_{BLC}	See figures 4 and 5 9/ 10/	9, 10, 11	03,04		30	ns
				01,02		25	
		M,D,L,R,F,G,H	9 1/			2/	ns
$\overline{BUSY}$ disable time from chip enable high	t_{BZC}		9, 10, 11	03,04		30	ns
				01,02		25	
		M,D,L,R,F,G,H	9 1/			2/	ns
Arbitration priority set-up time 11/ 12/	t_{PS}		9, 10, 11	All		5	ns
		M,D,L,R,F,G,H	9 1/			2/	ns
$\overline{BUSY}$ disable to valid data	t_{BDD}		9, 10, 11	03,04		55	ns
				01,02		45	
		M,D,L,R,F,G,H	9 1/			2/	ns
$\overline{BUSY}$ input to write	t_{WB}		9, 10, 11	All		0	ns
		M,D,L,R,F,G,H	9 1/			2/	ns
Write hold after $\overline{BUSY}$	t_{WH}		9, 10, 11	03,04		50	ns
				01,02		40	
		M,D,L,R,F,G,H	9 1/			2/	ns

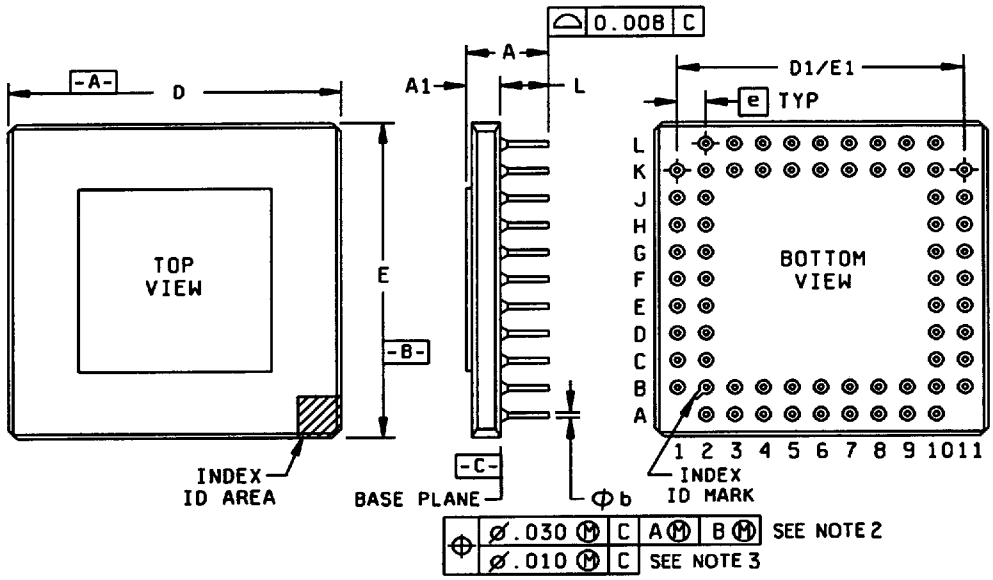
1/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C$. The M, D, L, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.
2/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
3/ Supplied as a design limit but not guaranteed or tested.
4/ Not more than one output may be shorted at a time for maximum duration of one second.
5/ I_{CC1} derates at 6.4mA/MHz.
6/ I_{CC2} derates at 3.2mA/MHz.
7/ Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
8/ Guaranteed, but not tested.
9/ Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC}/2$, input pulse levels of 0.5V to V_{CC}-0.5V, and output loading of the specified I_{OL}/I_{OH} and 50 pF load capacitance.
10/ AC test conditions use $V_{OH}/V_{OL} = V_{CC}/2 \pm 350mV$.
11/ Violation of t_{PS} (with addresses matching) results in at least one of the two busy output signals asserting, only one port remains busy.
12/ When violating t_{PS}, the busy signal asserts on one port or the other; there is no guarantee on which port the busy signal asserts.

TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C 3/	Memory Pattern	V_{CC} = 4.5 V		Bias for latch-up test V_{CC} = 5.5 V no latch-up LET = 3/
			Effective LET no upsets [MEV/(mg/cm^2)]	Maximum device cross section (cm^2) (LET = 120)	
All	+125°C	4/	≥ 65	5/	≥ 120

1/ For SEP test conditions, see 4.4.4 herein.
2/ Technology characterization and model verification supplemented by the in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature T_A = +125°C.
4/ Testing shall be performed using checkerboard and checkerboard bar test patterns
5/ ≤ 1.376 E $^{-2}$ for device types 01 and 03; ≤ 1.548 E $^{-2}$ for device types 02 and 04.

Case outline X

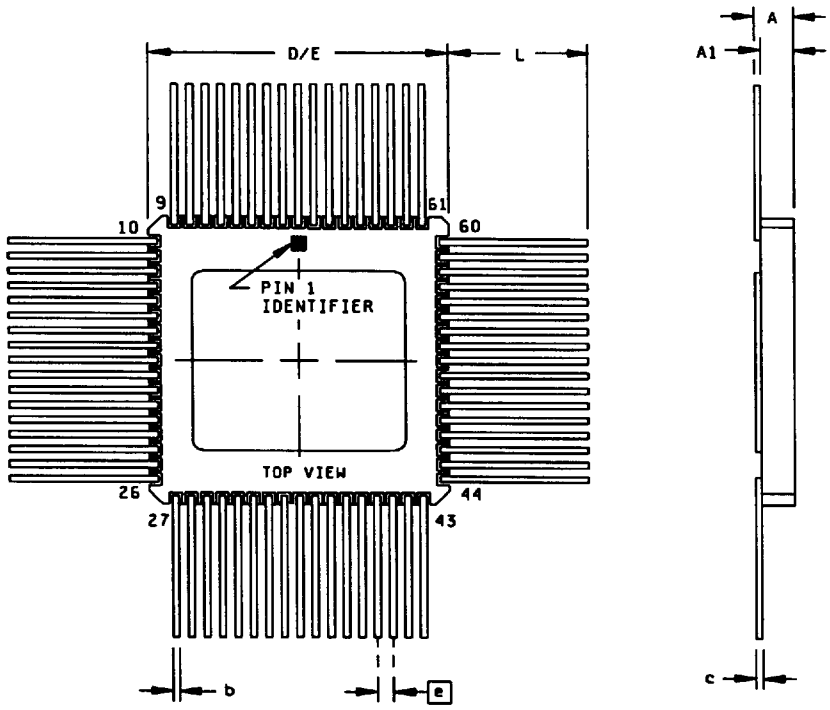


Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	6.2	7.1	.245	.280	E	29.0	30.0	1.14	1.18
A1	1.9	2.3	.075	.090	E1	25.4 Ref.		1.00 Ref.	
ϕb	0.41	0.5	.016	.020	e	2.54 BSC		.100 BSC	
D	29.0	30.0	1.140	1.180	L	4.32	4.83	.170	.190
D1	25.4 Ref.		1.00 Ref.		N	68			

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2. True position applies at base plane (Datum C).
3. True position applies at pin tips.
4. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

FIGURE 1. Case outline.

Case outline Y



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	1.9	2.29	.075	.090	D	21.6	24.50	.850	.965
A1	1.5	1.85	.059	.073	E	21.6	24.50	.850	.965
b	0.35	0.46	.014	.018	e	1.27 Typ.		.050 Typ.	
C	0.18	0.23	.007	.009	N	68			
L	6.35	---	.250	---					

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2. All leads increase max limit by 0.003 inches measured at the center of the flat when lead finish A is applied.
3. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

FIGURE 1. Case outline - continued.

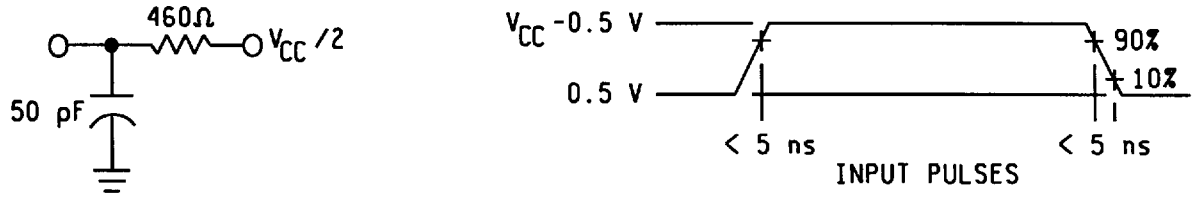
Device types		All									
Case outline		X	Y		X	Y		X	Y		
Terminal number		Terminal symbol	Terminal symbol	Terminal number		Terminal symbol	Terminal symbol	Terminal number		Terminal symbol	Terminal symbol
X	Y			X	Y			X	Y		
B2	1	I/O_{2L}	NC	K5	24	NC	I/O_{4R}	D10	47	A_{1L}	A_{1R}
B1	2	I/O_{3L}	NC	L5	25	NC	I/O_{5R}	D11	48	A_{2L}	A_{0R}
C2	3	I/O_{4L}	$\overline{CE}_L$	K6	26	GND	I/O_{6R}	C10	49	A_{3L}	NC
C1	4	I/O_{5L}	NC	L6	27	NC	I/O_{7R}	C11	50	A_{4L}	$\overline{BUSY}_R$
D2	5	GND	$R/\overline{W}_L$	K7	28	A_{11R}	NC	B11	51	A_{5L}	$M/\overline{S}$
D1	6	I/O_{6L}	$\overline{OE}_L$	L7	29	A_{10R}	$\overline{OE}_R$	B10	52	A_{6L}	GND
E2	7	I/O_{7L}	NC	K8	30	A_{9R}	$R/\overline{W}_R$	A10	53	A_{7L}	$\overline{BUSY}_L$
E1	8	V_{CC}	I/O_{0L}	L8	31	A_{8R}	NC	B9	54	A_{8L}	NC
F2	9	GND	I/O_{1L}	K9	32	A_{7R}	$\overline{CE}_R$	A9	55	A_{9L}	A_{0L}
F1	10	I/O_{0R}	I/O_{2L}	L9	33	A_{6R}	NC	B8	56	A_{10L}	A_{1L}
G2	11	I/O_{1R}	I/O_{3L}	L10	34	A_{5R}	NC	A8	57	A_{11L}	A_{2L}
G1	12	I/O_{2R}	I/O_{4L}	K10	35	A_{4R}	GND	B7	58	NC	A_{3L}
H2	13	V_{CC}	I/O_{5L}	K11	36	A_{3R}	NC	A7	59	V_{CC}	A_{4L}
H1	14	I/O_{3R}	GND	J10	37	A_{2R}	A_{11R}	B6	60	NC	A_{5L}
J2	15	I/O_{4R}	I/O_{6L}	J11	38	A_{1R}	A_{10R}	A6	61	NC	A_{6L}
J1	16	I/O_{5R}	I/O_{7L}	H10	39	A_{0R}	A_{9R}	B5	62	$\overline{CE}_L$	A_{7L}
K1	17	I/O_{6R}	V_{CC}	H11	40	NC	A_{8R}	A5	63	NC	A_{8L}
K2	18	I/O_{7R}	GND	G10	41	$\overline{BUSY}_R$	A_{7R}	B4	64	$R/\overline{W}_L$	A_{9L}
L2	19	NC	I/O_{0R}	G11	42	$M/\overline{S}$	A_{6R}	A4	65	$\overline{OE}_L$	A_{10L}
K3	20	$\overline{OE}_R$	I/O_{1R}	F10	43	GND	A_{5R}	B3	66	NC	A_{11L}
L3	21	$R/\overline{W}_R$	I/O_{2R}	F11	44	$\overline{BUSY}_L$	A_{4R}	A3	67	I/O_{0L}	NC
K4	22	NC	V_{CC}	E10	45	NC	A_{3R}	A2	68	I/O_{1L}	V_{CC}
L4	23	$\overline{CE}_R$	I/O_{3R}	E11	46	A_{0L}	A_{2R}				

NOTE: For device types 02 and 04, pins L2 and B3 are I/O_{8R} and I/O_{8L} respectively for case outline "X", and for pins 7 and 28 are I/O_{8L} and I/O_{8R} respectively for case outline "Y".

FIGURE 2. Terminal connections.

INPUTS			OUTPUTS	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	I/O_{0-7}	OPERATION
H	X	X	High Z	Power Down
X	X	H	High Z	I/O Lines Disabled
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	X	X	---	Illegal Condition

FIGURE 3. Truth table.



NOTES: 1. 50 pF includes scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point.

FIGURE 4. Test circuit and switching waveforms.

LOW V_{DD} DATA RETENTION WAVEFORM

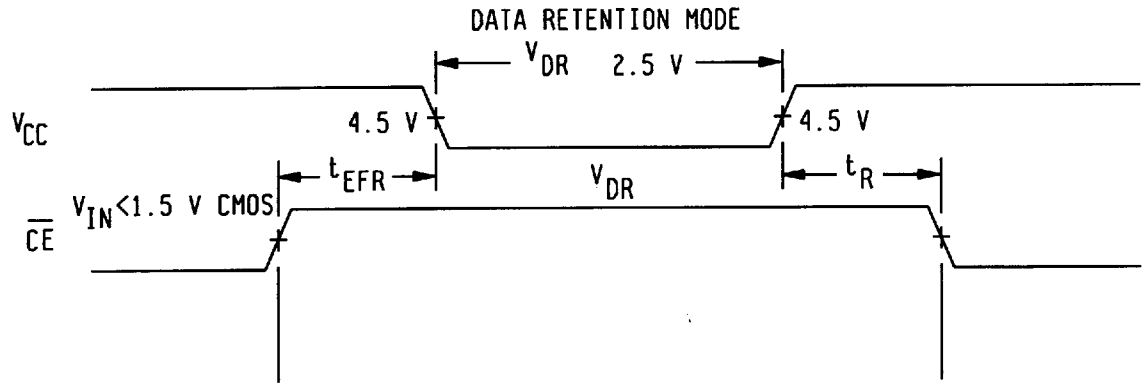
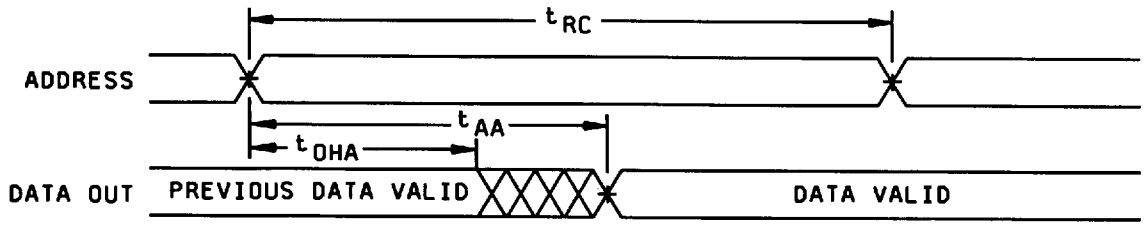


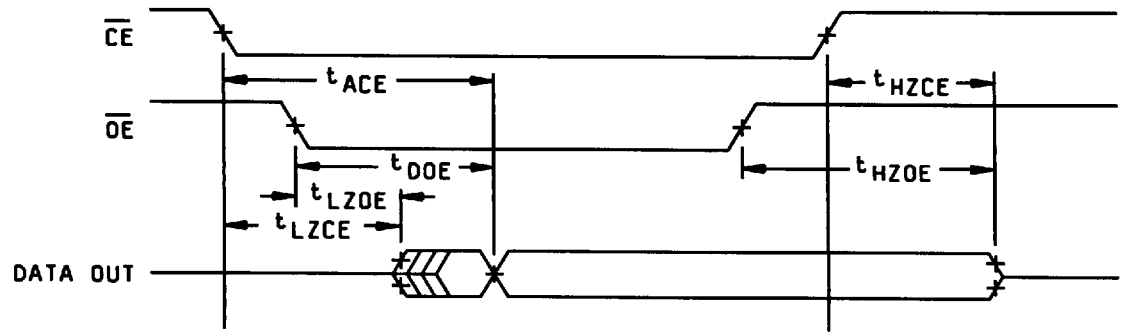
FIGURE 4. Test circuit and switching waveforms - Continued.

READ CYCLE 1



NOTES: 1. $\overline{R/W}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW.

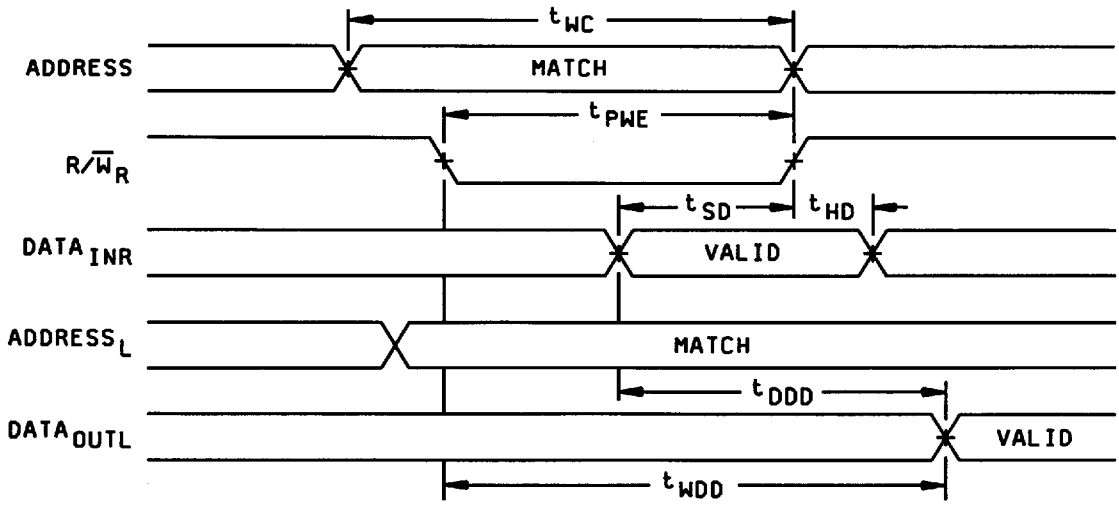
READ CYCLE 2



NOTES: 1. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
2. $\overline{R/W}$ is HIGH for read cycle.

FIGURE 4. Test circuit and switching waveforms - Continued.

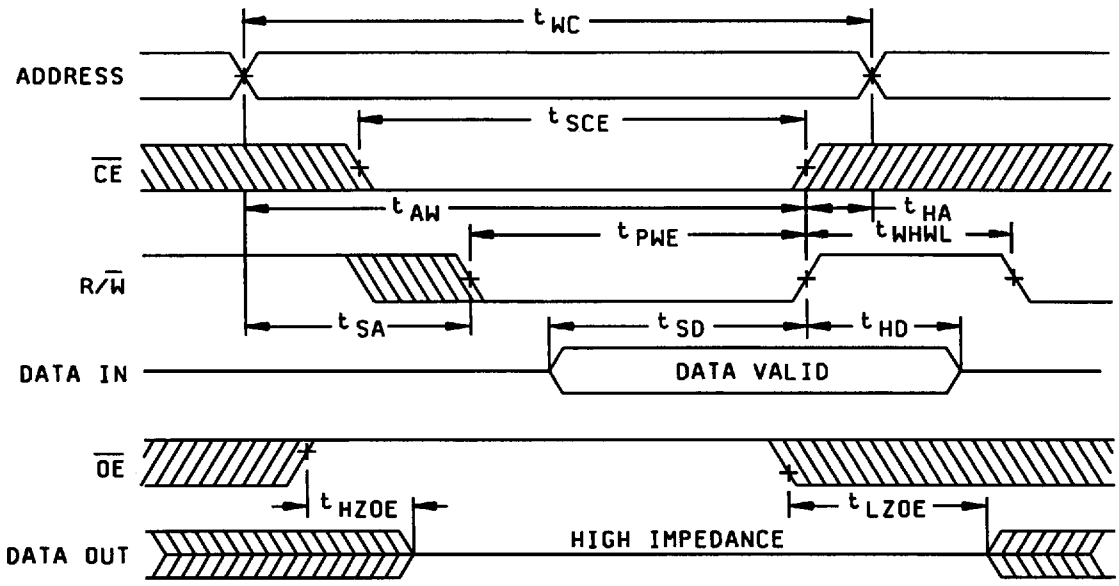
READ TIMING WITH PORT-TO-PORT DELAY



NOTES: 1. $\overline{BUSY}$ = HIGH for the writing port.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

FIGURE 4. Test circuit and switching waveforms - Continued.

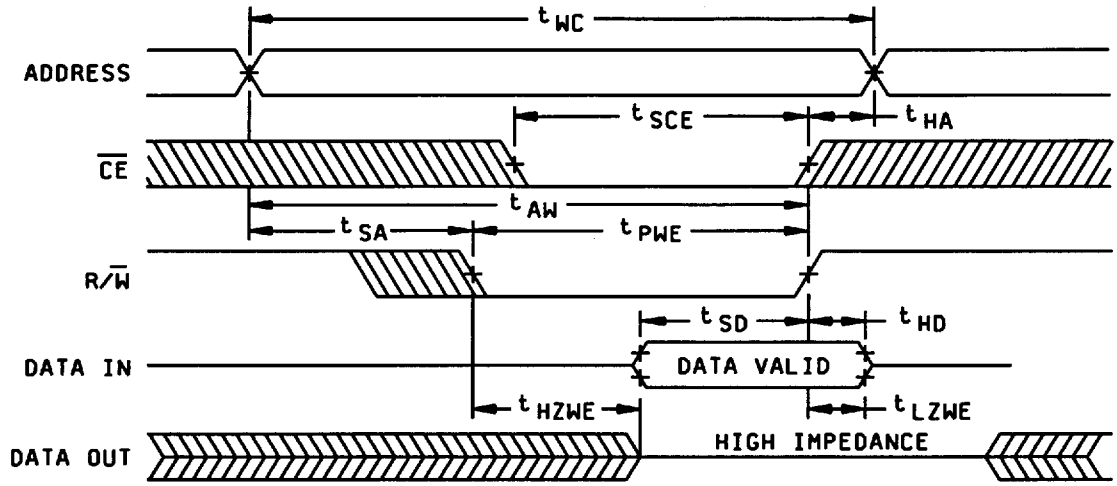
WRITE CYCLE: $\overline{OE}$ Three-States Data I/Os (Either Port)



NOTES: 1. The internal write time of memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
3. R/$\overline{W}$ must be HIGH during all address transactions.

FIGURE 4. Test circuit and switching waveforms - Continued.

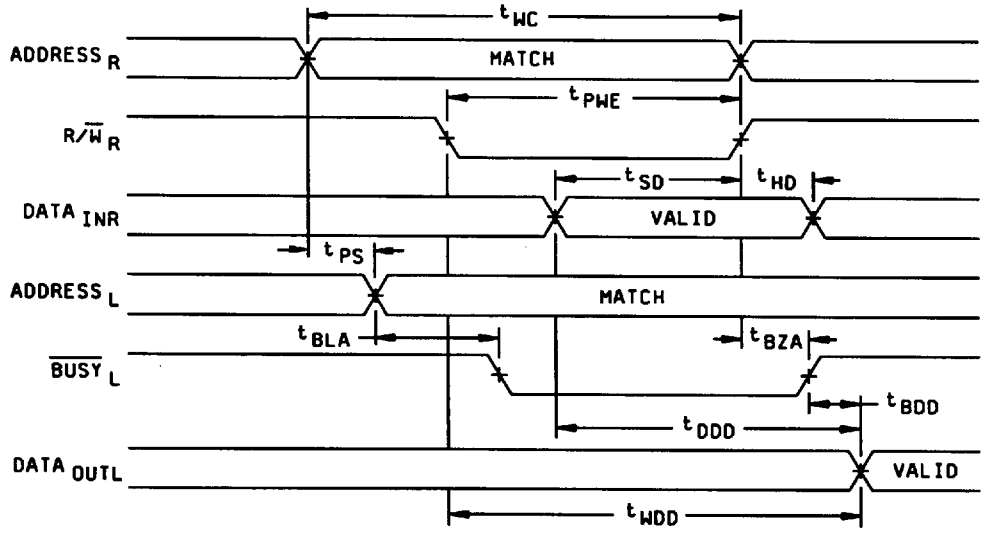
WRITE CYCLE 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)



NOTES: 1. The internal write time of memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW, Both signals must be LOW to initialize a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. R/$\overline{W}$ must be HIGH during all address transactions.
3. Data I/O pins enter high impedance even if $\overline{OE}$ is held LOW during write.

FIGURE 4. Test circuit and switching waveforms - Continued.

READ TIMING WITH $\overline{BUSY}$ ($M/\overline{S}$ = HIGH)



NOTE: 1. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

FIGURE 4. Test circuit and switching waveforms - Continued.

WRITE TIMING WITH $\overline{\text{BUSY}}$ ($\overline{\text{M/S}}$ = LOW)

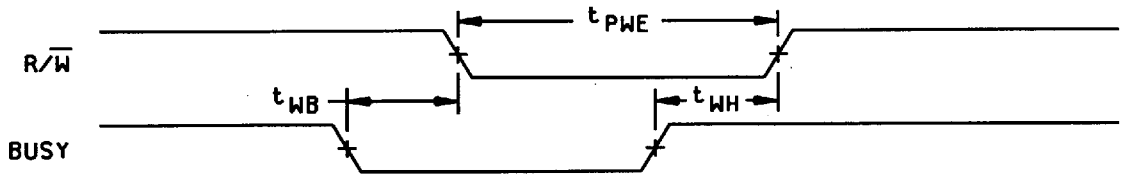
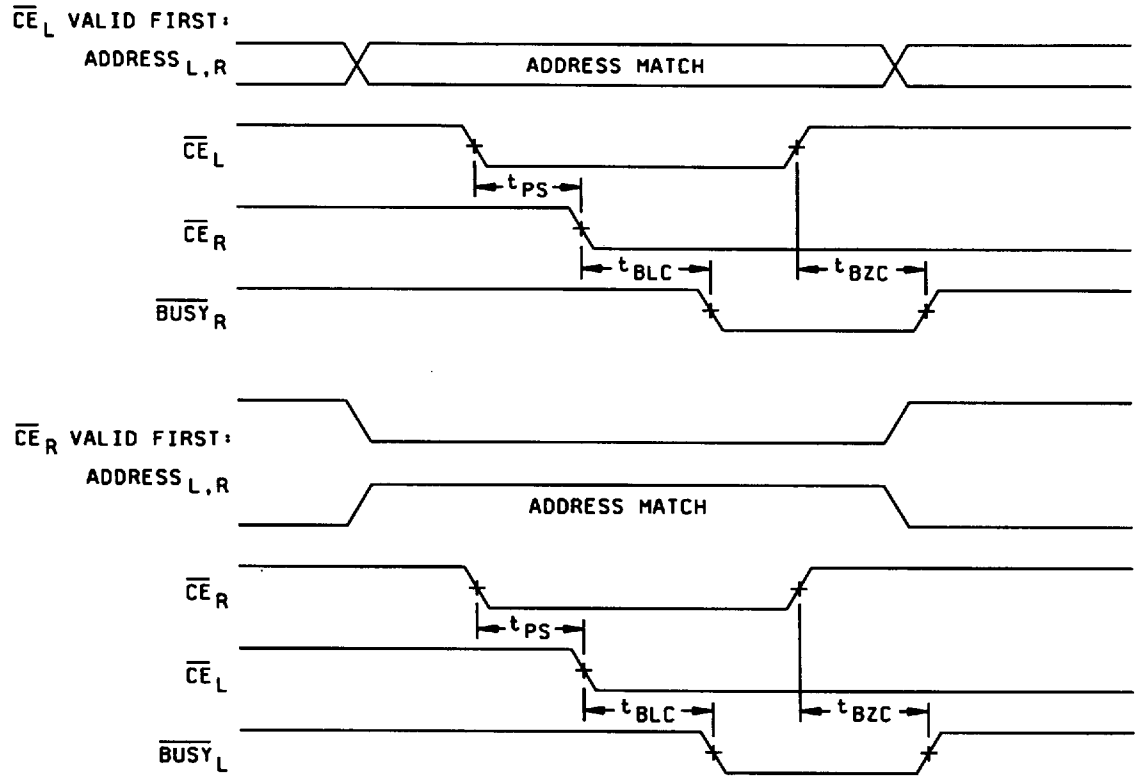


FIGURE 4. Test circuit and switching waveforms - Continued.

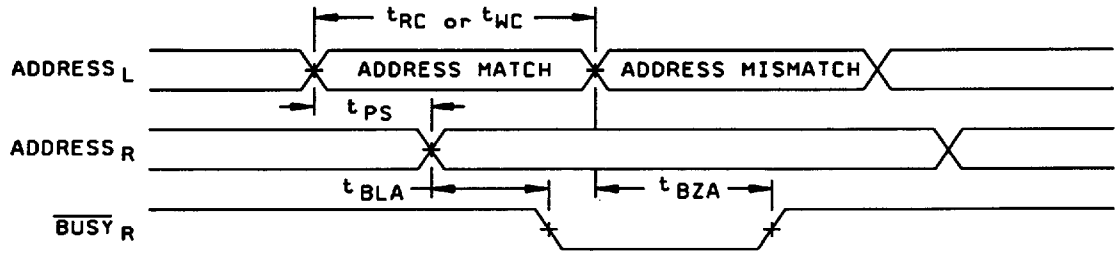
$\overline{\text{BUSY}}$ TIMING DIAGRAM NO. 1 ($\overline{\text{CE}}$ Arbitration)



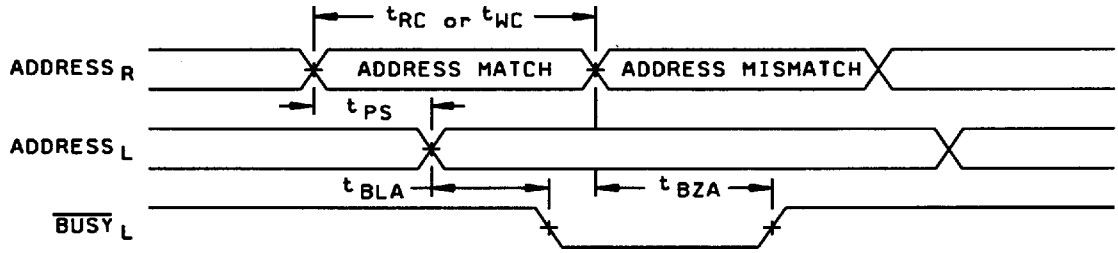
NOTE: If t_{PS} is violated, the $\overline{\text{BUSY}}$ signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{\text{BUSY}}$ will be asserted.

FIGURE 4. Test circuit and switching waveforms - Continued.

LEFT ADDRESS VALID FIRST:

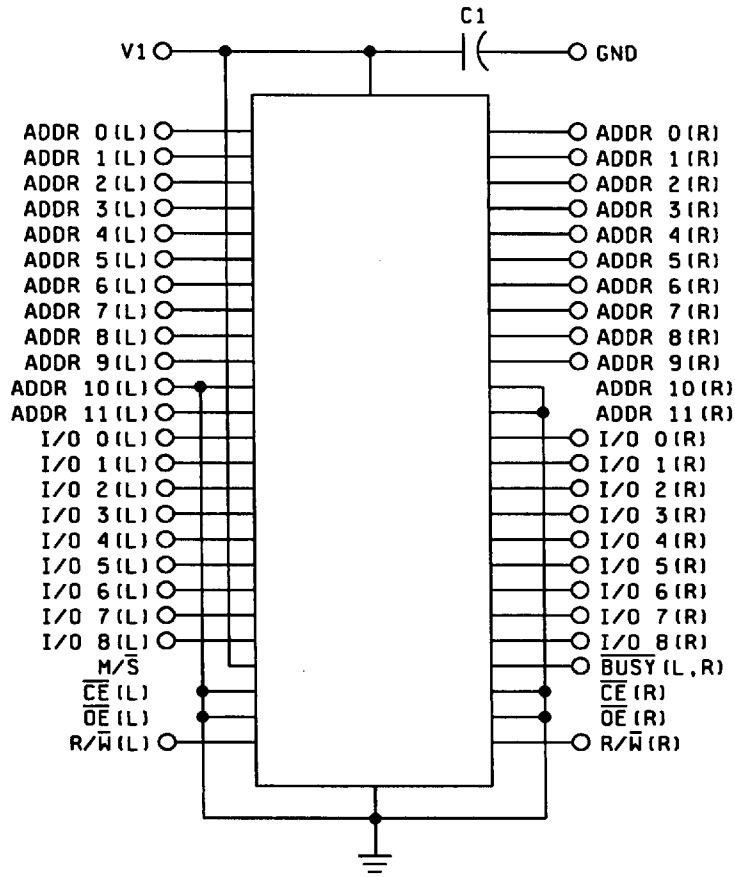


RIGHT ADDRESS VALID FIRST:



NOTE: If t_{PS} is violated, the $\overline{\text{BUSY}}$ signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{\text{BUSY}}$ will be asserted.

FIGURE 4. Test circuit and switching waveforms - Continued.



NOTES:
1. Power pin, V_{CC}, connected to V1.
2. Absolute voltage rating of paragraph 1.3 shall not be exceeded.
3. ESD handling precautions shall be followed.
4. The pattern in the memory array will be checkerboard for irradiation and accelerated aging tests.
5. Pin conditions during irradiation and accelerated aging tests:

$\overline{OE}$(L,R) = GNDI/O 0(L,R)
$\overline{CE}$(L,R) = GND
$\overline{BUSY}$(L,R) = NC
R/$\overline{W}$(L,R) = 250 kHz
M/S = V_{CC}
V1 = V_{CC} = 5.5 V
C1 = 0.1 µF ± 10%

I/O 0-8(L,R) = 125 kHz
ADDR 0(L,R) - ADDR 11(L,R):

ADDR 0 = 3.90 kHz	ADDR 6 = 31.3 kHz
ADDR 1 = 1.95 kHz	ADDR 7 = .488 kHz
ADDR 2 = .976 kHz	ADDR 8 = .244 kHz
ADDR 3 = 15.6 kHz	ADDR 9 = .122 kHz
ADDR 4 = 7.8 kHz	ADDR 10 = GND
ADDR 5 = 62.5 kHz	ADDR 11 = GND

FIGURE 5. Radiation exposure circuit.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters (see 4.2)	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements (see 4.4)	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters (see 4.4)	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ See 4.4.1d.
7/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device class V performance of delta limits shall be as specified in the manufacturer's QM plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging shall be performed on all devices requiring a RHA level greater than 5K rads(Si). The post-anneal end point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

Table IIB. Delta limits at +25°C.

Test 1/	All device types
I_{CC5}	±10μA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.4.2 Single event phenomena (SEP). SEP testing shall be required on class S and V devices. SEP testing shall be performed on the SEC or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be greater than 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and at the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latchup measurements.

g. For SEP test limits see table IB herein.

4.4.4.3 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

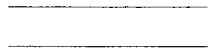
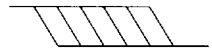
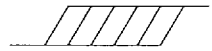
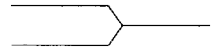
6.3 Record of users. Military and industrial users should inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for, each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.2.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.

Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.