REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes in table I. Editorial changes throughout.	1990 AUG 27	W. Heckman

REV																								
SHEET																								
REV					A	A			A															
SHEET	22	23	24	25	26	27	28	29	30															

REV STATUS OF SHEETS																							
	REV	A	A	A				A		A	A	A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Christopher A. Rauch

CHECKED BY: Charles Reusing

APPROVED BY: William K. Heckman

DRAWING APPROVAL DATE: 14 SEPTEMBER 1989

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, NMOS, 16-BIT MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89596

SHEET 1 OF 30

DESC FORM 193
SEP 87

• U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1773-2

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89596	01	Z	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Clock speed
01	8097BH	16-bit microcontroller	12 MHz

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Y	See figure 1 (68-lead, 1.870" x 1.870" x .106"), leaded chip carrier with unformed leads
Z	P-AC (68-pin, 1.180" x 1.180" x .345"), pin grid array

1.3 Absolute maximum ratings.

Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V_{SS} or ANGND (except $\overline{EA}$)	-0.3 V dc to +7.0 V dc
Voltage from $\overline{EA}$ to V_{SS} or ANGND	-0.3 V dc to +13.0 V dc
Power dissipation (P_D)	1.5 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Y	9°C/W 1/
Case Z	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C) 2/	-55°C to +125°C
Digital supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Analog supply voltage range (V_{REF})	4.5 V dc to 5.5 V dc
Power down supply voltage range (V_{PD})	4.5 V dc to 5.5 V dc
Oscillator frequency range (f_{OSC})	6 MHz to 12 MHz

1/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede that value herein.
2/ Case temperatures are instant on.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.3 Instruction set summary. The instruction set summary shall be as specified on figure 4.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ $V_{SS} = ANGND = 0\ V$ $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current	I_{CC}	All outputs disconnected 2/	1, 2, 3	All		275	mA
V_{PD} supply current	I_{PD}	Normal operation and power down 2/	1, 2, 3	All		1	mA
V_{REF} supply current	I_{REF}	2/	1, 2, 3	All		8	mA
Input low voltage (except $\overline{RESET}$)	V_{IL}		1, 2, 3	All	-0.3	0.8	V
Input low voltage, $\overline{RESET}$	V_{IL1}		1, 2, 3	All	-0.3	0.7	V
Input high voltage (except $\overline{RESET}$, NMI and XTAL1)	V_{IH}		1, 2, 3	All	2.0	V_{CC} +0.5	V
Input high voltage, $\overline{RESET}$ rising	V_{IH1}		1, 2, 3	All	2.4	V_{CC} +0.5	V
Input high voltage, $\overline{RESET}$ falling hysteresis	V_{IH2}		1, 2, 3	All	2.1	V_{CC} +0.5	V
Input high voltage, NMI, XTAL1	V_{IH3}		1, 2, 3	All	2.2	V_{CC} +0.5	V
Input leakage current to each pin of HSI, Port 3, Port 4 and P2.1	I_{LI}	$V_{IN} = 0$ to V_{CC} 2/	1, 2, 3	All		±10	µA
DC input leakage current to each pin of Port 0	I_{LI1}	$V_{IN} = 0$ to V_{CC} 2/	1, 2, 3	All		3	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ $V_{SS} = ANGND = 0\ V$ $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high current to EA	I_{IH}	$V_{IH} = 2.4\ V$ 2/	1, 2, 3	All		100	µA
Input low current to Port 1, and P2.6, P2.7	I_{IL}	$V_{IL} = 0.45\ V$ 2/	1, 2, 3	All		-125	µA
Input low current to RESET	I_{IL1}	$V_{IL} = 0.45\ V$ 2/	1, 2, 3	All	-0.25	-2	mA
Input low current, P2.2, P2.3, P2.4, READY, BUSWIDTH	I_{IL2}	$V_{IL} = 0.45\ V$ 2/	1, 2, 3	All		-50	µA
Output low voltage on quasi-bidirectional port pins and Port 3, Port 4 when used as ports	V_{OL}	$I_{OL} = 0.8\ mA$ 2/ 3/	1, 2, 3	All		0.45	V
Output low voltage on quasi-bidirectional port pins and Port 3, Port 4 when used as ports	V_{OL1}	$I_{OL} = 2.0\ mA$ 2/ 3/ 4/ 5/	1, 2, 3	All		0.75	V
Output low voltage on standard output pins, RESET and Bus/control pins	V_{OL2}	$I_{OL} = 2.0\ mA$ 2/ 3/ 4/ 5/ 6/	1, 2, 3	All		0.45	V
Output high voltage on quasi-bidirectional pins	V_{OH}	$I_{OH} = -20\ µA$ 2/ 3/	1, 2, 3	All	2.4		V
Output high voltage on standard output pins and Bus/control pins	V_{OH1}	$I_{OH} = -200\ µA$ 2/ 3/	1, 2, 3	All	2.4		V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ $V_{SS} = ANGND = 0\ V$ $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high current on $\overline{RESET}$	I_{OH3}	$V_{OH} = 2.4\ V$ 2/	1,2,3	All	-50		µA
Pin capacitance	C_S	f = 1.0 MHz See 4.3.1c 2/	4	All		10	pF
Functional tests		See 4.3.1d 2/	7,8	All			
READY hold after CLKOUT edge	t_{CLYX}	Timing requirements (system components must meet these specifications)	9,10,11	All	0		ns
End of ALE/$\overline{ADV}$ to READY valid	t_{LLYV}	See figure 5 f_{OSC} = 10 MHz	9,10,11	All		$2t_{OSC}$ -70	ns
End of ALE/$\overline{ADV}$ to READY high	t_{LLYH}		9,10,11	All	$2t_{OSC}$ +40	$4t_{OSC}$ -80	ns
Non-READY time	t_{YLYH}		9,10,11	All		1000	ns
Address valid to input data valid 7/	t_{AVDV}		9,10,11	All		$5t_{OSC}$ -120	ns
$\overline{RD}$ active to input data valid	t_{RLDV}		9,10,11	All		$3t_{OSC}$ -100	ns
Data hold after $\overline{RD}$ inactive	t_{RHDX}		9,10,11	All	0		ns
$\overline{RD}$ inactive to input data float	t_{RHDZ}		9,10,11	All	0	t_{OSC} -25	ns
Address valid to BUSWIDTH valid 7/	t_{AVGV}		9,10,11	All		$2t_{OSC}$ -125	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $V_{CC} = V_{PD} = 5\ V \pm 10\%$, $V_{SS} = ANGND = 0\ V$, $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
BUSWIDTH hold after ALE/$\overline{ADV}$ low	t_{LLGX}	Timing requirements (system components must meet these specifications)	9,10,11	All	t_{OSC} +40		ns
ALE/$\overline{ADV}$ low to BUSWIDTH valid	t_{LLGV}	See figure 5, f_{OSC} = 10 MHz	9,10,11	All		t_{OSC} -75	ns
Oscillator frequency	f_{OSC}	See figure 5	9,10,11	All	6.0	12.0	MHz
Oscillator period	t_{OSC}		9,10,11	All	83	166	ns
XTAL1 rising edge to clockout rising edge	t_{OHCH}	See figure 5, f_{OSC} = 10 MHz	9,10,11	All	0	120	ns
CLKOUT period 8/	t_{CHCH}		9,10,11	All	$3t_{OSC}$	$3t_{OSC}$	ns
CLKOUT high time	t_{CHCL}		9,10,11	All	$3t_{OSC}$ -35	$3t_{OSC}$ +10	ns
CLKOUT low to ALE high	t_{CLLH}		9,10,11	All	-30	-15	ns
ALE/$\overline{ADV}$ low to CLKOUT high	t_{LLCH}		9,10,11	All	t_{OSC} -25	t_{OSC} +45	ns
ALE/$\overline{ADV}$ high time 9/	t_{LHLL}		9,10,11	All	t_{OSC} -30 9/	t_{OSC} +35 9/	ns
Address setup to end of ALE/$\overline{ADV}$ 7/	t_{AVLL}		9,10,11	All	t_{OSC} -50		ns
$\overline{RD}$ or $\overline{WR}$ low to address float 10/	t_{RLAZ}		9,10,11	All		25	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = V_{PD} = 5\ V \pm 10\%$ $V_{SS} = ANGND = 0\ V$ $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
End of ALE/$\overline{ADV}$ to $\overline{RD}$ or $\overline{WR}$ active	t_{LLRL}	See figure 5 f_{OSC} = 10 MHz	9,10,11	All	t_{OSC} -40		ns
Address hold after end of ALE/$\overline{ADV}$ 10/	t_{LLAX}		9,10,11	All	t_{OSC} -40		ns
$\overline{WR}$ pulse width	t_{WLWH}		9,10,11	All	$3t_{OSC}$ -35		ns
Output data valid to end of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	t_{QVWH}		9,10,11	All	$3t_{OSC}$ -60		ns
Output data hold after $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$	t_{WHQX}		9,10,11	All	t_{OSC} -50		ns
End of $\overline{WR}$/$\overline{WRL}$/$\overline{WRH}$ to ALE/$\overline{ADV}$ high	t_{WHLH}		9,10,11	All	t_{OSC} -75		ns
$\overline{RD}$ pulse width	t_{RLRH}		9,10,11	All	$3t_{OSC}$ -30		ns
End of $\overline{RD}$ to ALE/$\overline{ADV}$ high	t_{RHLH}		9,10,11	All	t_{OSC} -45		ns
CLOCKOUT low to ALE/$\overline{ADV}$ low	t_{CLLL}		9,10,11	All	t_{OSC} -40	t_{OSC} +35	ns
$\overline{RD}$ high to INST, $\overline{BHE}$, AD8-15 inactive	t_{RHBX}		9,10,11	All	t_{OSC} -25	t_{OSC} +30	ns
$\overline{WR}$ high to INST, $\overline{BHE}$, AD8-15 inactive	t_{WHBX}		9,10,11	All	t_{OSC} -50	t_{OSC} +100	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55^{\circ}C \le T_C \le +125^{\circ}C$, $V_{CC} = V_{PD} = 5\ V \pm 10\%$, $V_{SS} = ANGND = 0\ V$, $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{WRL}$, $\overline{WRH}$ low to $\overline{WRL}$ $\overline{WRH}$ high	t_{HLHH}	See figure 5, f_{OSC} = 10 MHz	9,10,11	All	$2t_{OSC}$ -35	$2t_{OSC}$ +40	ns
ALE/$\overline{ADV}$ low to $\overline{WRL}$, $\overline{WRH}$ low	t_{LLHL}		9,10,11	All	$2t_{OSC}$ -30	$2t_{OSC}$ +55	ns
Output data valid to $\overline{WRL}$, $\overline{WRH}$ low	t_{QVHL}		9,10,11	All	t_{OSC} -60		ns
Serial port clock period	t_{XLXL}	Serial port shift register mode, see figure 5	9,10,11	All	$8t_{OSC}$		ns
Serial port clock falling edge to rising edge	t_{XLXH}		9,10,11	All	$4t_{OSC}$ -50	$4t_{OSC}$ +50	ns
Output data setup to clock rising edge	t_{QVXH}		9,10,11	All	$3t_{OSC}$		ns
Output data hold after clock rising edge	t_{XHQX}		9,10,11	All	$2t_{OSC}$ -70		ns
Next output data valid after clock rising edge	t_{XHQV}		9,10,11	All		$2t_{OSC}$ +50	ns
Input data setup to clock rising edge	t_{DVXH}		9,10,11	All	$2t_{OSC}$ +200		ns
Input data hold after clock rising edge	t_{XHDX}		9,10,11	All	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C < T_C < +125°C$ $V_{CC} = V_{PD} = 5$ V ±10% $V_{SS} = ANGND = 0$ V $f_{OSC} = 6.0$ to 12 MHz unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Last clock rising to output float	t_{XHQZ}	Serial port shift register mode, see figure 5	9,10,11	All		$5t_{OSC}$	ns
Oscillator frequency	$1/t_{OLOL}$	External clock drive See figure 5	9,10,11	All	6	12	MHz
High time	t_{OHOX}		9,10,11	All	25		ns
Low time	t_{OLOX}		9,10,11	All	30		ns
Rise time	t_{OLOH}		9,10,11	All		15	ns
Fall time	t_{OHOL}		9,10,11	All		15	ns
Resolution		See figure 5 $V_{REF} = 5$ V ±10%	9,10,11	All	1024 10	1024 10	level bits
Absolute error			9,10,11	All	0	±4	LSBS
Nonlineraity			9,10,11	All	0	±4	LSBS
Differential non-linearity			9,10,11	All	0	±2	LSBS
Channel to channel matching			9,10,11	All	0	±1	LSBS
Off isolation 11/ 12/ 13/		See figure 5	9,10,11	All	-60		dB

See footnotes on next page.

1/ Case temperatures are instant on.

2/ $V_{REF} = V_{EA} = 5$ V ±10%.

3/ Quasi-bidirectional pins include those on Port 1, for P2.6 and P2.7. Standard output pins include TXD, RXD (mode 0 only), PWM and HSO pins. Bus/control pins include CLKOUT, ALE, $\overline{BHE}$, $\overline{RD}$ $\overline{WR}$, INST, and AD0-15.

4/ Maximum current per pin must be externally limited to the following value if V_{OL} is held above 0.45 V:
I_{OL} on quasi-bidirectional pins and Ports 3 and 4 when used as ports: 4.0 mA.
I_{OL} on standard output pins and $\overline{RESET}$: 8.0 mA.
I_{OL} on Bus/control pins: 2.0 mA.

5/ During normal (nontransient) operation, the following limits apply:
Total I_{OL} on Port 1 must not exceed 8.0 mA.
Total I_{OL} on P2.0, P2.6, $\overline{RESET}$ and all HSO pins must not exceed 15 mA.
Total I_{OL} on Port 3 must not exceed 10 mA.
Total I_{OL} on P2.5, P2.7, and Port 4 must not exceed 20 mA.

6/ I_{OL} on HSO.X (X = 0, 4, 5) = 1.6 mA @ 0.5 V.

7/ The term "Address Valid" applies to AD0-15, $\overline{BHE}$, and INST.

8/ CLKOUT is directly generated as a divide-by-three of the oscillator. The period will be $3t_{OSC}$ ±10 ns if t_{OSC} is constant and the rise and fall times on XTAL1 are less than 10 ns.

9/ Maximum specification applies only to ALE. Minimum specification applies to both ALE and $\overline{ADV}$.

10/ The term "Address" in this definition applies to AD0-7 for 8-bit cycles, and AD0-15 for 16-bit cycles.

11/ These values are not tested in production and are based on theoretical estimates and laboratory tests.

12/ DC to 100 kHz.

13/ Multiplexer break-before-make guaranteed.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

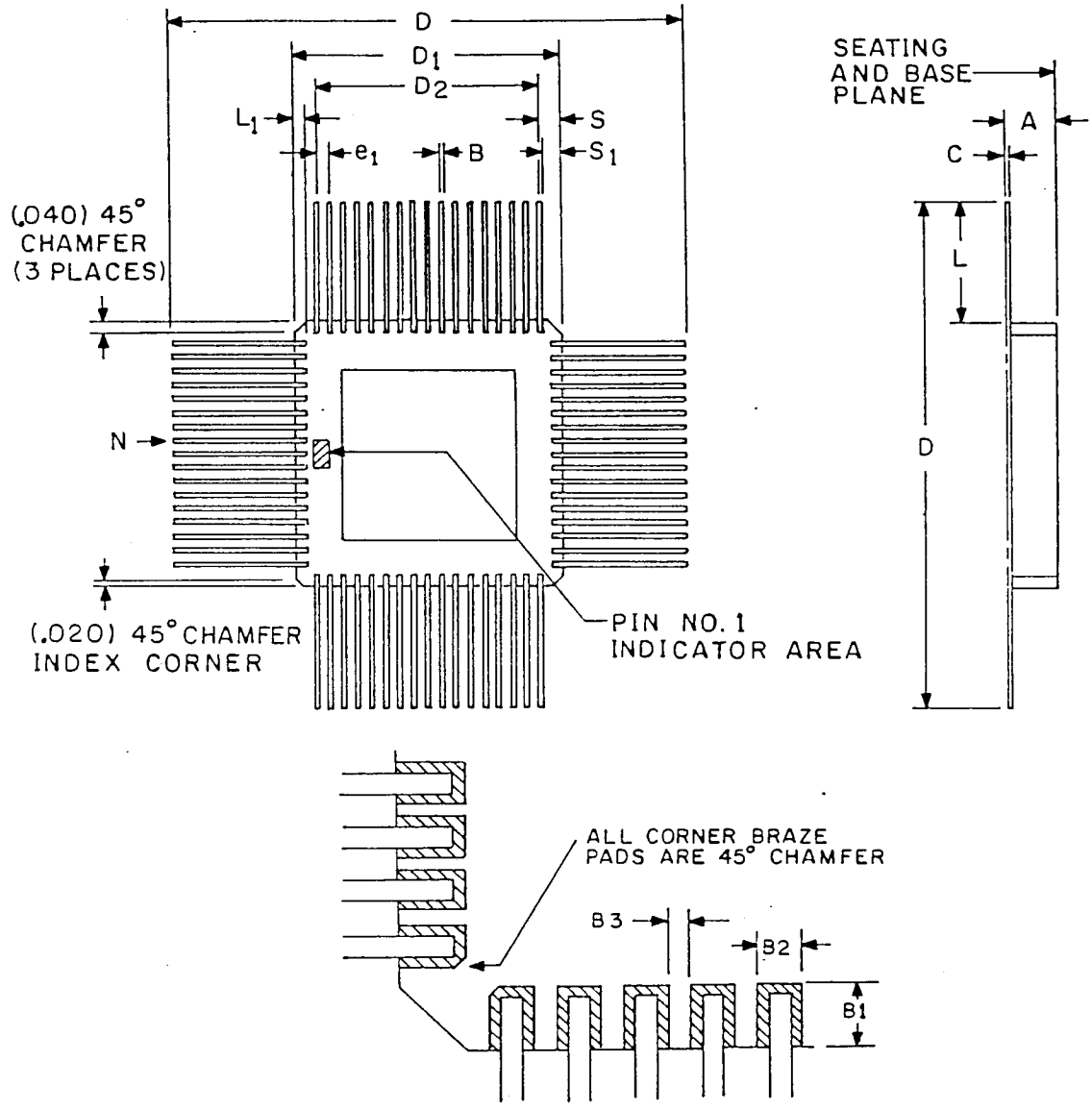

FIGURE 1. Case outline Y.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89596
		REVISION LEVEL	SHEET 12

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Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.80	.106	2.03	2.69
B	.016	.020	0.41	0.51
B_1 (see note)	.040	.060	1.02	1.52
B_2 (see note)	.030	.040	0.76	1.02
B_3 (see note)	.005	.020	0.13	0.51
C	.008	.012	0.20	0.31
D	1.640	1.870	41.66	47.50
D_1	.935	.970	23.75	24.64
D_2	.800 BSC		20.32 BSC	
e_1	.050 BSC		1.27 BSC	
L	.375	.450	9.52	11.43
L_1	.040	.060	1.02	1.52
N	68		68	
S	.066	.087	1.68	2.21
S_1	.050	---	1.27	---

NOTE: These are typical values.

FIGURE 1. Case outline Y - Continued.

Case Y

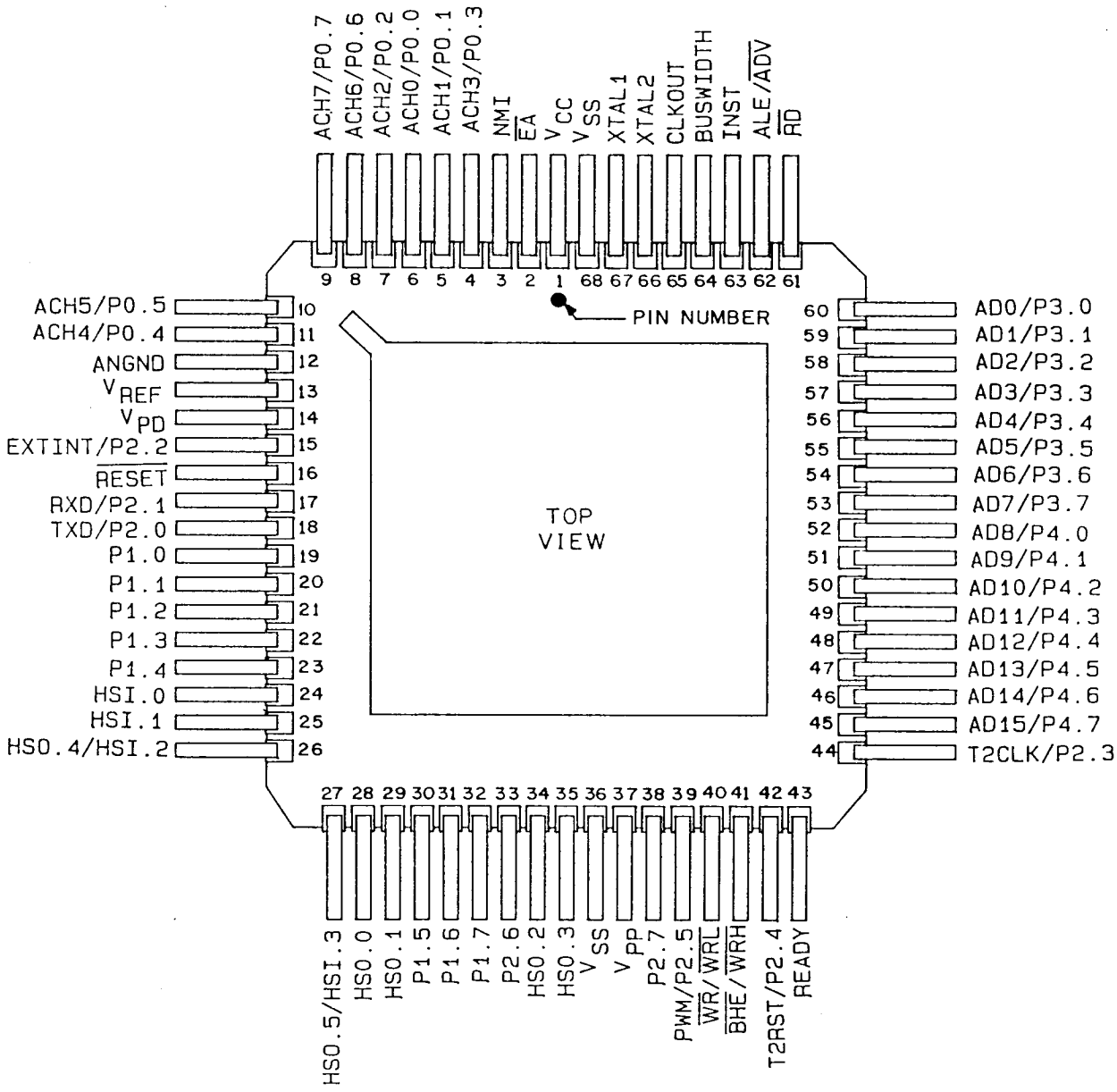


FIGURE 2. Terminal connections.

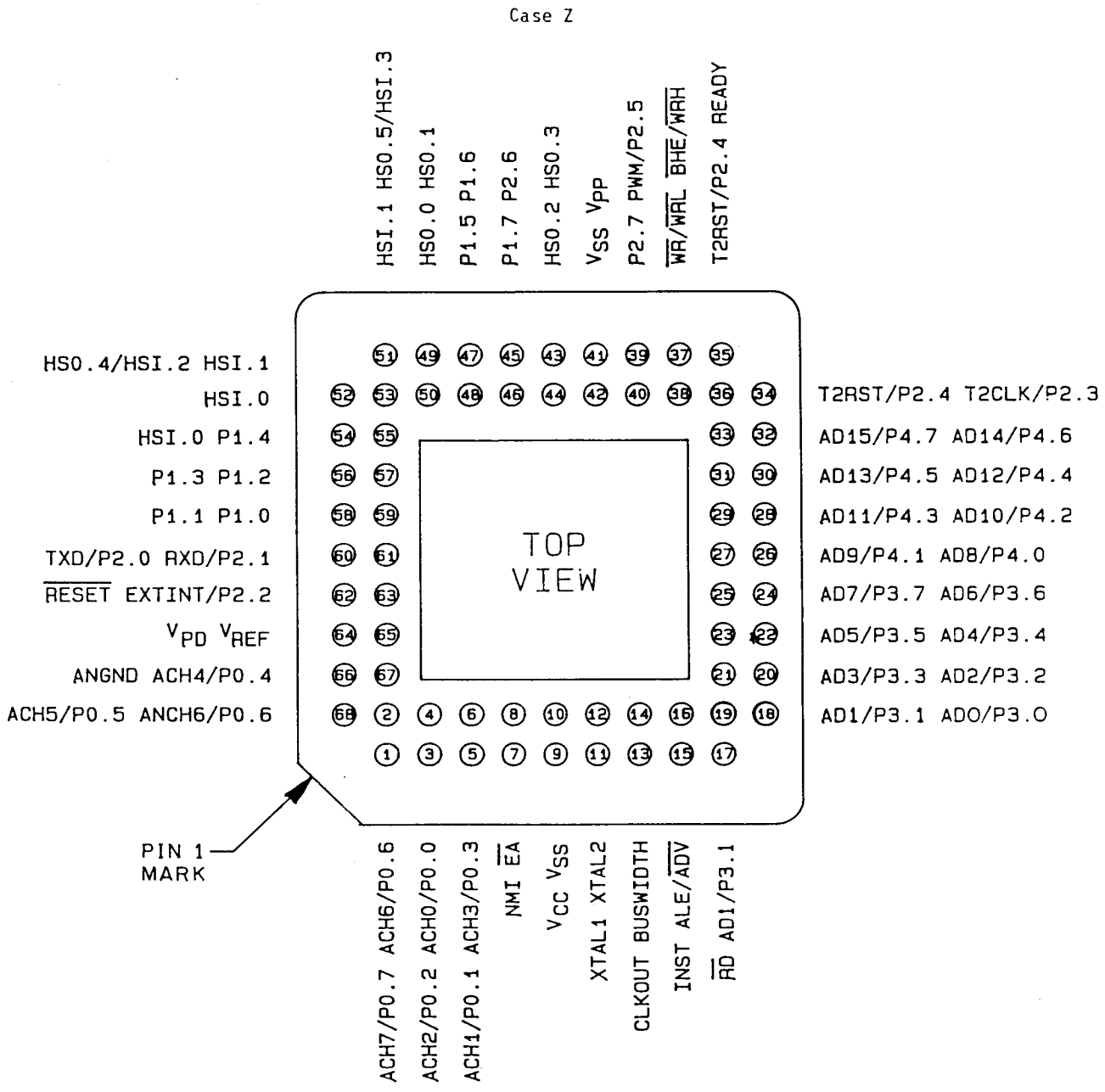


FIGURE 2. Terminal connections - Continued.

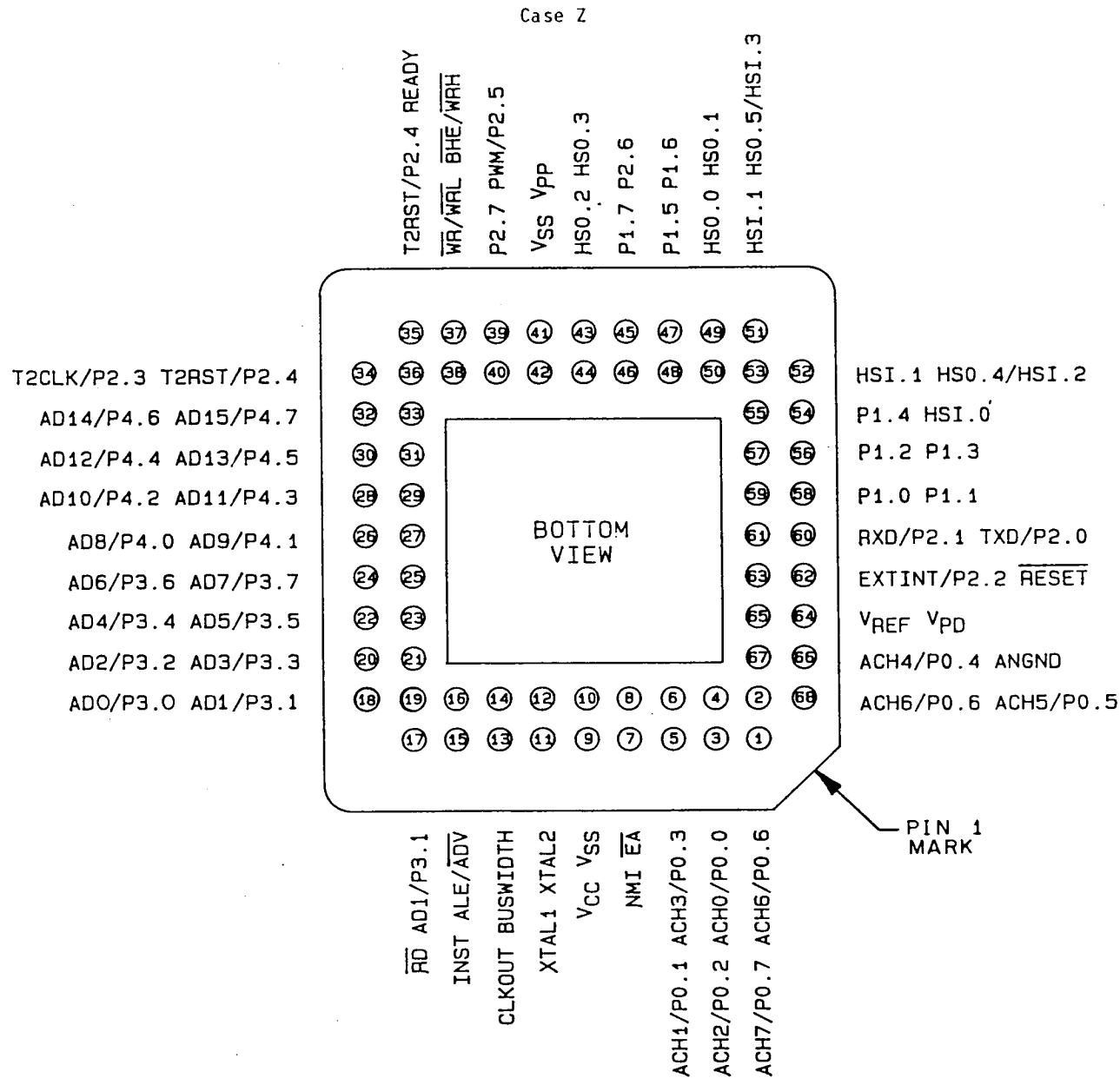


FIGURE 2. Terminal connections - Continued.

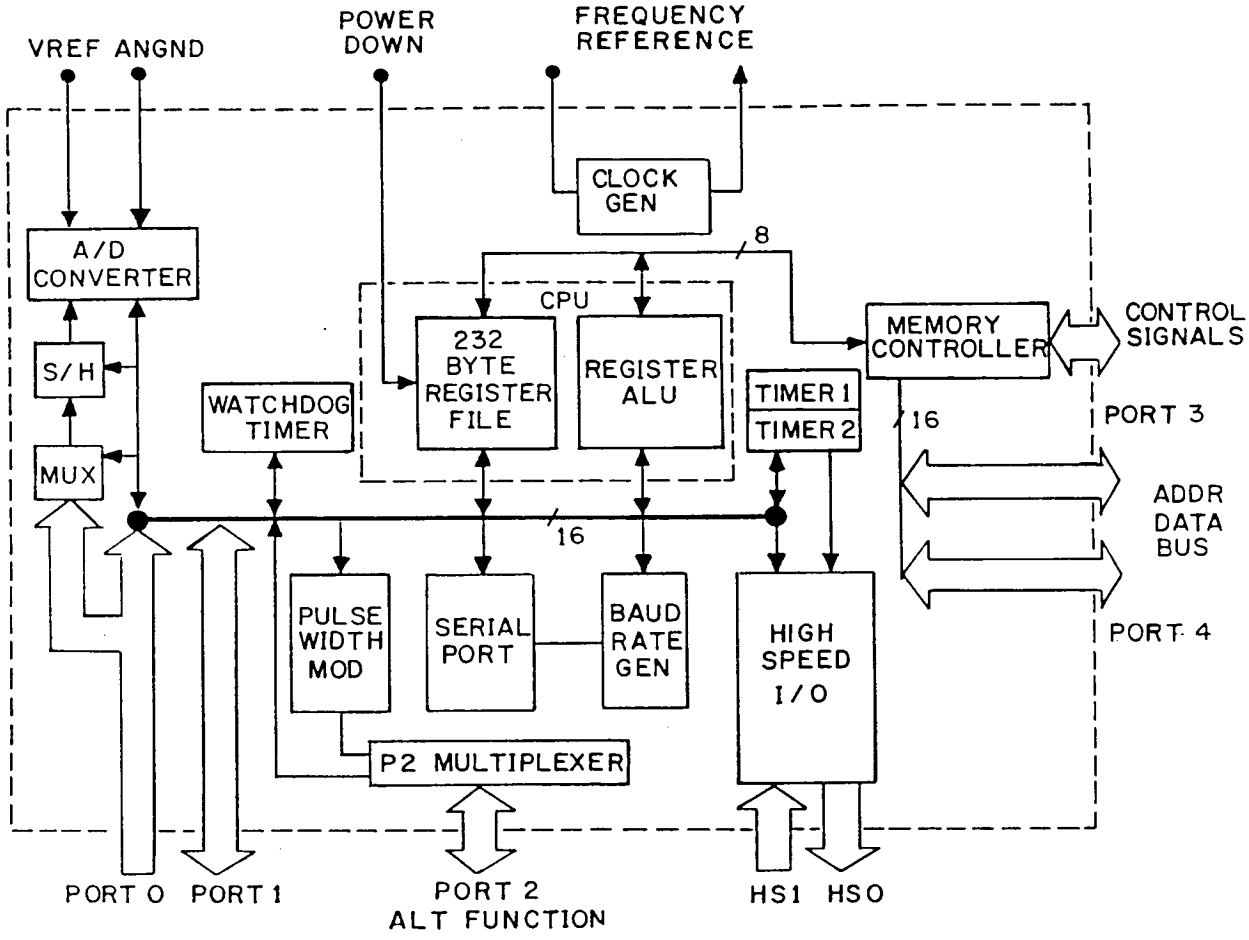


FIGURE 3. Functional block diagram.

Mnemonic	Oper-ands	Operation (note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
ADD/ADDB	2	D ← D + A	✓	✓	✓	✓	↑	---	
ADD/ADDB	3	D ← B + A	✓	✓	✓	✓	↑	---	
ADDC/ADDCB	2	D ← D + A + C	↓	✓	✓	✓	↑	---	
SUB/SUBB	2	D ← D - A	✓	✓	✓	✓	↑	---	
SUB/SUBB	3	D ← B - A	✓	✓	✓	✓	↑	---	
SUBC/SUBCB	2	D ← D - A + C - 1	↓	✓	✓	✓	↑	---	
CMP/CMPB	2	D - A	✓	✓	✓	✓	↑	---	
MUL/MULU	2	D, D + 2 ← D*A	---	---	---	---	---	?	2
MUL/MULU	3	D, D + 2 ← B*A	---	---	---	---	---	?	2
MULB/MULUB	2	D, D + 1 ← D*A	---	---	---	---	---	?	3
MULB/MULUB	3	D, D + 1 ← B*A	---	---	---	---	---	?	3
DIVU	2	D ← (D, D + 2)/A, D + 2 ← remainder	---	---	---	✓	↑	---	2
DIVUB	2	D ← (D, D + 1)/A, D + 1 ← remainder	---	---	---	✓	↑	---	3
DIV	2	D ← (D, D + 2)/A, D + 2 ← remainder	---	---	---	?	↑	---	
DIVB	2	D ← (D, D + 1)/A, D + 1 ← remainder	---	---	---	?	↑	---	
AND/ANDB	2	D ← D and A	✓	✓	0	0	---	---	
AND/ANDB	3	D ← B and A	✓	✓	0	0	---	---	
OR/ORB	2	D ← D or A	✓	✓	0	0	---	---	
XOR/XORB	2	D ← D (excl. or) A	✓	✓	0	0	---	---	
LD/LDB	2	D ← A	---	---	---	---	---	---	
ST/STB	2	A ← D	---	---	---	---	---	---	
LDBSE	2	D ← A; D + 1 ← Sign(A)	---	---	---	---	---	---	3,4
LDBZE	2	D ← A; D + 1 ← 0	---	---	---	---	---	---	3,4

FIGURE 4. Instruction set summary.

Mnemonic	Operands	Operation (note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
PUSH	1	SP ← SP - 2; (SP) ← A	---	---	---	---	---	---	
POP	1	A ← (SP); SP ← SP + 2	---	---	---	---	---	---	
PUSHF	0	SP ← SP - 2; (SP) ← PSW; PSW ← 0000H I ← 0	0	0	0	0	0	0	
POPF	0	PSW ← (SP); SP ← SP + 2; I ← ✓	✓	✓	✓	✓	✓	✓	
SJMP	1	PC ← PC + 11-bit offset	---	---	---	---	---	---	5
LJMP	1	PC ← PC + 16-bit offset	---	---	---	---	---	---	5
BR (indirect)	1	PC ← (A)	---	---	---	---	---	---	
SCALL	1	SP ← SP - 2; (SP) ← PC; PC ← PC + 11-bit offset	---	---	---	---	---	---	5
LCALL	1	SP ← SP - 2; (SP) ← PC; PC ← PC + 16-bit offset	---	---	---	---	---	---	5
RET	0	PC ← (SP); SP ← SP + 2	---	---	---	---	---	---	
J (conditional)	1	PC ← PC + 8-bit offset (if taken)	---	---	---	---	---	---	5
JC	1	Jump if C = 1	---	---	---	---	---	---	5
JNC	1	Jump if C = 0	---	---	---	---	---	---	5
JE	1	Jump if Z = 1	---	---	---	---	---	---	5
JNE	1	Jump if Z = 0	---	---	---	---	---	---	5
JGE	1	Jump if N = 0	---	---	---	---	---	---	5
JLT	1	Jump if N = 1	---	---	---	---	---	---	5
JGT	1	Jump if N = 0 and Z = 0	---	---	---	---	---	---	5
JLE	1	Jump if N = 1 or Z = 1	---	---	---	---	---	---	5
JH	1	Jump if C = 1 and Z = 0	---	---	---	---	---	---	5
JNH	1	Jump if C = 0 or Z = 1	---	---	---	---	---	---	5
JV	1	Jump if V = 1	---	---	---	---	---	---	5

FIGURE 4. Instruction set summary - Continued.

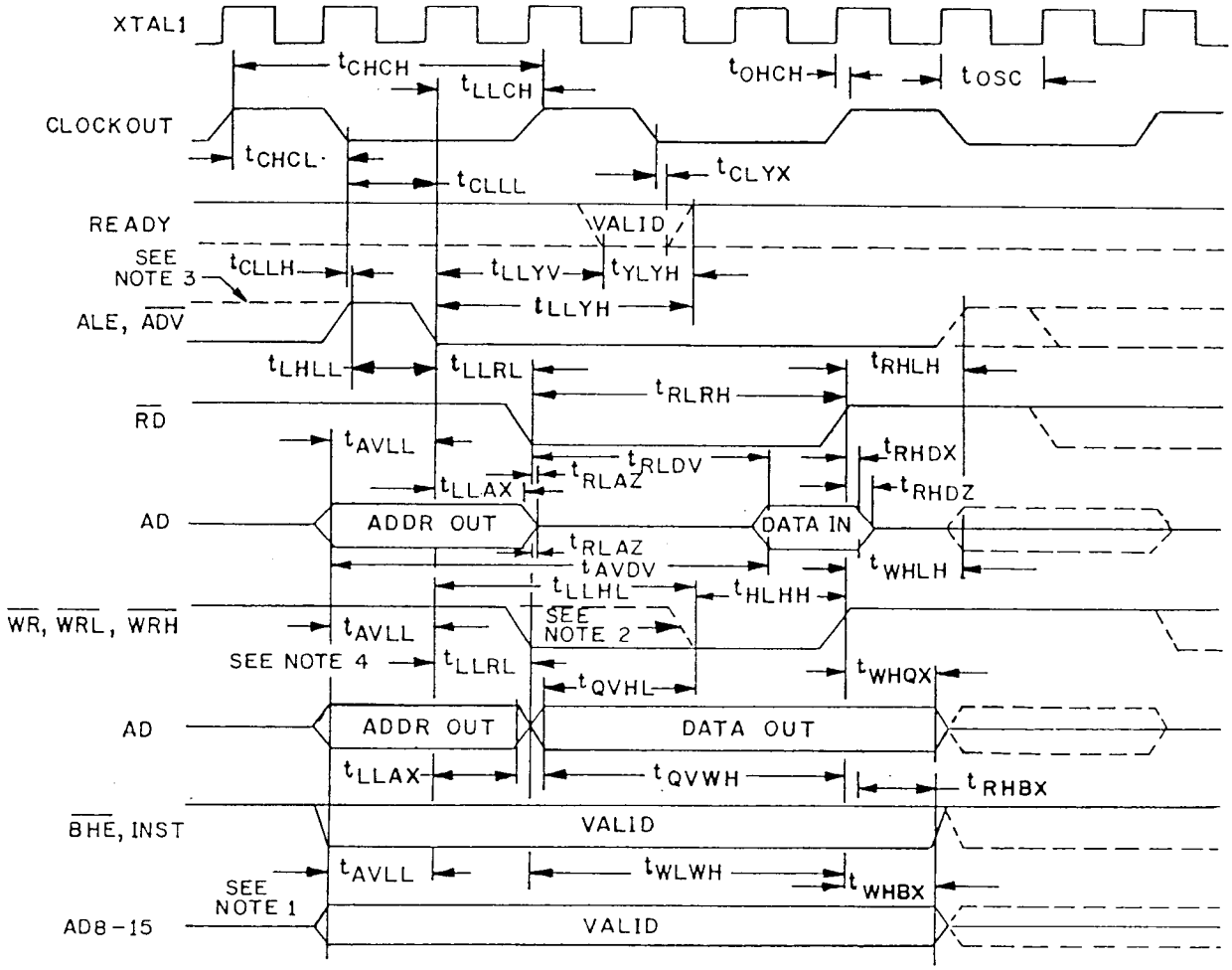
Mnemonic	Oper-ands	Operation (note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
JNV	1	Jump if V = 0	---	---	---	---	---	---	5
JVT	1	Jump if VT = 1; Clear VT	---	---	---	---	0	---	5
JNVT	1	Jump if VT = 0; Clear VT	---	---	---	---	0	---	5
JST	1	Jump if ST = 1	---	---	---	---	---	---	5
JNST	1	Jump if ST = 0	---	---	---	---	---	---	5
JBS	3	Jump if specified bit = 1	---	---	---	---	---	---	5,6
JBC	3	Jump if specified bit = 0	---	---	---	---	---	---	5,6
DJNZ	1	D ← D - 1; if D≠ 0 then PC ← PD + 8-bit offset	---	---	---	---	---	---	5
DEC/DECB	1	D ← D - 1	✓	✓	✓	✓	↑	---	
NEG/NEGB	1	D ← 0 - D	✓	✓	✓	✓	↑	---	
INC/INCB	1	D ← D + 1	✓	✓	✓	✓	↑	---	
EXT	1	D ← D; D + 2 ← Sign (D)	✓	✓	0	0	---	---	2
EXTB	1	D ← D; D + 1 ← Sign (D)	✓	✓	0	0	---	---	3
NOT/NOTB	1	D ← Logical not (D)	✓	✓	0	0	---	---	
CLR/CLRB	1	D ← 0	1	0	0	0	---	---	
SHL/SHLB/SHLL	2	C ← msb ----- lsb ← 0	✓	?	✓	✓	↑	---	7
SHR/SHRB/SHRL	2	0 → msb ---- lsb → C	✓	?	✓	0	---	✓	7
SHRA/SHRAB/SHRAL	2	msb → msb ----- lsb → C	✓	✓	✓	0	---	✓	7
SETC	0	C ← 1	---	---	1	---	---	---	
CLRC	0	C ← 0	---	---	0	---	---	---	
CLRVT	0	VT ← 0	---	---	---	---	0	---	
RST	0	PC ← 2080H	0	0	0	0	0	0	8
DI	0	Disable all interrupts (I ← 0)	---	---	---	---	---	---	
EI	0	Enable all interrupts (I ← 1)	---	---	---	---	---	---	

FIGURE 4. Instruction set summary - Continued.

Mnemonic	Oper-ands	Operation (note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
NOP	0	PC ← PC + 1	---	---	---	---	---	---	
SKIP	0	PC ← PC + 2	---	---	---	---	---	---	
NORML	2	Left shift til msb = 1; D ← shift count	✓	?	0	---	---	---	7
TRAP	0	SP ← SP - 2; (SP) ← PC PC ← (2010H)	---	---	---	---	---	---	9

NOTES:
1. If the mnemonic ends in "B", a byte operation is performed, otherwise a word operation is done. Operands D, B, and A must conform to the alignment rules for the required operand type. D and B are locations in the register file; A can be located anywhere in memory.
2. D, D + 2 are consecutive WORDS in memory; D is DOUBLE-WORD aligned.
3. D, D + 1 are consecutive BYTES in memory; D is WORD aligned.
4. Changes a byte to a word.
5. Offset is a 2's complement number.
6. Specified bit is one of the 2048 bits in the register file.
7. The "L" (long) suffix indicates double-word operation.
8. Initiates a reset by pulling $\overline{\text{RESET}}$ low. Software should reinitialize all the necessary registers with code starting at 2080H.
9. The assembler will not accept this mnemonic.

FIGURE 4. Instruction set summary - Continued.



NOTES:
1. 8-bit bus only.
2. 8-bit bus; or when write strobe mode selected.
3. When $\overline{ADV}$ selected.
4. 8 or 16-bit bus and write strobe mode not selected.

FIGURE 5. Switching test circuit and waveforms.

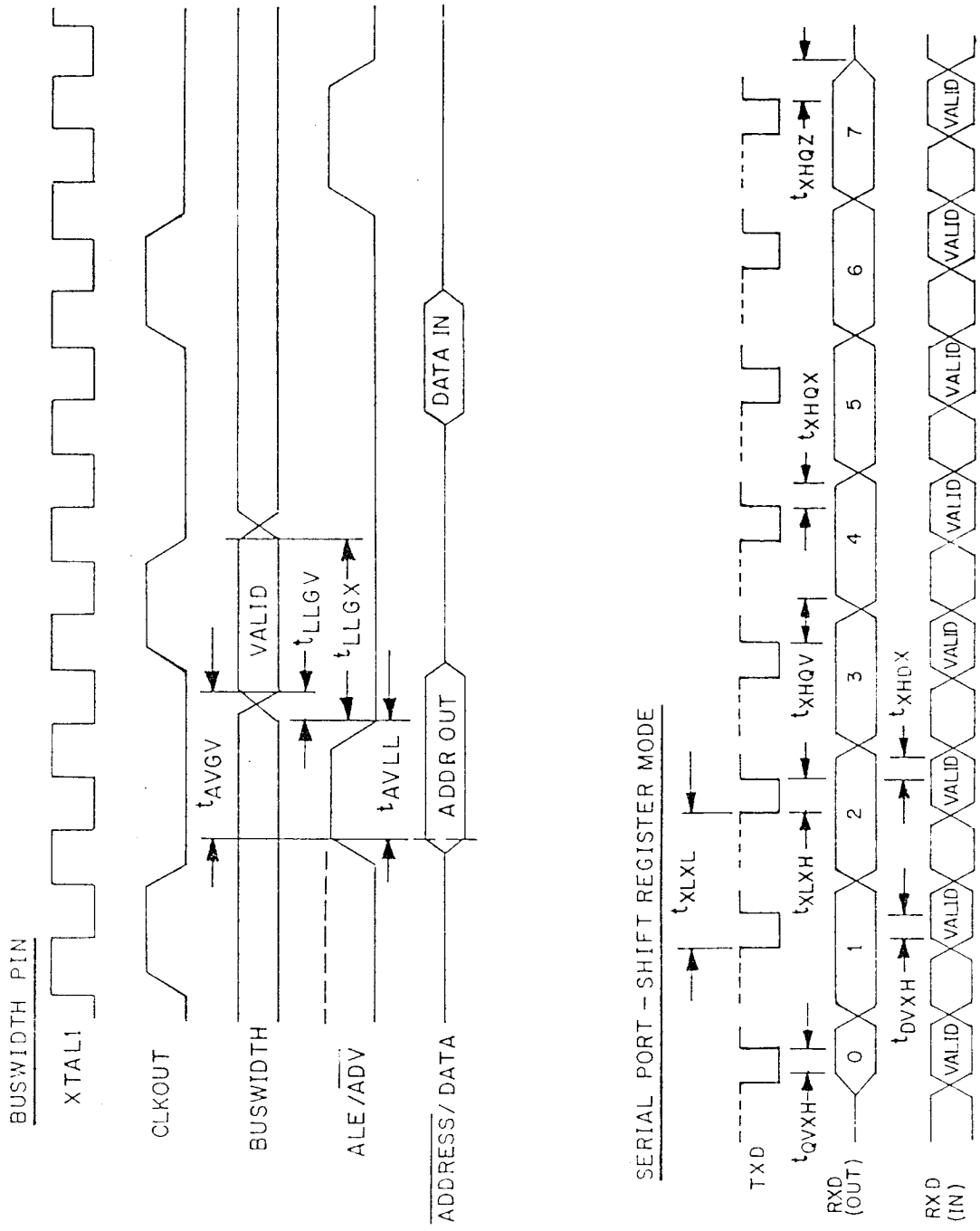


FIGURE 5. Switching test circuit and waveforms - Continued.

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		REVISION LEVEL	SHEET 23

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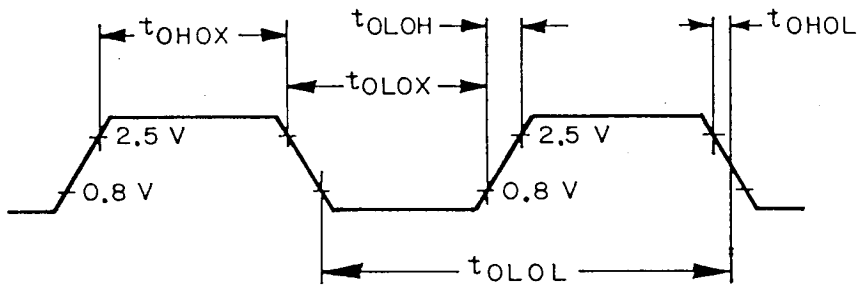
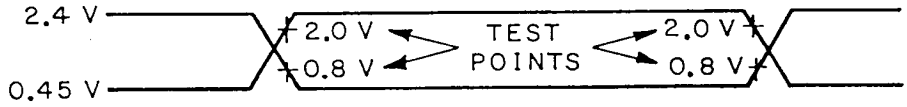
External clock drive waveforms

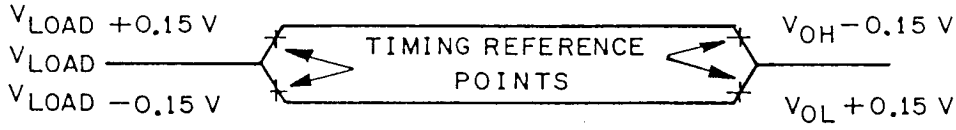


AC testing input, output waveform



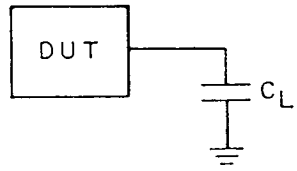
AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

Float waveform



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs $I_{OL}/I_{OH} \geq \pm 15$ mA.

Output load circuit



C_L = 80 pF unless otherwise specified.

FIGURE 5. Switching waveforms and test circuit - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_S measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. Subgroups 7 and 8 functional testing shall verify the instruction set (see figure 4).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,8A,10

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Pin descriptions.

Symbol	Name and function
V_{CC}	Main supply voltage (5 V).
V_{SS}	Digital circuit ground (0 V). There are two V_{SS} pins, both of which must be connected.
V_{PD}	RAM standby supply voltage (5 V). This voltage must be present during normal operation. In a power down condition (i.e, V_{CC} drops to zero), if $\overline{RESET}$ is activated before V_{CC} drops below specification and V_{PD} continues to be held with specification, the top 16 bytes in the register file will retain their contents. $\overline{RESET}$ must be held low during the power down and should not be brought high until V_{CC} is within specification and the oscillator has stabilized.
V_{REF}	Reference voltage to the A/D converter (5 V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
V_{PP}	Used as the programming voltage for EPROM parts only. This pin has no function for the 8097BH device.
XTAL1	Input of the oscillator inverter and of the terminal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is one-third the oscillator frequency. It has a 33 percent duty cycle.
$\overline{RESET}$	Reset input to the chip, input low for at least two state times to reset the chip. The subsequent low-to-high transition resynchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. $\overline{RESET}$ has an internal pullup.

Symbol	Name and function
BUSWIDTH	Input for bus width selection. If CCR bit one is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a zero an 8-bit cycle occurs. If CCR bit one is a zero, the bus is always an 8-bit bus. If this pin is left unconnected, it will rise to V_{CC}.
NMI	A postive transition causes a vector to external memory location 0000H. External memory from 00H through 0FFH is reserved for development systems.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle.
$\overline{EA}$	Input for memory select (external access). $\overline{EA}$ is tied to a TTL-low causing accesses to locations 2000H through 3FFFH to be directed to off-chip memory.
ALE/$\overline{ADV}$	Address latch enable or Address valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus cycle. $\overline{ADV}$ can be used as a chip select for external memory. ALE/$\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}$/$\overline{WRL}$	Write and Write low output to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is activated only during external memory writes.
$\overline{BHE}$/$\overline{WRH}$	Bus high enable or Write high output to external memory, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{BHE}$ = 1), to the high byte only (A0 = 1, $\overline{BHE}$ = 0), or both bytes (A0 = 0, $\overline{BHE}$ = 0). If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}$/$\overline{WRH}$ is activated only during external memory writes.

Symbol	Name and function
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. The bus cycle can be lengthened by up to 1 µs. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready, is available through configuration of CCR. READY has a weak internal pullup, so it goes to one unless externally pulled low.
HSI	Inputs to high speed input unit. Four HSI pins are available: HS1.0, HS1.1, HS1.2, and HS1.3. Two of them (HS1.2 and HS1.3) are shared with the HSO unit.
HSO	Outputs from high speed output unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4, and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI unit.
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multifunctional port. Six of its pins are shared with other functions, the remaining two are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.

6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8959601YX	34649	MQ8097BH
5962-8959601ZX	34649	MG8097BH

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 W. Williams Field Road Chandler, AZ 85224