DATA SHEET

凌陽科技
SUNPLUS

SPOD80A

80-Channels Dot Matrix Column/Row OLED Driver

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Version 1.0

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Table of Contents

PAGE

80-CHANNELS DOT MATRIX COLUMN/ROW OLED DRIVER

1. GENERAL DESCRIPTION

The SPOD80A, an 80-channels dot matrix column/row OLED driver, is fabricated by low power CMOS technology. By incorporating an 80-bit shift register, an 80-bit data latch, and an 80-bit driver, the SPOD80A can drive constant current/voltage to 80 column/row lines simultaneously according to the selection mode and input data.

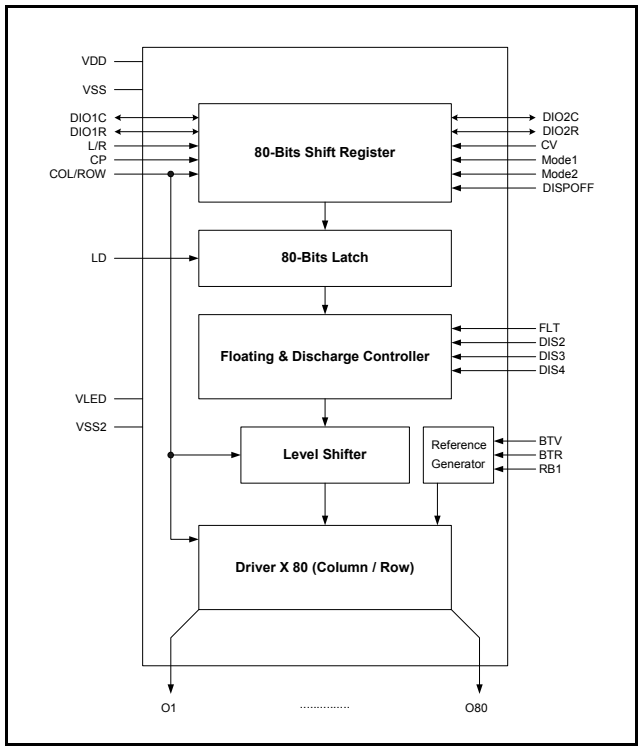
2. FEATURES

- Shift Clock frequency: 5.0MHz (Max.) (VDD = 2.4V - 5.5V)
- Serial data input
- Current/Voltage driving modes are selectable with CV pin (for column driver only)
- Supply voltage for OLED driver: 9.0V - 16V
- Internal discharge circuit
- Cascade function
- Built-in display off function
- 12 types of driving configurations

3. PACKAGE

- Bare chip

4. BLOCK DIAGRAM



5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
O17 - O1 O40 - O18 O63 - O61 O80 - O64	1 - 17 80 -102 55 - 77 32 - 48	O	Column/Row output
CP	24	I	Data shift clock. The data is shifted to 80 bits shift register at the falling edge of 'CP' when used as column driver.
LD	23	I	Data load pulse. When used as a column driver, a row of display data is latched at the falling edge of 'LD'. When used as a row driver, 'LD' is the shift clock input.
DIO1C DIO2C DIO1R DIO2R	25 19 26 20	I/O	Series data input/output of column/row driver. 1). When 'L/R' = 1, 'DIO1C' and 'DIO1R' are series data inputs of column driver and row driver respectively. 'DIO2C' and 'DIO2R' are series data outputs of column driver and row driver respectively. 2). When 'L/R' = 0, 'DIO2C' and 'DIO2R' are series data inputs of column driver and row driver respectively. 'DIO1C' and 'DIO1R' are series data outputs of column driver and row driver respectively. 3). When 'MODE1'⊕'Mode2' = 0, 'COL/ROW' = 1, SPOD80A is used as dedicated column driver, series data input of row driver, 'DIO1R' or 'DIO2R' depending on 'L/R', should be connected to VSS or float. 4). When 'MODE1'⊕'Mode2' = 0, 'COL/ROW' = 0, SPOD80A is used as dedicated row driver, series data input of column driver, 'DIO1C' or 'DIO2C' depending on 'L/R', should be connected to VSS or float.
COL/ROW	51	I	Column driver/Row driver selection
VDD	27	-	Power supply of digital circuit
VSS	18	-	GND of digital circuit
VLED	54 79 108	-	Power supply of OLED driving buffer
VSS2	49 78 103	-	GND of OLED driving buffer
L/R	50	I	Selection of data shift direction
MODE1 MODE2	53 52	I	Mode selection. There are 12 modes can be selected when combine 'MODE1', 'MODE2' with 'COL/ROW' and 'L/R'.
CV	22	I	Selection of driving method, default is 'H'. CV = 1, current driving mode CV = 0, voltage driving mode This mode selection is valid when used as column driver only.
BTV BTR	28 29	I I	Brightness control input. By adjusting an external voltage (VBT) and resistor (RBT), the output current in O[1:80] can be adjusted, see function description. This adjustment is valid when used as column driver and CV = 1 only.
RB1	31	-	Internal/external resistor selection. Connect this pin to ground while using internal resistor, or float it when using external resistor

Mnemonic	PIN No.	Type	Description
DIS2 DIS3 DIS4	106 105 104	I	Pulse width control of internal discharge By setting DIS2 - DIS4, the pulse width of internal discharge can be set to be 0, 2, 4, 6, 8, 10, 12, 14 TWCP. Where DIS4 is MSB; DIS2 is LSB. The default value of DIS4, 3, 2 is 010.
FLT	107	I	Output voltage control. While set to 'H', the driver will be float when input data is '0'. While set to 'L', the driver outputs deselect level (VSS2) when input data is '0'. This mode selection is valid only when used as column driver. The default value is 'H'.
DISPOFF	21	I	Control for output deselect level 1). While set to 'L', the driver outputs deselect level (VSS2). 2). While set to 'H', the driver outputs constant current/voltage depending on mode selection.
VBS	30	-	Bypass capacitor A 0.1μF capacitor connecting to VSS2 is necessary

6. FUNCTIONAL DESCRIPTIONS

6.1. 12 Types of Driving Configurations

COL/ROW	Mode1	Mode2	L/R	O[1:16]	O[17:32]	O[33:48]	O[49:64]	O[65:80]
1	0/1	0/1	1	COL	COL	COL	COL	COL
1	0/1	0/1	0	COL	COL	COL	COL	COL
1	0	1	1	COL	COL	COL	COL	ROW
1	0	1	0	ROW	COL	COL	COL	COL
1	1	0	1	COL	COL	COL	ROW	ROW
1	1	0	0	ROW	ROW	COL	COL	COL
0	1	0	1	COL	COL	ROW	ROW	ROW
0	1	0	0	ROW	ROW	ROW	COL	COL
0	0	1	1	COL	ROW	ROW	ROW	ROW
0	0	1	0	ROW	ROW	ROW	ROW	COL
0	0/1	0/1	1	ROW	ROW	ROW	ROW	ROW
0	0/1	0/1	0	ROW	ROW	ROW	ROW	ROW

Note: When 'Mode1'⊕'Mode2' = 0, SPOD80A is used as dedicated column driver or row driver.
When 'Mode1'⊕'Mode2' = 1, SPOD80A is used as column/row driver.

6.2. Current/Voltage Driving Mode

SPOD80A provides two kinds of driving methods, current driving and voltage driving. By setting CV = 'H', outputs programmed to be column driver will source a constant current when input data is 'H' ; and will be high impedance or deselect level (VSS2) when input data is 'L'.

By setting CV = 'L', outputs programmed to be column driver will output select level (VLED) when input data is 'H' ; and will be high impedance or deselect level (VSS2) when input data is 'L'.

6.3. Relationship between the Display Data and Driver Output PINs

6.3.1. Column driver

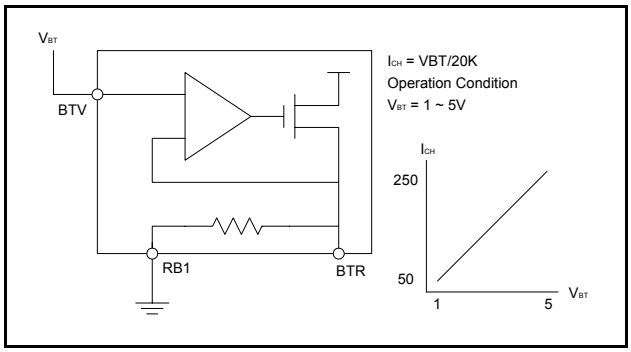
COL/ROW		1	1	1	1	1	1	0	0	0	0
Mode1		0/1	0/1	0	0	1	1	1	1	0	0
Mode2		0/1	0/1	1	1	0	0	0	0	1	1
L/R		1	0	1	0	1	0	1	0	1	0
Data In		DIO1C	DIO2C	DIO1C	DIO2C	DIO1C	DIO2C	DIO1C	DIO2C	DIO1C	DIO2C
Data Out		DIO2C	DIO1C	DIO2C	DIO1C	DIO2C	DIO1C	DIO2C	DIO1C	DIO2C	DIO1C
Figure of Clock	1st	O[80]	O[1]	O[64]	O[17]	O[48]	O[33]	O[32]	O[49]	O[16]	O[65]
	|	|	|	|	|	|	|	|	|	|	|
	16th	O[65]	O[16]	O[49]	O[32]	O[33]	O[48]	O[17]	O[64]	O[1]	O[80]
	17th	O[64]	O[17]	O[48]	O[33]	O[32]	O[49]	O[16]	O[65]	NA	NA
	|	|	|	|	|	|	|	|	|	NA	NA
	32nd	O[49]	O[32]	O[33]	O[48]	O[17]	O[64]	O[1]	O[80]	NA	NA
	33rd	O[48]	O[33]	O[32]	O[49]	O[16]	O[65]	NA	NA	NA	NA
	|	|	|	|	|	|	|	NA	NA	NA	NA
	48th	O[33]	O[48]	O[17]	O[64]	O[1]	O[80]	NA	NA	NA	NA
Figure of Clock	49th	O[32]	O[49]	O[16]	O[65]	NA	NA	NA	NA	NA	NA
	|	|	|	|	|	NA	NA	NA	NA	NA	NA
	64th	O[17]	O[64]	O[1]	O[80]	NA	NA	NA	NA	NA	NA
	65th	O[16]	O[65]	NA	NA	NA	NA	NA	NA	NA	NA
	|	|	|	NA	NA	NA	NA	NA	NA	NA	NA
	80th	O[1]	O[80]	NA	NA	NA	NA	NA	NA	NA	NA

6.3.2. Row driver

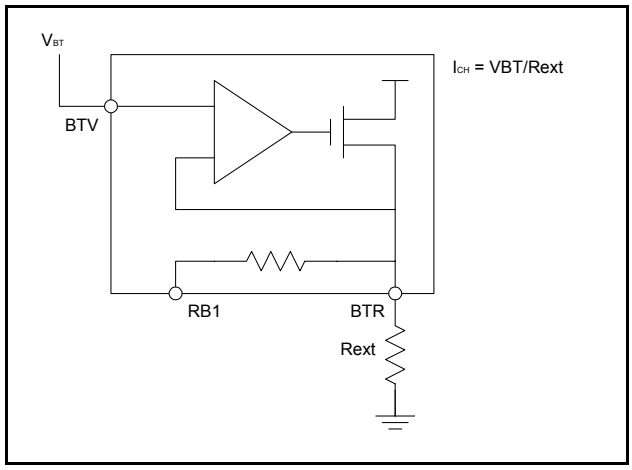
COL/ROW		0	0	0	0	0	0	1	1	1	1
Mode1		0/1	0/1	0	0	1	1	1	1	0	0
Mode2		0/1	0/1	1	1	0	0	0	0	1	1
L/R		1	0	1	0	1	0	1	0	1	0
Data In		DIO1R	DIO2R	DIO1R	DIO2R	DIO1R	DIO2R	DIO1R	DIO2R	DIO1R	DIO2R
Data Out		DIO2R	DIO1R	DIO2R	DIO1R	DIO2R	DIO1R	DIO2R	DIO1R	DIO2R	DIO1R
Figure of Clock	1st	O[1]	O[80]	O[17]	O[64]	O[33]	O[48]	O[49]	O[32]	O[65]	O[16]
	|	|	|	|	|	|	|	|	|	|	|
	16th	O[16]	O[65]	O[32]	O[49]	O[48]	O[33]	O[64]	O[17]	O[80]	O[1]
	17th	O[17]	O[64]	O[33]	O[48]	O[49]	O[32]	O[65]	O[16]	NA	NA
	|	|	|	|	|	|	|	|	|	NA	NA
	32nd	O[32]	O[49]	O[48]	O[33]	O[64]	O[17]	O[80]	O[1]	NA	NA
	33rd	O[33]	O[48]	O[49]	O[32]	O[65]	O[16]	NA	NA	NA	NA
	|	|	|	|	|	|	|	|	NA	NA	NA	NA
	48th	O[48]	O[33]	O[64]	O[17]	O[80]	O[1]	NA	NA	NA	NA
	49th	O[49]	O[32]	O[65]	O[16]	NA	NA	NA	NA	NA	NA
	|	|	|	|	|	|	NA	NA	NA	NA	NA	NA
	64th	O[64]	O[17]	O[80]	O[1]	NA	NA	NA	NA	NA	NA
	65th	O[65]	O[16]	NA	NA	NA	NA	NA	NA	NA	NA
	|	|	|	NA	NA	NA	NA	NA	NA	NA	NA	NA
	80th	O[80]	O[1]	NA	NA	NA	NA	NA	NA	NA	NA

6.4. Brightness Control

6.4.1. Using internal resistor

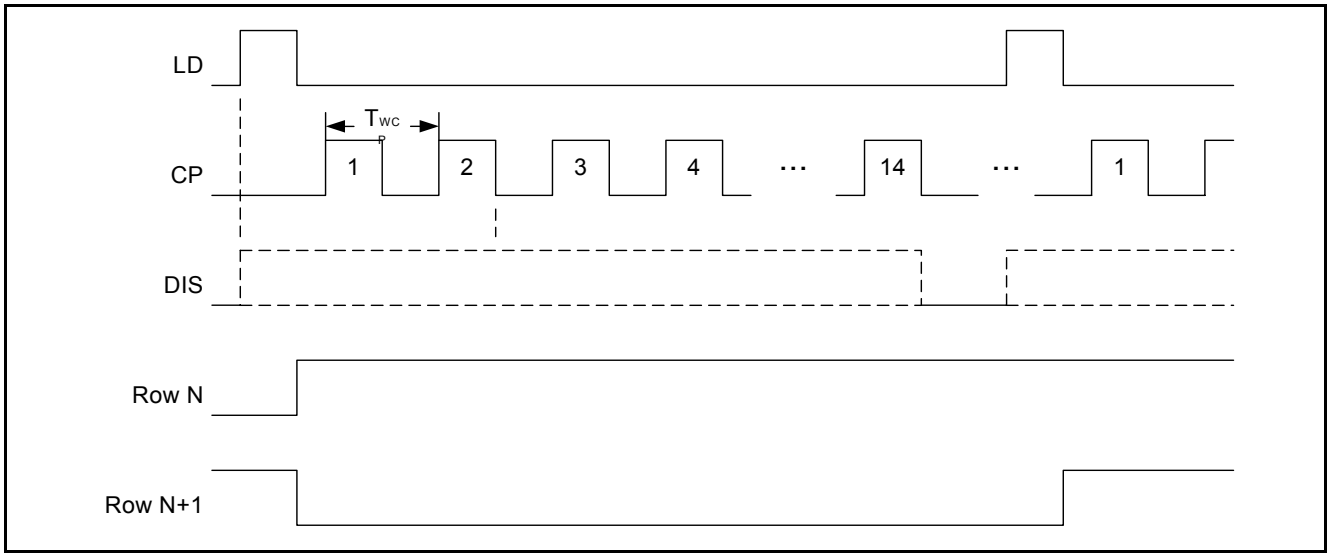


6.4.2. Using external resistor



6.5. Internal Discharge Function

SPOD80A supports internal discharge function. An internal discharge pulse will be active at the rising edge of 'LD', and be inactive at the falling edge of 'CP', the duration of the internal discharge pulse is programmable. By setting DIS2 - DIS4, user can set discharge pulse width to be 0, 2, 4, 6, 8, 10, 12, 14 T_{WCP}, period of shift clock CP. The default value of DIS4 - DIS2 is 010, where DIS2 is LSB; DIS4 is MSB. This function is only valid when used as column driver.



7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (Logic)	VDD	-0.5 ~ 7.0	V
Supply voltage (Driving buffer)	V_{LED}	-0.5 ~ 18.0	V
Input voltage range	V_{IN}	-0.5 ~ VDD+0.5	V
Output voltage range	V_{OUT}	-0.5 ~ VDD+0.5	V
Storage temperature	T_{STG}	-45.0 to 125.0	℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD	2.4	-	5.5	V
Supply voltage (Driving buffer)	VLED	9.0	-	16.0	V
Operating temperature	T_{OPR}	-20.0	-	70.0	℃

7.3. DC Characteristics

7.3.1. Column mode

(VSS = VSS2 = 0V；VDD = 2.4V - 5.5V; VLED = 16.0V; T_{OPR} = -20℃ ~ 70℃)

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}	VDD = 3.3V	DIO1C, L/R, DIO2C, CP, DIO1R, CV, DIO2R, LD, MODE1, FLT, MODE2, COL/ROW, DIS2, DIS3, DIS4, DISPOFF	2.0	-	-	V
	V_{IL}	VDD = 3.3V		-	-	0.8	V
Output voltage (1)	V_{OH1}	I_{OH} = -0.2mA	DIO1C, DIO2C, DIO1R, DIO2R	VDD-0.2	-	-	V
	V_{OL1}	I_{OL} = 0.2mA		-	-	0.2	V
Input leakage current (1)	I_{HIL1}	V_{IN} = VDD	L/R, CP, LD, COL/ROW, MODE1, MODE2, DISPOFF	-	-	1.0	µA
	I_{LIL1}	V_{IN} = VSS		-1.0	-	-	µA
Input leakage current (2)	I_{HIL2}	V_{IN} = VDD	CV, DIS3, FLT	-	-	1.0	µA
	I_{LIL2}	V_{IN} = VSS		-40	-	-	µA
Input leakage current (3)	I_{HIL3}	V_{IN} = VDD	DIS2, DIS4	-	-	40	µA
	I_{LIL3}	V_{IN} = VSS		-1.0	-	-	µA
I/O leakage current	I_{HIOL}	V_{IN} = VDD	DIO1C, DIO2C, DIO1R, DIO2R	-	-	2.0	µA
	I_{LIOL}	V_{IN} = VSS		-2.0	-	-	µA
Column ON output current	I_{CH}	V_{BTV} = 5.0V, CV = 'H'	*1	-200	-250	-300	µA
Column OFF output current	I_{CL}	CV = 'H', FLT = 'H'		-1.0	-	-	µA
Column On output voltage	V_{CH}	CV = 'L', I_{CH} = -0.2mA	*1	VLED-0.3V	-	-	V
Column OFF output voltage	V_{CL}	CV = 'L', I_{CL} = 0.2mA		-	-	0.3	V
Supply current	I_{CVDD}	*2	VDD	-	-	1.0	mA
	I_{CVLED}		VLED	-	-	200	µA
Display OFF current	I_{COFF1}	*3	VDD	-	-	1.0	mA
	I_{COFF2}		VLED	-	-	1.0	µA

7.3.2. Row mode

(VSS = VSS2 = 0V；VDD = 2.4V - 5.5V; VLED = 16.0V; T_{OPR} = -20℃ ~ 70℃)

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}	VDD = 3.3V	DIO1C, L/R, DIO2C, CP, DIO1R, CV, DIO2R, LD, MODE1, FLT, MODE2, COL/ROW, DIS2, DIS3, DIS4, DISPOFF	2.0	-	-	V
	V_{IL}	VDD = 3.3V		-	-	0.8	V
Output voltage	V_{OH}	I_{OH} = -0.2mA	DIO1C, DIO2C, DIO1R, DIO2R,	VDD-0.2	-	-	V
	V_{OL}	I_{OL} = 0.2mA		-	-	0.2	V
Input leakage current	I_{HIL1}	V_{IN} = VDD	L/R, CP, LD, COL/ROW, MODE1, MODE2, DISPOFF	-	-	1.0	μA
	I_{LIL1}	V_{IN} = VSS		-1.0	-	-	μA
Input leakage current (2)	I_{HIL2}	V_{IN} = VDD	CV, DIS3, FLT	-	-	1.0	μA
	I_{LIL2}	V_{IN} = VSS		-40	-	-	μA
Input leakage current (3)	I_{HIL3}	V_{IN} = VDD	DIS2, DIS4	-	-	40	μA
	I_{LIL3}	V_{IN} = VSS		-1.0	-	-	μA
I/O leakage current	I_{HIOL}	V_{IN} = VDD	DIO1C, DIO2C, DIO1R, DIO2R	-	-	2.0	μA
	I_{LIOL}	V_{IN} = VSS		-2.0	-	-	μA
Row OFF output voltage	V_{RH}	I_{RH} = -0.2mA	*4	VLED-0.3	-	-	V
Row ON output voltage	V_{RL}	I_{RL} = 48mA (*5)		-	-	1.92	V
Supply current	I_{RVDD}	*2	VDD	-	-	1.0	mA
	I_{RVLED}		VLED	-	-	150	μA
Display OFF current	I_{ROFF1}	*3	VDD	-	-	1.0	mA
	I_{ROFF2}		VLED	-	-	1.0	μA

Note*1: Depending on the selected mode, the applicable pins will be

COL/ROW	Mode1	Mode2	L/R	Applicable Pins
1	0/1	0/1	1	O[1:80]
1	0/1	0/1	0	O[1:80]
1	0	1	1	O[1:64]
1	0	1	0	O[17:80]
1	1	0	1	O[1:48]
1	1	0	0	O[33:80]
0	1	0	1	O[1:32]
0	1	0	0	O[49:80]
0	0	1	1	O[1:16]
0	0	1	0	O[65:80]

Note*2: VDD = 3.0V, f_{CP} = 2.08MHz, f_{LD}=12.8KHz, No load. The input data is turned over by CP.

Note*3: VDD = 3.0V, f_{CP} = 5.0MHz, No load. The input data is turned over by CP. DISPOFF set to 'L'.

Note*4: Depending on the selected mode, the applicable pins will be

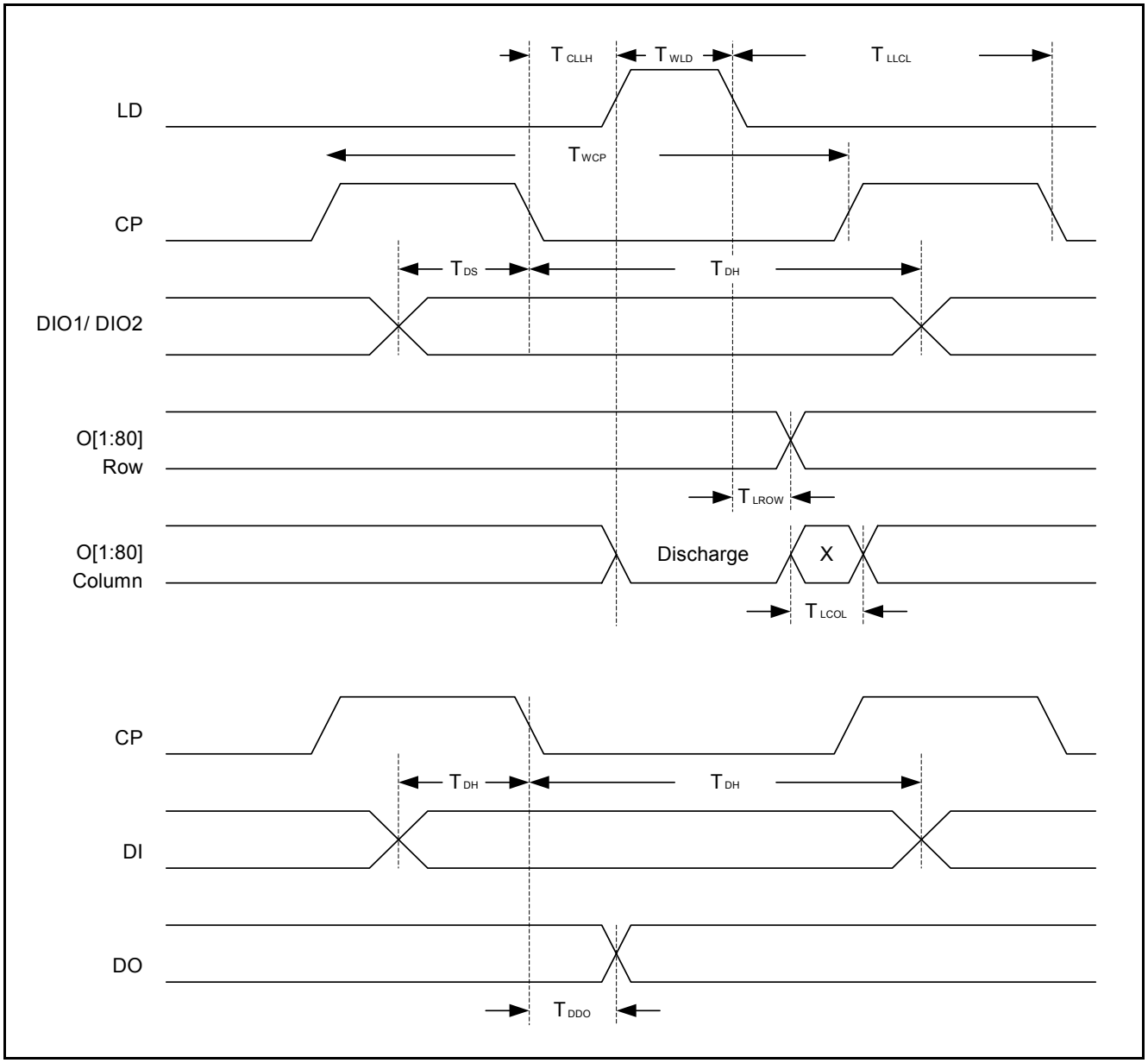
COL/ROW	Mode1	Mode2	L/R	Applicable Pins
1	0	1	1	O[65:80]
1	0	1	0	O[1:16]
1	1	0	1	O[49:80]
1	1	0	0	O[1:32]
0	1	0	1	O[33:80]
0	1	0	0	O[1:48]
0	0	1	1	O[17:80]
0	0	1	0	O[1:64]
0	0/1	0/1	1	O[1:80]
0	0/1	0/1	0	O[1:80]

Note*5: Because of the row driving capability of SPOD80A, the maximum column lines that SPOD80A can drive are 160. That is, there are only 2 SPOD80As can cascade as column drivers when using SPOD80A as row driver.

7.4. AC Characteristic

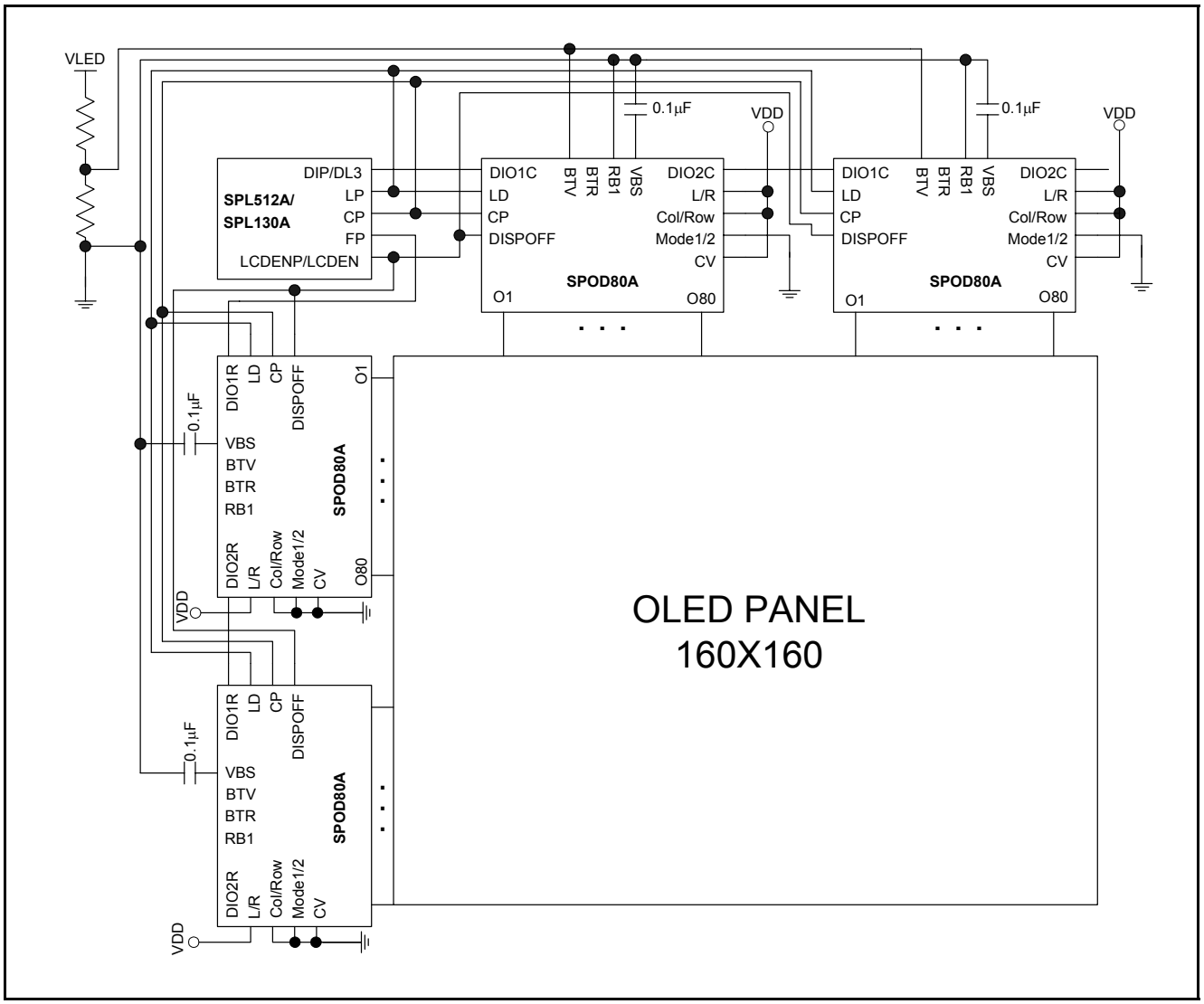
(VSS = VSS2 = 0V; VDD = 2.4V - 5.5V; VLED = 16.0V; T_{OPR} = -20℃ ~ 70℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	T_{WCP}		200	-	-	ns
Data latch in setup time	T_{DS}		40	-	-	ns
Data latch in hold time	T_{DH}		40	-	-	ns
CP low to LD high	T_{CLLH}		20	-	-	ns
LD low to CP low	T_{LLCL}		20	-	-	ns
LD 'H' pulse width	T_{WLD}		100	-	-	ns
LD low to Row output	T_{LROW}	Load = 0.6nF	-	-	9.0	μs
LD high to column output	T_{LCOL}	*6	-	-	-	ns
Output delay time	T_{DDO}	C_L = 15pF	40	-	100	ns



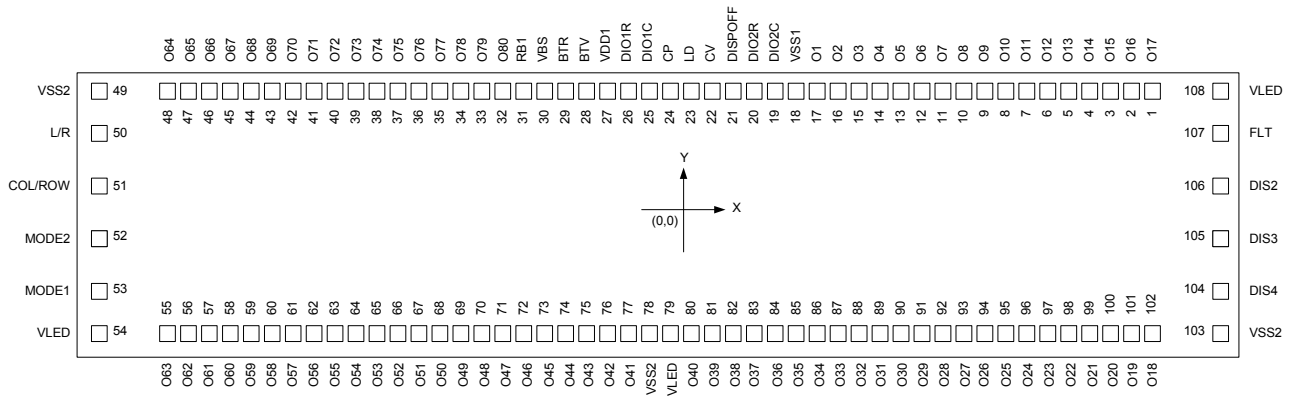
Note*6: Depending on loading, please refer to DC characteristics.

8. APPLICATION CIRCUIT



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 7960μm x 1470μm

PAD Size: 100μm x 100μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure that the IC function properly, bond all VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPOD80A-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	O17	3329	598	45	O67	-2871	598
2	O16	3169	598	46	O66	-3021	598
3	O15	3019	598	47	O65	-3171	598
4	O14	2869	598	48	O64	-3331	598
5	O13	2729	598	49	VSS2	-3833	586
6	O12	2589	598	50	L/R	-3833	383
7	O11	2449	598	51	COL/ROW	-3833	127
8	O10	2309	598	52	MODE2	-3833	-128
9	O9	2169	598	53	MODE1	-3833	-384
10	O8	2029	598	54	VLED	-3833	-588
11	O7	1889	598	55	O63	-3331	-600
12	O6	1749	598	56	O62	-3171	-600
13	O5	1609	598	57	O61	-3021	-600
14	O4	1469	598	58	O60	-2871	-600
15	O3	1329	598	59	O59	-2731	-600
16	O2	1189	598	60	O58	-2591	-600
17	O1	1049	598	61	O57	-2451	-600
18	VSS1	909	598	62	O56	-2311	-600
19	DIO2C	769	598	63	O55	-2171	-600
20	DIO2R	629	598	64	O54	-2031	-600
21	DISPOFF	489	598	65	O53	-1891	-600
22	CV	349	598	66	O52	-1751	-600
23	LD	209	598	67	O51	-1611	-600
24	CP	69	598	68	O50	-1471	-600
25	DIO1C	-71	598	69	O49	-1331	-600
26	DIO1R	-211	598	70	O48	-1191	-600
27	VDD1	-351	598	71	O47	-1051	-600
28	BTV	-491	598	72	O46	-911	-600
29	BTR	-631	598	73	O45	-771	-600
30	VBS	-771	598	74	O44	-631	-600
31	RB1	-911	598	75	O43	-491	-600
32	O80	-1051	598	76	O42	-351	-600
33	O79	-1191	598	77	O41	-211	-600
34	O78	-1331	598	78	VSS2	-71	-600
35	O77	-1471	598	79	VLED	69	-600
36	O76	-1611	598	80	O40	209	-600
37	O75	-1751	598	81	O39	349	-600
38	O74	-1891	598	82	O38	489	-600
39	O73	-2031	598	83	O37	629	-600
40	O72	-2171	598	84	O36	769	-600
41	O71	-2311	598	85	O35	909	-600
42	O70	-2451	598	86	O34	1049	-600
43	O69	-2591	598	87	O33	1189	-600
44	O68	-2731	598	88	O32	1329	-600

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
89	O31	1469	-600	99	O21	2869	-600
90	O30	1609	-600	100	O20	3019	-600
91	O29	1749	-600	101	O19	3169	-600
92	O28	1889	-600	102	O18	3329	-600
93	O27	2029	-600	103	VSS2	3832	-588
94	O26	2169	-600	104	DIS4	3832	-384
95	O25	2309	-600	105	DIS3	3832	-128
96	O24	2449	-600	106	DIS2	3832	127
97	O23	2589	-600	107	FLT	3832	383
98	O22	2729	-600	108	VLED	3832	586

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11. REVISION HISTORY

Date	Revision #	Description	Page
APR. 30, 2001	0.1	Original	11
JUN. 29, 2001	1.0	1. Delete "*PRELIMINARY*"	
		2. Correct PACKAGE description in the "*3. PACKAGE*"	1
		3. Correct chip size	13
		4. Add Note1 to Note3 in the "*9.1 PAD Assignment*"	13
		5. Renew to a new document format	