Integrated Circuit Systems, Inc.

ICS1891

Advanced Information

100Base-TX PHYceiver™ for Repeater Applications

General Description

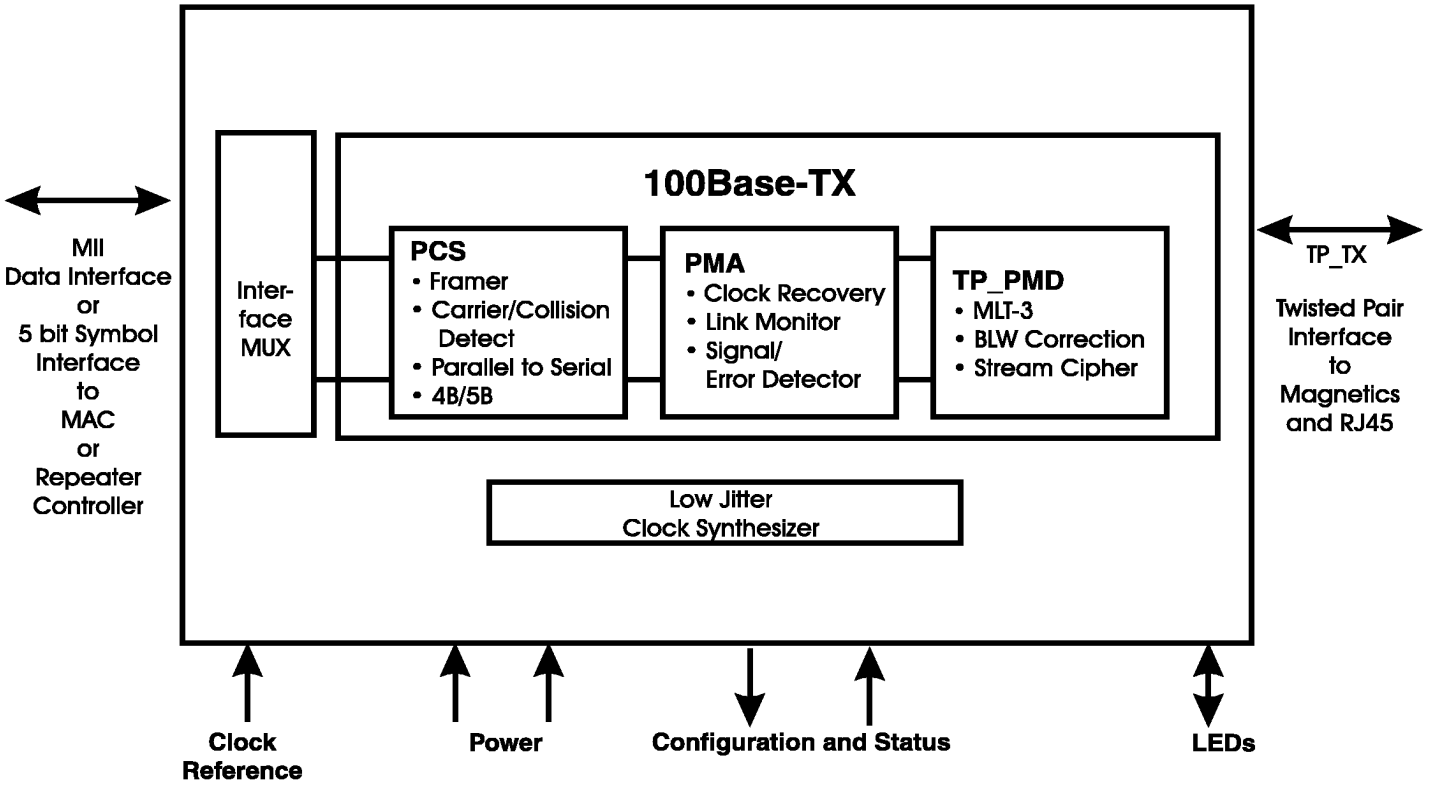
The **ICS1891** is a fully integrated physical layer device supporting 100Mb/s only CSMA/CD Fast Ethernet Repeater applications. It is designed meet the specific requirements of repeater applications such as small PCB footprint, shared data bus support, and low power. The **ICS1891** is compliant with the IEEE 802.3u Ethernet standard for 100Mb/s operation.

The **ICS1891** supports a variety of repeater controllers by providing both a standard 100Mb/s Media Independent Interface (MII) and a 5-bit symbol interface. The device allows repeater designers to implement a 100Mb/s physical layer port with one IC, a few passives, and total power consumption of less than one Watt. The **ICS1891** interfaces directly to a transmit and receive isolation transformer and can support unshielded twisted pair (UTP) category 5 cables up to 105 meters.

Features

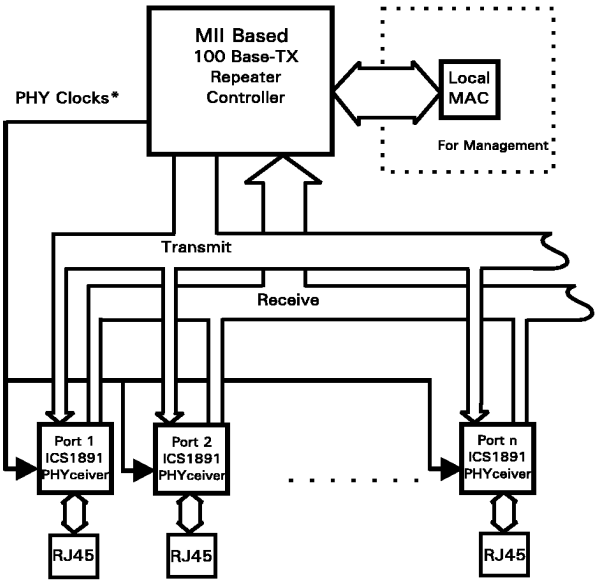
- One chip integrated physical layer
- All CMOS, Low power design (<200mA max)
- Small footprint 64-pin 14mm^2 QFP package
- IEEE 802.3u CSMA/CD compliant
- Media Independent Interface (MII)
- 5-bit Symbol Interface provided
- 100Base-TX Half Duplex
- Fully integrated TP-PMD including Stream Cipher Scrambler, MLT-3 encoder, Adaptive Equalization, and Baseline Wander Correction Circuitry

Block Diagram

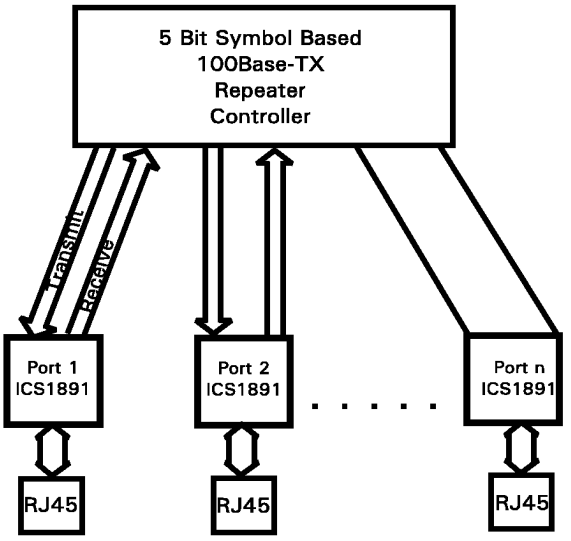


Application Designs

MII Based Repeaters



5 Bit Symbol Based Repeaters



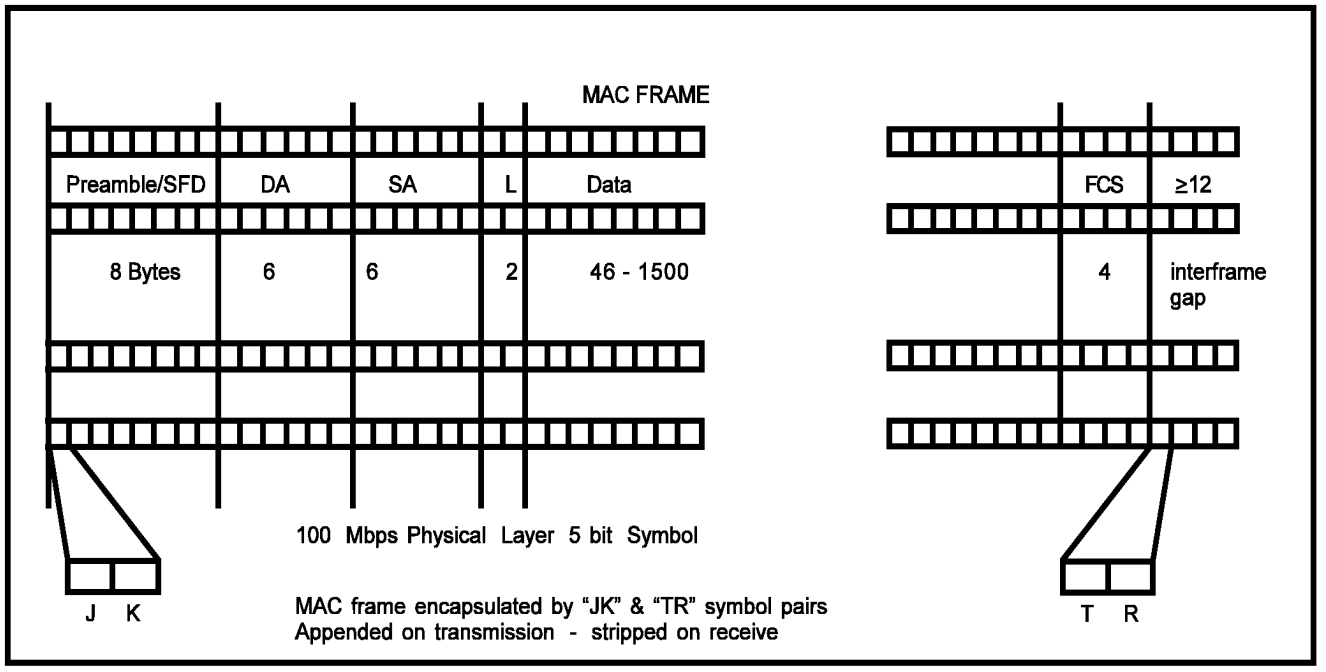
ICS1890 vs. ICS1891

The **ICS 1890** is an all purpose, fully integrated, 10/100 physical layer device targeted for all types of ethernet applications including: Adapter Cards, Repeaters, Switches, Routers, Bridges or any other application that needs 10Base-T and 100Base-T operation.

The **ICS 1891** is targeted for the 100Mb Repeater market. As the **ICS1891** does not have the 10Mb function nor Autonegotiation (details below) it is ideally suited for Half Duplex, Repeaters.

Feature guide for the differences between the 1890 and the 1891

	1890	1891
100Base-T Operation	Y	Y
MII Interface	Y	Y
5 Bit Symbol Interface	Y	Y
Half Duplex Operation	Y	Y
Hardware Configuration Mode	Y	Y
Adaptive Equalization	Y	Y
All CMOS Low Power	Y	Y
Base Line Wander Correction	Y	Y
10Base-T Operation	Y	N
Autonegotiation	Y	N
Management Interface	Y	N
Full Duplex Operation	Y	N



Architecture

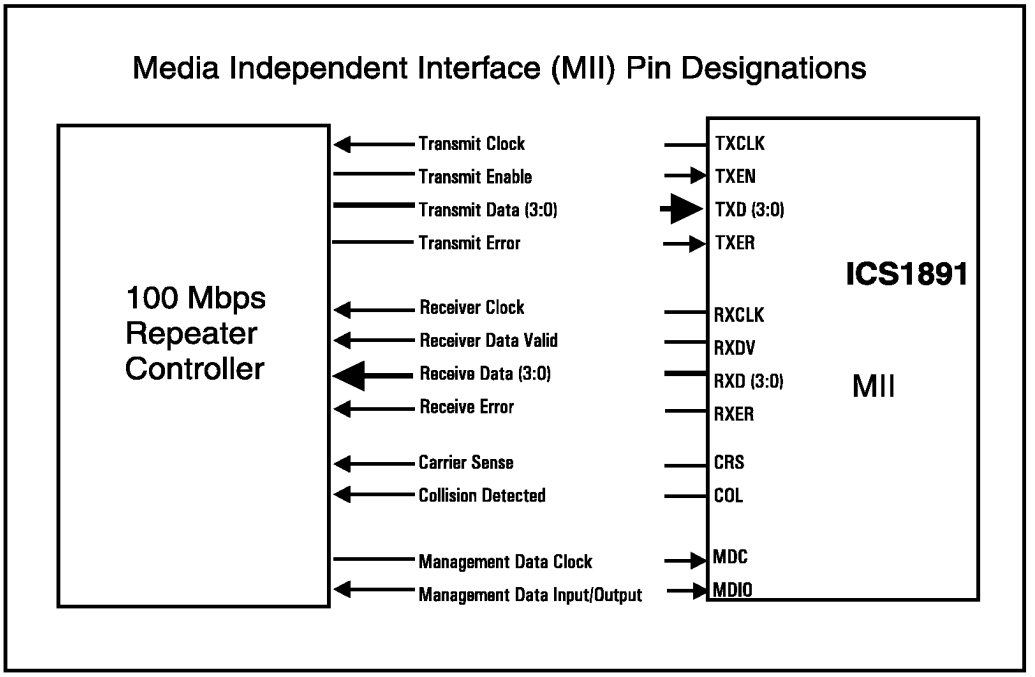
100Base-TX Operation

The **ICS1891** is essentially a nibble/bit stream processor. When transmitting, it takes sequential nibbles presented at the Media Independent Interface (MII) and translates them to a serial bit stream for transmission on the media. When receiving, it takes the serial bit stream from the media and translates it to sequential nibbles for presentation to the MII. It has no knowledge of the underlying structure of the MAC frame it is conveying.

When transmitting, the **ICS1891** encapsulates the MAC frame (including the preamble) with the start-of-stream and end-of-stream delimiters. When receiving, it strips off the SSD and substitutes the normal preamble pattern and then presents this and subsequent preamble nibbles to the MII. When it encounters the ESD, it ends the presentation of nibbles to the MII. Thus, the MAC reconciliation layer sees an exact copy of the transmitted frame.

During periods when no frames are being transmitted or received, the device signals and detects the idle condition. This allows the higher levels to determine the integrity of the connection. In the 100Base-TX mode, a continuous stream of scrambled ones is transmitted signifying the idle condition. The receive channel includes logic that monitors the IDLE data stream to look for this pattern and thereby establishes the link integrity.

The 5-bit Symbol Interface option allows access to raw groups of 5-bit data with lower latency through the PHY. This is useful in building lower latency repeaters. It also allows easy connection to repeater controllers that only support a 100Base-TX 5-bit Symbol Interface.



Interface Overviews

Overview of Repeater to PHY Interfaces

To accommodate different repeater controllers, the **ICS1891** provides two types of Repeater to PHY interfaces. The two interfaces are - MII Data Interface and 5-bit Symbol Interface.

The standard and most commonly used interface is the 100 Mb/s MII Data Interface which provides framed 4-bit nibbles and control signals. This interface also allows a seamless mix of technologies like 100Base-TX, 100 Base-FX, and 100Base-T4.

The 5-bit Symbol Interface provides 5-bits of unframed data as well as the normal MII CRS signal which can be used as a fast carrier look-ahead with customer controller. This interface is intended for 100Base-TX repeater applications that require nothing more than recovered parallel data, where all framing is handled in the repeater core logic.

MII Data Interface

The **ICS1891** implements an IEEE 802.3u Media Independent Interface.

The MII is a specification of signals and protocols which formalizes the interfacing of an Ethernet Controller to the underlying physical layer. The specification is such that different physical media may be supported (such as 100 Base-TX, 100Base-T4 and 100Base-FX) transparently to the Controller.

The MII Data Interface specifies transmit and receive data paths. Each path is 4-bits wide allowing for transmission of a data nibble. The transmit data path includes a transmit clock for synchronous transfer, a transmit enable signal and a transmit error signal. The receive data path includes a receive data clock for synchronous transfer, a receive data valid signal and a receive error signal. Both the transmit clock and receive clock are sourced by the **ICS1891**.

The **ICS1891** provides the MII signals carrier sense and collision detect. Carrier sense indicates that data is being received. Collision detect indicates that data has been received while a transmission is in progress.

5-Bit Symbol Interface

The 5-bit Symbol Interface is an alternative parallel interface between the PHY and Repeater Controller than the standard MII Data interface. The Symbol Interface bypasses the Physical Coding Sublayer (PCS) and provides a direct unframed 5-bit symbol interface to the Physical Media Access (PMA) layer. The Symbol Interface bypasses the Physical Coding Sublayer (PCS) in the **ICS1891**. 5-bit patterns placed on the STD TXD pins are serialized, MLT-3 coded and transmitted onto the cable. Received data is MLT-3 decoded parallelized, and clocked out on the SRD pins. Received data is not framed by the **ICS1891**. This function must be performed by the repeater controller along with data descrambling. The 5-bit Symbol Interface provides a lower level interface and, therefore, lower bit delay than the standard MII Data Interface.

This interface is selected by setting the MII/SI pin to SYMBOL INTERFACE mode.

The Symbol Interface consists of a 14 signal interface: STCLK, STD[4:0], SRCLK, SRD[4:0], SCRS, SD.

Data is exchanged between the Repeater Controller and PHY using 5-bit unframed code groups at 25 MHz clock rate.

A signal defect output is provided for the repeater controller's use.

The Symbol Interface provides a CRS signal by continuing to use the logic that is bypassed by this interface. This gives a carrier indication faster than is possible from the Repeater Controller since the bits are examined serially as soon as they enter the PHY.

Since only the Symbol Interface or the MII Interface is active at once, it is possible to share the MII Data interface pins for Symbol Interface functionality.

The pins have the following mapping:

MII	Symbol	Pin
TXCLK	STCLK	43
TXEN	(1)	44
TXER	STD4	42
TXD3	STD3	48
TXD2	STD2	47
TXD1	STD1	46
TXD0	STD0	45
RXCLK	SRCLK	37
RXDV	(2)	36
RXER	SRD4	38
RXD3	SRD3	32
RXD2	SRD2	33
RXD1	SRD1	34
RXD0	SRD0	35
CRS	SCRS	50
COL	(3)	49
LSTA	SD	21

(1) 100Base-TX is a continuous transmission system and the Repeater Controller is responsible for sourcing IDLE symbols when it is not transmitting data when using the Symbol Interface.

(2) Since data is not framed when this interface is used, RXDV has no meaning.

(3) Since the Repeater Controller is responsible for sourcing both active and idle data, the PHY can not tell when it is transmitting in the traditional sense, so no collisions can not be detected. Other mode configuration pins behave identically regardless of which data interface is used.

MII Management Interface

The MII standard specifies a two-wire management interface and a protocol between station management and the physical layer. The **ICS1891** is intended for unmanaged applications or applications that collect statistics without polling the PHY and, therefore, does not implement the MII Management Interface.

Twisted Pair Interface

The **ICS1891** is able to operate in 100Base-TX mode using a simple interface to a universal 1:1 magnetics module and single RJ-45 connector jack.

The interface signals consist of a differential pair of transmit signals and a differential pair of receive signals. The interface also provides a pin for setting the 100M transmit current.

Clock Reference Interface

The **ICS1891** synthesizes all its required clock signals from a single 25 MHz frequency reference supplied to the Clock Reference Interface (REF_IN).

Any reference must meet the stringent IEEE standard requirements for total accuracy under all conditions of ±50 parts per million (ppm), even though the device can easily function (out of specification) with a less accurate reference.

Two reference configurations are supported.

A simple CMOS level signal may be fed into the REF_IN.

A CMOS level crystal oscillator module may be used to provide the frequency reference for the REF_IN input instead of a simple reference.

Configuration and Status Interface

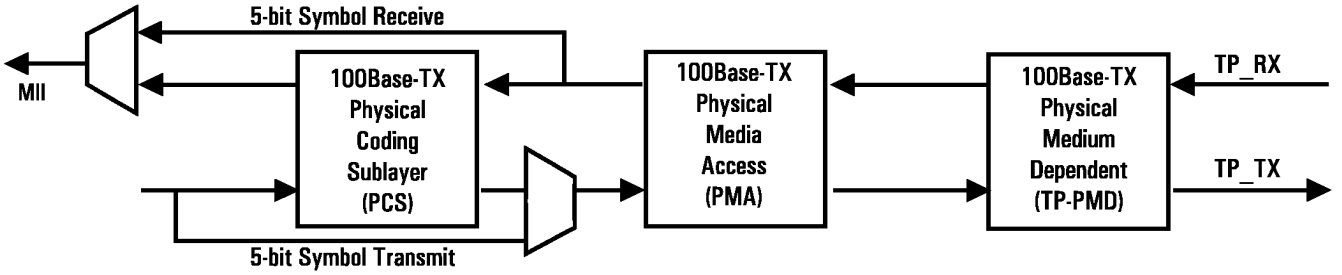
This interface provides a full set of pins to allow the device to be completely configured by hardware.

The interface also provides dynamic tristate control over both the Twisted Pair Transmit interface and the MII Receive interface.

Link Status and Stream Cipher Locking status signals are provided for use by a Repeater Conroller or custom logic.

LED Interface

LEDs for Activity, Collision and Link are provided by the **ICS1891**. The Pin Description section provides detailed connection instructions.



Major 100Base-TX Blocks

Functional Blocks

100Base-TX Physical Coding Sublayer [PCS]

Carrier Detector & Framer

The carrier detector examines the serial bit stream looking for the SSD, the "JK" symbol pair. In the idle state, IDLE symbols (all logic ones) will be received. If the carrier detector detects a logic zero in the bit stream, it examines the following bits looking for the first two non-contiguous zeros, confirms that the first 5-bits form the "J" symbol (11000) and asserts carrier detect. At this point the serial data is framed and the second symbol is checked to confirm the "K" symbol (10001). If successful, the following framed data (symbols) are presented to the 4B5B decoder. If the "JK" pair is not confirmed, the false carrier detect is asserted and the idle state is re-entered.

Collision Detector

Collision is asserted when transmission and data reception occur simultaneously.

Parallel/Serial Converter

This block converts data between 4-bit nibbles and 1-bit serial data.

4B/5B Encoder/Decoder

When the **ICS1891** is operating in the 100Base-TX mode, 4B5B coding is used. This coding scheme maps a 4-bit nibble to a 5-bit code group. Since this gives 32 possible symbols and the data only requires 16 symbols, 16 symbols are designated control or invalid. The control symbols used are "JK" as the start-of-stream delimiter (SSD), "TR" as the end-of-stream delimiter (ESD), "I" as the IDLE symbol and "H" to signal an error. All other symbols are invalid and, if detected, will set the receive error bit in the status register.

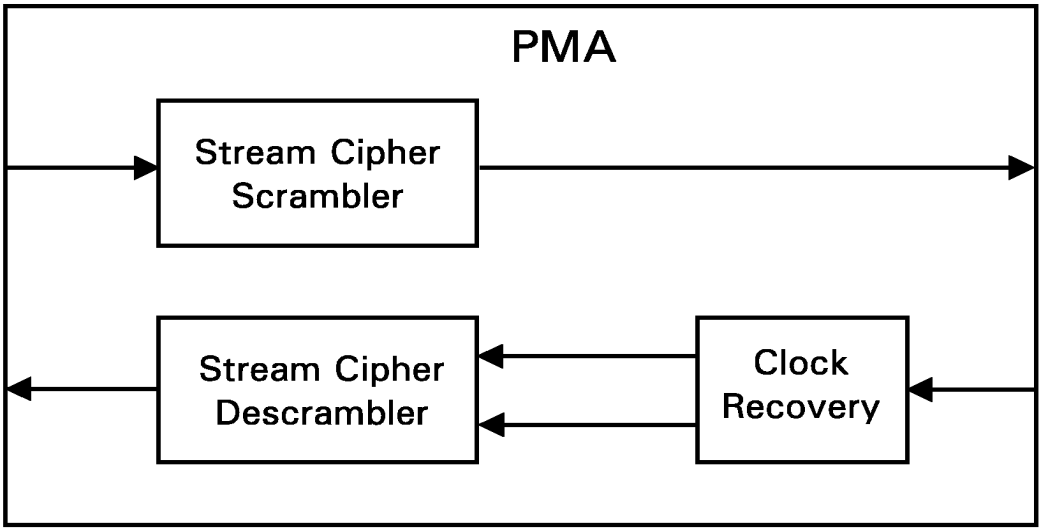
When transmitting, nibbles from the MII are converted to 5-bit code groups. The first 16 nibbles obtained from the MII are the Repeater Controller frame preamble. The **ICS1891** replaces the first two nibbles with the start-of-stream delimiter (the "JK" symbol pair). Following the last nibble, the **ICS1891** adds the end-of-stream delimiter (the "TR" symbol pair).

When receiving, 5-bit code groups are converted to nibbles and presented to the MII. If the **ICS1891** detects one or more invalid symbols, it sets the receive error bit in the status register. When receiving a frame, the first two 5-bit code groups received are the start-of-stream delimiter (the "JK" symbol pair), the **ICS1891** strips them and substitutes two nibbles of the normal preamble pattern. The last two 5-bit code groups are the end-of-stream delimiter (the "TR" symbol group), these are stripped from the nibbles presented to the Repeater Controller.

4B5B EncodingTable

Symbol	Meaning	4B Code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
I	Idle	undefined	11111
J	SSD	0101	11000
K	SSD	0101	10001
T	ESD	undefined	01101
R	ESD	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001

Symbol	Meaning	4B Code 3210	5B Code 43210
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V(S)	Invalid	undefined	11001



100Base-T Physical Media Access [PMA]

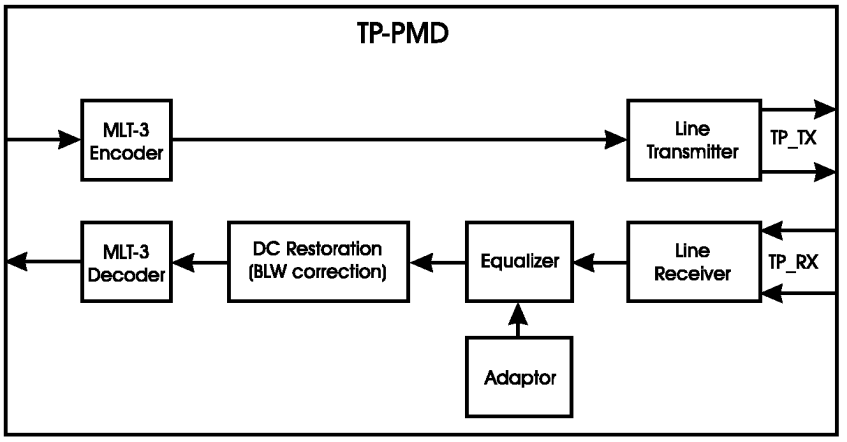
Clock Recovery

The Clock Recovery block locks onto the incoming data stream, extracts the embedded clock, and presents the data synchronized to the recovered clock. This process produces signals with very low timing uncertainty and noise (jitter).

In the event that the PLL is unable to lock on to the receive signal, it generates a "not locked signal." The transmit clock synthesizer provides a center frequency reference for operation of the clock recovery circuit in the absence of data. The "receive signal detected" and "not locked" signals are both used by the logic which monitors the receive channel for errors.

Transmit Clock Synthesizer

The **ICS1891** synthesizes the transmit clock using a PLL to produce 25 MHz for 100Base-TX. Internal clock frequencies of 125 MHz are also generated. This allows the use of a low cost 25 MHz crystal oscillator or a low jitter reference frequency.



100Base-T Twisted Pair Physical Media Dependent [TP-PMD]

Stream Cipher Scrambler/Descrambler

When the **ICS1891** is operating in the 100Base-TX mode, a stream cipher scrambler/descrambler that conforms to theANSI Standard X3T9.5 FDDI TP-PMD is employed. The purpose of the stream cipher scrambler is to randomize the 100 Mbps data on transmission resulting in a reduction of the peak amplitudes in the frequency spectrum. The stream cipher descrambler restores the received 5-bit code groups to their unscrambled values.

MLT-3 Encoder/Decoder

When the **ICS1891** is operating in the 100Base-TX mode, an MLT-3 encoder and decoder is employed. The purpose of the MLT-3 encoder is to convert the NRZI transmitted bit stream to a three-level code resulting in a reduction in the energy over the critical frequency range of 20 MHz to 100 MHz. The MLT-3 decoder converts the received three-level code back to an NRZI bit stream.

DC Restoration

The 100Base-TX specification uses a stream cipher scrambler in order minimize peak amplitudes in the frequency spectrum. However, the nature of the stream cipher and MLT-3 encoding is such that long run lengths of zeroes can cause the production of a DC component. This DC component cannot be transmitted through the isolation transformers and results in baseline wander. Baseline wander decreases noise immunity since the baseline moves closer to either the positive or negative signal comparaters. Figure 1 is an exaggerated simulation of the effect of baseline wander (the time period would normally be much longer).

The **ICS1891** uses DC restoration to restore the lost DC component of the recovered digital data, thus correcting for baseline wander.

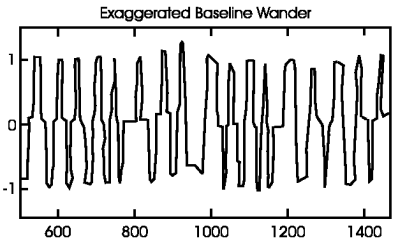


Figure 1

Adaptive Equalizer

The **ICS1891** includes an adaptive equalizer to compensate for signal amplitude and phase distortion incurred from the transmission media. Signal equalization will actively occur for twisted pair cable lengths of up to 105 meters.

At a data rate of 100 Mbps, the cable introduces significant signal distortion due to high frequency roll off and phase shift. The high frequency loss is mainly due to skin-effect which causes the conductor resistance to rise as the square of the frequency (see Figure 2).

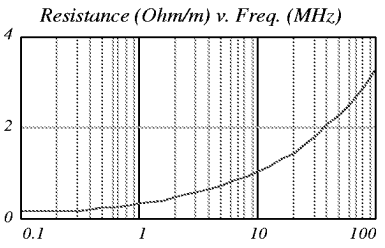


Figure 2

Typical and worst case frequency response for 100 meters (worst case length as derived from draft standard EIA/TIA-568-A) of UTP Category 5 cable is shown in Figure 3.

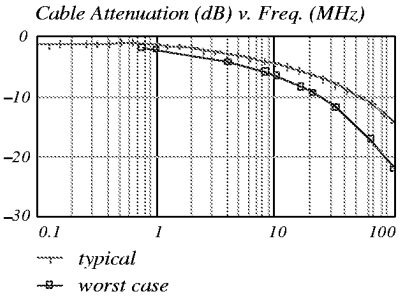


Figure 3

The pulse shape of the received signal is critical for MLT-3 encoded data since there are three distinct levels to resolve in order to properly recover the data. Figure 4 shows the typical signal at the input and output ends of 100 meters of UTP Category 5 cable.

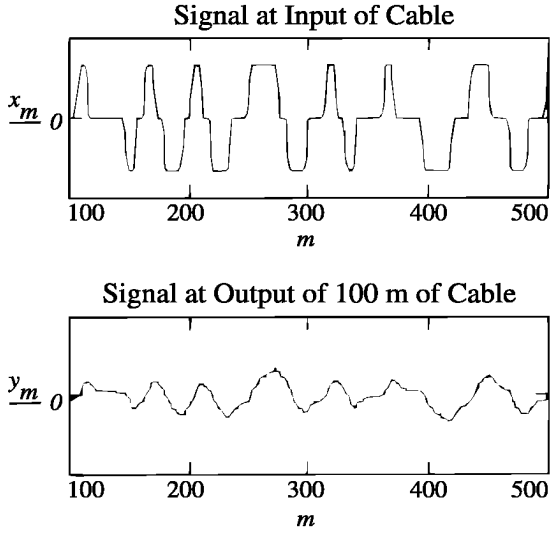


Figure 4

Since the cable length that must be equalized can be anything from 0 to 105 meters, the optimum equalization cannot be fixed, but must depend on cable length. Thus, adaptive equalization must be applied at the receive end to restore the signal.

Since the signal amplitude at the transmit end of the cable is known (2.0V differential), the received signal amplitude reveals the cable length and the adaptive equalizer can adjust the amount of equalization by sensing the amplitude of the received pulses. To illustrate, as the received pulse amplitude decreases, the equalizer applies more equalization since it can be inferred that the cable length is longer. As a loop tries to drive the amplitude of the received pulses to a constant reference by controlling a variable gain amplifier, the control signal which results can be used to control the frequency response equalization as well. Of course, the equalization need not change rapidly, since once a particular cable run is installed the attenuation and high frequency loss remain relatively constant.

Line Transmitter

The line transmitter logic of the **ICS1891** is a current-driven differential driver which generates a three-level (100Base-TX, MLT-3) transmission. Waveshaping is applied to control the output edge rate and eliminate the need for expensive external filters. The transmitter interfaces directly to an inexpensive isolation transformer (magnetics).

Line Receiver

The line receiver circuit accepts a differential three-level (100Base-TX, MLT-3) signal which first passes through an isolation transformer.

Magnetics

A Universal Magnetics module is used to provide isolation and signal coupling onto the twisted pair cabling for 100Base-TX.

Pin Descriptions

Signal	Meaning	Signal	Meaning
TXCLK*	Transmit Clock		
TXEN*	Transmit Enable	MII/SI	MII Data/Stream Interface
TXD3*	Transmit Data 3		
TXD2	Transmit Data 2		
TXD1*	Transmit Data 1		
TXD0*	Transmit Data 0		
TXER*	Transmit Error		
		ITCLS~	Invert Transmit Clock Latching Setting
RXCLK*	Receive Clock	TPTRI	Twisted Pair Tristate
RXDV*	Receive Data Valid	RXTRI	Receive Repeater-PHY Interface Tristate
RXD3	Receive Data 3	LSTA*	Link Status
RXD2*	Receive Data 2	RESET~	System Reset
RXD1*	Receive Data 1		
RXD0*	Receive Data 0		
RXER*	Receive Error		
CRS*	Carrier Sense		
COL*	Collision Detect	LILED	Link Integrity LED
		CLLED	Collision det LED
		ACLED	Activity LED
REF_IN	Frequency reference		
		N/C	17 No Connect Pins
TP_TX+	Twisted Pair Transmit Data+		
TP_TX-	Twisted Pair Transmit Data-	VDD	9 VDD Pins
TP_RX+	Twisted Pair Receive Data+	VSS	7 VSS Pins
TP_RX-	Twisted pair Receive Data-		
100TCSR	100M Transmit Current Set Resistor		

* Re-defined for symbol Repeater-PHY interface

Pin Descriptions

MII Data Interface

The following pin descriptions apply in either 10 or 100 Mbps mode when the MII Data Interface is selected. These pins are re-used for the 5-bit Symbol Interface, 10M Serial Interface, and the Link Pulse Interface. These extra pin meanings are described in separate interface sections with the "pseudo" pin name followed by the actual pin name that the function is mapped onto.

Transmit Clock **TXCLK**

The Transmit Clock (TXCLK) is a continuous clock signal generated by the **ICS1891** to synchronize information transfer on the Transmit Enable, Transmit Data and Transmit Error lines. The **ICS1891** clock frequency is 25 MHz.

Transmit Enable **TXEN**

Transmit Enable (TXEN) indicates to the **ICS1891** that the Repeater is sending valid data nibbles for transmission on the physical media. Synchronous with its assertion, the **ICS1891** will begin reading the data nibbles on the transmit data lines. It is the responsibility of the MAC to order the nibbles so that the preamble is sent first, followed by destination, source, length, data and CRC fields since the **ICS1891** has no knowledge of the frame structure and is merely a "nibble" processor. The **ICS1891** terminates transmission of nibbles following the de-assertion of Transmit Enable (TXEN).

Transmit Data 3 **TXD3**

Transmit Data 3 (TXD3) is the most significant bit of the transmit data nibble. TXD3 is sampled by the **ICS1891** synchronously with the Transmit Clock when TXEN is asserted. When TXEN is de-asserted, the **ICS1891** is unaffected by the state of TXD3.

Transmit Data 2 **TXD2**

Transmit Data 2 (TXD2) is sampled by the **ICS1891** synchronously with the Transmit Clock when TXEN is asserted. When TXEN is de-asserted, the **ICS1891** is unaffected by the state of TXD2.

Transmit Data 1 **TXD1**

Transmit Data 1 (TXD1) is sampled by the **ICS1891** synchronously with the Transmit Clock when TXEN is asserted. When TXEN is de-asserted, the **ICS1891** is unaffected by the state of TXD1.

Transmit Data 0 **TXD0**

Transmit Data 0 (TXD0) is the least significant bit of the transmit data nibble. TXD0 is sampled by the **ICS1891** synchronously with the Transmit Clock when TXEN is asserted. When TXEN is de-asserted, the **ICS1891** is unaffected by the state of TXD0.

Transmit Error **TXER**

The assertion of Transmit Error (TXER) for one or more clock periods will cause the **ICS1891** to emit one or more invalid symbols. The signal must be synchronous with TXCLK. In the normal operating mode, a HALT symbol will be substituted for the next nibble decoded.

Receive Clock **RXCLK**

The Receive Clock (RXCLK) is sourced by the **ICS1891**. There are two possible sources for the Receiver Clock (RXCLK). When a carrier is presented on the receiver pair, the source is the recovered clock from the data stream. When no carrier is present on the receiver pair, the source is the Transmit Clock (TXCLK). The IDLE symbol is sent during periods of inactivity and the Recovered clock will be selected.

The **ICS1891** will only switch between clock sources when Receive Data Valid (RXDV) is de-asserted. During the period between Carrier Sense (CRS) being asserted and Receive Data Valid being asserted, a clock phase change of up to 360 degrees may occur. Following the de-assertion of Receive Data Valid a clock phase of 360 degrees may occur.

When Receive Data Valid is asserted, the Receive Clock frequency is 25 MHz. The **ICS1891** synchronizes Receive Data Valid, Received Data and Receive Error with Receive Clock (RXCLK).

Receive Data Valid **RXDV**

Receive Data Valid (RXDV) is generated by the **ICS1891**. It indicates that the **ICS1891** is recovering and decoding data nibbles on the Receive Data (RXD) data lines synchronous with the Receive Data Clock (RXCLK). It is the responsibility of the Repeater to frame the nibbles since the **ICS1891** has no knowledge of the frame structure and is merely a "nibble" processor. The **ICS1891** asserts RXDV when it detects and recovers the preamble or the start of stream delimiter (SSD) and de-asserts it following the last data nibble or upon detection of a signal error. RXDV is synchronous with the Receive Data Clock (RXCLK).

Receive Data 3 **RXD3**

Receive Data 3 (RXD3) is the most significant bit of the receive data nibble. RXD is sourced by the **ICS1891**. When Receive Data Valid (RXDV) is asserted by the **ICS1891**, it will transfer the 4th bit of the symbol synchronously with Receive Clock (RXCLK).

Receive Data 2 **RXD2**

Receive Data 2 (RXD2) is sourced by the **ICS1891**. When Receive Data Valid (RXDV) is asserted by the **ICS1891**, it will transfer the 3rd bit of the symbol synchronously with Receive Clock (RXCLK).

Receive Data 1 **RXD1**

Receive Data 1 (RXD1) is sourced by the **ICS1891**. When Receive Data Valid (RXDV) is asserted by the **ICS1891**, it will transfer the 2nd bit of the symbol synchronously with Receive Clock (RXCLK).

Receive Data 0 **RXD0**

Receive Data 0 (RXD0) is the least significant bit of the receive data nibble. RXD0 is sourced by the **ICS1891**. When Receive Data Valid (RXDV) is asserted by the **ICS1891**, it will transfer the 1st bit of the symbol synchronously with Receive Clock (RXCLK).

Receive Error **RXER**

The **ICS1891** detects two types of receive errors, errors occurring during the reception of valid frames and an error condition known as false carrier detect. False carrier detect is signaled so that repeater applications can prevent the propagation of false carrier detection. RXER always transitions synchronously with RXCLK.

The assertion of Receive Error (RXER) for one or more clock periods during the period when RXDV is asserted (receiving a frame) indicates that the **ICS1891** has detected a read channel error. There are three sources of read channel error: loss of receive signal, failure of the PLL to lock and invalid symbol detection.

RXER may also be asserted when RXDV is de-asserted. The **ICS1891** will assert RXER and set RXD(3:0) to 1110 if a false carrier is detected. For a good carrier to be detected, the **ICS1891** looks continuously at the incoming IDLE stream (1111...) for two non-contiguous logic zeroes and then checks for the SSD of "JK." In the event that two non-contiguous logic zeroes are detected but the JK symbol pair is not, then a false carrier condition is signaled and the IDLE condition is re-entered.

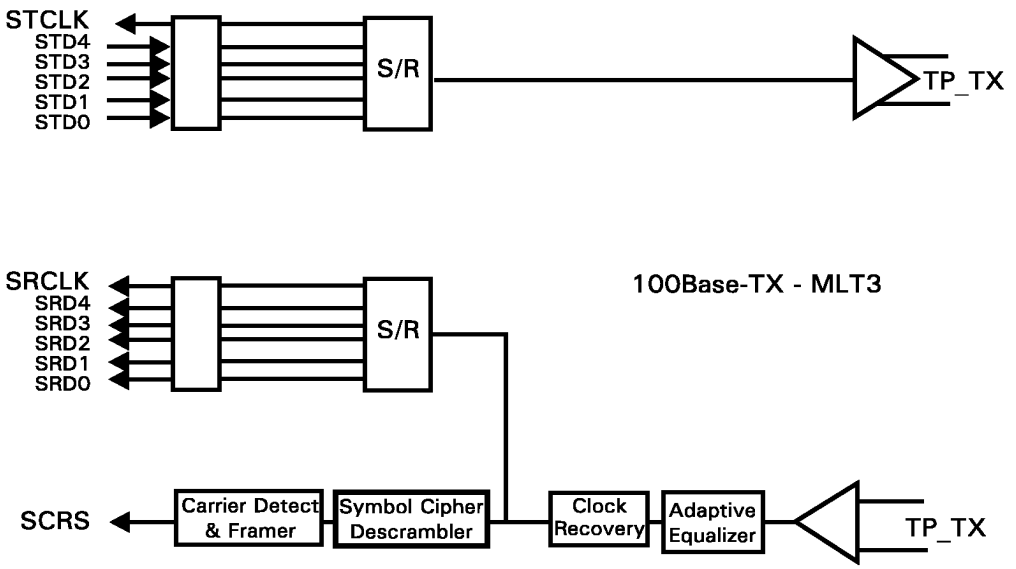
Carrier Sense **CRS**

The **ICS1891** asserts Carrier Sense (CRS) when it detects that the receive lines are non-idle. It is de-asserted when receive lines become idle. CRS is not synchronous to either the transmit or receive clocks.

Collision Detected **COL**

The **ICS1891** asserts Collision Detected (COL) when it detects a receive carrier (non-idle condition) while transmitting (TXEN asserted).

The non-idle condition is detected by two non-contiguous zeros in any 10-bit code group. COL is not synchronous to either the transmit or receive clocks.



5-Bit Symbol Interface

5-Bit Symbol Interface - Pin Mapping

When the **ICS1891** is operating in the symbol mode, the MII Data Interface is remapped to accommodate the 5-bit Symbol Interface. The following table details the exact pin mapping. Each individual pin description also contains the "new 5-bit Symbol Interface pseudo pin name" followed by the real MII Data Interface pin name that it is mapped onto.

MII	Symbol	Pin
TXCLK	STCLK	43
TXEN	(1)	44
TXER	STD4	42
TXD3	STD3	48
TXD2	STD2	47
TXD1	STD1	46
TXD0	STD0	45
RXCLK	SRCLK	37
RXDV	(2)	36
RXER	SRD4	38
RXD3	SRD3	32
RXD2	SRD2	33
RXD1	SRD1	34
RXD0	SRD0	35
CRS	SCRS	50
COL	(3)	49
LSTA	SD	21

(1) 100Base-TX is a continuous transmission system and the Repeater is responsible for sourcing IDLE symbols when it is not transmitting data when using the Stream Interface.

(2) Since data is not framed when this interface is used, RXDV has no meaning.

(3) Since the Repeater is responsible for sourcing both active and idle data, the PHY can not tell when it is transmitting in the traditional sense so collisions can not be detected.

Other mode configuration pins behave identically regardless of which data interface is used.

Transmit Clock **STCLK/(TXCLK)**
The Transmit Clock (STCLK) is a continuous clock signal generated by the **ICS1891** to synchronize the Transmit Data lines. The **ICS1891** clock frequency is 25 MHz.

Transmit Data 4 **STD4/(TXER)**
Transmit Data 4 (STD4) is the most significant bit and is sampled continuously by the **ICS1891** synchronously with the Transmit Clock.

Transmit Data 3 **STD3/(TXD3)**
Transmit Data 3 (STD3) is sampled continuously by the **ICS1891** synchronously with the Transmit Clock.

Transmit Data 2 **STD2/(TXD2)**
Transmit Data 2 (STD2) is sampled continuously by the **ICS1891** synchronously with the Transmit Data Clock.

Transmit Data 1 **STD1/(TXD1)**
Transmit Data 1 (STD1) is sampled continuously by the **ICS1891** synchronously with the Transmit Clock.

Transmit Data 0 **STD0/(TXD0)**
Transmit Data 0 (STD0) (the least significant bit) is sampled continuously by the **ICS1891** synchronously with the Transmit Clock.

Receive Clock **SRCLK/(RXCLK)**
The Receive Clock (SRCLK) is sourced by the **ICS1891**. There are two possible sources for the Receive Clock (SRCLK). When a carrier is present on the receive pair, the source is the recovered clock from the data stream. When no carrier is present on the receive pair, the source is the Transmit Clock (STCLK).

The Receive Clock frequency is always 25 MHz.

Receive Data 4 **SRD4/(RXER)**
Receive Error (SRD4) is the most significant bit of the receive data nibble and is continuously asserted by the **ICS1891**.

Receive Data 3 **SRD3/(RXD3)**
Receive Data 3 (SRD3) is continuously asserted by the **ICS1891**.

Receive Data 2 **SRD2/(RXD2)**
Receive Data 2 (SRD2) is continuously asserted by the **ICS1891**.

Receive Data 1 **SRD1/(RXD1)**
Receive Data 1 (SRD1) is continuously asserted by the **ICS1891**.

Receive Data 0 **SRD0/(RXD0)**
Receive Data 0 (SRD0) is the least significant bit of the receive data nibble.

Carrier Sense **SCRS/(CRS)**
Carrier Sense is provided in the 5-bit Symbol Interface mode as a fast receive carrier look-ahead for optional application use. Carrier is detected using the same circuitry used in the MII Data Interface mode that is "bypassed" in this mode.

The **ICS1891** asserts Carrier Sense (SCRS) when it detects that either the transmit or receive lines are non-idle in half duplex mode. It is de-asserted when both the transmit and receive lines are idle in half duplex mode. SCRS is not synchronous to either the transmit or receive clocks.

Signal Detect **SD/(LSTA)**
This signal is asserted when the PLL detects 100Base-T activity on the receive channel.

Twisted Pair Interface

Transmit Pair TP_TX+ & TP_TX-

The Transmit pair TP_TX+ and TP_TX- carries the serial bit stream for transmission over the UTP cable. The current-driven differential driver is programmed to produce a three-level (100Base-TX, MLT-3) signal. These output signals interface directly with an isolation transformer.

Note that these pins may be tristated using the TPTRI control pin.

Receive Pair TP_RX+ & TP_RX-

The Receive pair TP_RX+ and TP_RX- carries the serial bit stream from the mandatory isolation transformer. The serial bit stream is a three-level (100Base-TX, MLT-3) signal.

100M Transmit Current Set Resistor 100TCSR

A resistor is required to be connected between this pin and the nearest transmit ground to set the value of the transmit current used in 100M 5-bit symbol interface mode.

The value and tolerance of this resistor is specified in the Electricals section.

Clock Reference Interface

Frequency Reference (REF_IN)

This pin connects to a 25 MHz frequency reference source.

When a frequency reference source like a crystal oscillator module is used, its output should be connected to REF_IN.

Configuration and Status Interface

MII Data/Symbol Interface Select MII/SI

This input pin selects the MAC to PHY interface to be used. When the input is low the MII Data Interface is selected.

When the input is high, the 5-bit symbol Interface is selected. This provides a simple unframed 5-bit symbol interface with lower latency.

Invert Transmit Clock Latching Setting ITCLS~

The **ICS1891** allows transmit data to be latched relative to either TXCLK or REF_IN. Latching the data to TXCLK is the behavior specified in the 100Base-T MII specification, but in some applications it is desirable to latch data with the REF_IN clock. An example of where this might be beneficial is in a repeater application where all data transmission on multiple **ICS1891**s need to be synchronized to a common clock.

Select the setting of the ITCLS pin that latches the transmit data with the clock of your choice. The following table shows the possible combinations. This pin has an internal pull-up so it may be left not connected for some applications.

ITCLS	Latching Clock
0	TXCLK
1*	REF_IN

* Default if N/C.

TP_TX Tristate **TPTRI**

When this pin is set to a logic zero, the twisted pair transmitter output pins will be enabled normally to source 100Base-TX.

When this pin is set to a logic one, the twisted pair transmitter output pins will be tristated.

Repeater - PHY Receive Interface Tristate **RXTRI**

When this input is a logic zero the selected Repeater-PHY interface behaves normally.

When this input is a logic one, the RXCLK, RXD[3:0], RXER, and RXDV pins are tristated. This allows repeater designs to bus the shared receive lines without requiring extra tristatable buffers on each port. Note that the CRS and COL pins are not tristated. This allows repeater logic to use these signals to determine which receive port to enable.

Link Status **LSTA**

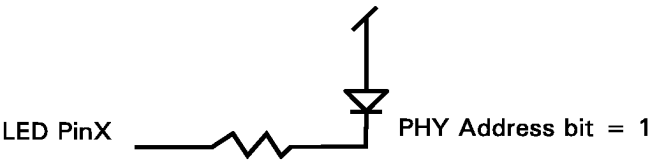
This output reflects the current Link Status. It is similar to bit (1:2) but changes dynamically instead of latching on a link failure. The output is low when the link is invalid and is high when a valid link has been established.

System Reset **RESET~**

When grounded, this pin causes the **ICS1891** to enter a reset/low power state. On the low to high transition of RESET, the device will begin to complete its reset cycle. Upon completion, the **ICS1891** will be initialized its default state.

LED Usage

The LED and current limiting resistor should be connected to the LED pin as shown below.



Resistor values should be in the range of 1kΩ to 10kΩ. A 1kΩ resistor is recommended.

Note: If LEDs are not required for the application, then a single resistor to VDD on *any one* of the LED pins is required. This will ensure proper operation of the **ICS1891**.

Link Integrity LED **LILED**

The **ICS1891** turns on this LED when the Link Integrity status is OK.

Collision LED **CLLED**

The **ICS1891** turns on this LED when a collision is detected. This signal is stretched to ensure that a single collision will be seen. If the collisions are continuous, the LED will appear permanently on.

Activity LED **ACLED**

The **ICS1891** turns on this LED when either transmit or receive activity is detected. This signal is stretched to ensure that a single activity event will be seen. If the activity is continuous, the LED will appear permanently on.

Power Supply

These 7 VDD and 8 VSS pins supply power to the **ICS1891** device.

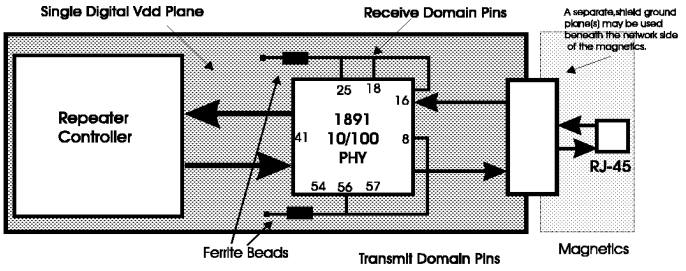
It is very important to properly isolate the **ICS1891** 10/100Base-TX Physical Layer Device from noise sources in a system design. There are two key areas to consider, isolation from digital noise and noise coupling between the transmitter and receiver.

Filtering for the **ICS1891** is accomplished by separating the power supply into three domains: digital, transmit and receive. All suppy pins on the device fall into one of these three categories as shown in the following table.

Digital Domain	Transmit Domain	Receive Domain
41 VDD 40 VSS	8 VDD 7 VSS	16 VDD 18 VDD 17 VSS
54 VDD 51 VSS	56 VDD 55 VSS	25 VDD 29 VSS
57 VDD 63 VSS	1 VDD	

In that table each supply pin is followed directly by its corresponding ground pin. Supply pins are shown paired up with their appropriate neighbor for bypass purposes. All ground pins are tied to a single ground plane. Each supply pair should be bypassed with a 0.1uF capacitor located as close to the device as possible.

The diagram below illustrates the supply isolation: A single Vdd plane with point-to-point trace routing the Digital Domain Vdd pins drop directly down to the single power plane while the Transmit and Receive Domain pins are isolated via point-to-point routing and inline ferrite beads.



Pin Descriptions

PIN NUMBER	PIN NAME	I/O	TYPE	DESCRIPTION
1	VDD[2]			Trasmit Domain Power (config.)
2	N/C[4]			
3	N/C			
4	100TCSR			100M Transmit Current Set Resistor
5	TP_TX+	O		Twisted Pair Transmit Data+
6	TP_TX-	O		Twisted Pair Transmit Data-
7	VSS			
8	VDD			Transmit Domain Power (Transmitter)
9	TPTRI	I	TTL-compatible	Twisted Pair Tristate
10	TP_RX+	I		Twisted Pair Receive Data+
11	TP_RX-	I		Twisted Pair Receive Data-
12	N/C			
13	ITCLS~	I	TTL-compatible	Invert Transmit Clock Latching Setting
14	N/C			
15	N/C			
16	VDD			Receive Domain Power (Receiver)
17	VSS			
18	VDD			Receive Domain Power (Receiver)
19	MII/SI	I	TTL-compatible	MII Data/Stream Interface
20	N/C			
21	LSTA*	O	TTL-compatible	Link Status
22	RESET~	I	TTL-compatible	System Reset
23	VSS			
24	N/C[5]			
25	VDD			Receive Domain Power (RPLL)
26	N/C			
27	N/C			
28	N/C[3]			
29	VSS			
30	N/C[3]			
31	N/C[3]			
32	RXD3[1]	O	TTL-compatible	Receive Data 3

NOTE:

[1] Redefined for 5-bit Symbol Interfaces.
[2] When replacing an **ICS1890** with an **ICS1891**, this pin must be V_{DD}.
[3] When using the **ICS1891** as a replacement for an **ICS1890** this pin may be V_{DD}, V_{SS}, or N/C. For new designs leave the pin N/C.
[4] When using the **ICS1891** as a replacement for an **ICS1890** this pin may be V_{DD} or N/C. For new designs leave the pin N/C.
[5] When using the **ICS1891** as a replacement for an **ICS1890** this pin may be V_{SS} or N/C. For new designs leave the pin N/C.

Pin Descriptions

PIN NUMBER	PIN NAME	I/O	TYPE	DESCRIPTION
33	RXD2[1]	O	TTL-compatible	Receive Data 2
34	RXD1[1]	O	TTL-compatible	Receive Data 1
35	RXD0[1]	O	TTL-compatible	Receive Data 0
36	RXDV[1]	O	TTL-compatible	Receive Data Valid
37	RXCLK[1]	O	TTL-compatible	Receive Clock
38	RXER	O	TTL-compatible	Receive Error
39	RXTRI	I	TTL-compatible	Receive MAC-PHY Interface Tristate
40	VSS			
41	VDD			Digital Domain Power
42	TXER[1]	I	TTL-compatible	Transmit Error
43	TXCLK[1]	O	TTL-compatible	Transmit Error
44	TXEN[1]	I	TTL-compatible	Transmit Enable
45	TXD0[1]	I	TTL-compatible	Transmit Data 0
46	TXD1[1]	I	TTL-compatible	Transmit Data 1
47	TXD2[1]	I	TTL-compatible	Transmit Data 2
48	TXD3[1]	I	TTL-compatible	Transmit Data 3
49	COL[1]	O	TTL-compatible	Collision Detect
50	CRS[1]	O	TTL-compatible	Carrier Sense
51	VSS			
52	N/C			
53	REF_IN	I		Frequency Reference Input
54	VDD			Digital Domain Power
55	VSS			
56	VDD			Transmit Domain Power (TPLL)
57	VDD			Digital Domain Power
58	ACLED[6]	O	LED	Activity LED
59	CLLED[6]	O	LED	Collision det LED
60	LILED[6]	O	LED	Link Integrity LED
61	N/C			
62	N/C			
63	VSS			
64	N/C[3]			

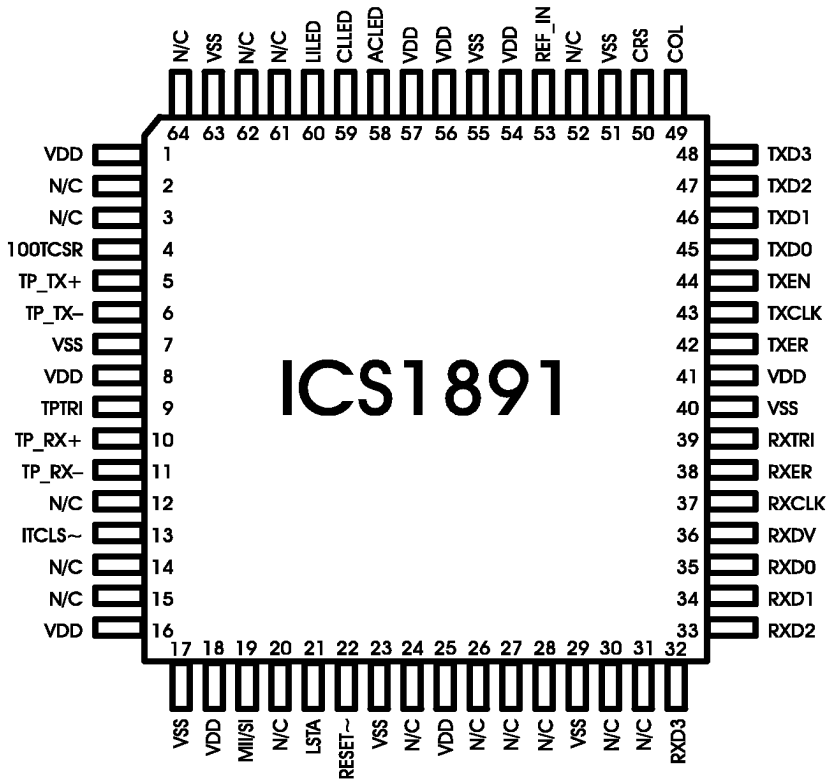
NOTE:

[1] Redefined for other PCS 5-bit symbol interfaces.

[3] When using the **ICS1891** as a replacement for an **ICS1890** this pin may be V_{DD}, V_{SS}, or N/C. For new designs leave the pin N/C.

[6] When replacing an **ICS1890** with an **ICS1891**, one of these three pins must be connected to an LED circuit or pull-up resistor as specified in the LED pin description section.

Pin Configuration



Absolute Maximum Ratings

V_{DD} (measured to V_{SS}) 7.0V
Digital Inputs/Outputs . . . . . V_{SS}-0.5 to V_{DD}+0.5V
Ambient Operating Temperature . . . . . 0 to 70° C
Storage Temperature. . . . . -65 to 150° C
Junction Temperature . . . . . 175° C
Soldering Temperature . . . . . 260° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Ambient Operating Temp.	TA		0	+70	°C
Power Supply	VSS VDD		0.0 +4.75	0.0 +5.25	V V

Recommended Component Values

PARAMETER	MIN	TYP	MAX	UNITS
Crystal Oscillator Frequency*	-50	25	+50	MHz ±ppm
100TCSR Resistor Value	-5%	6.81	+1%	KΩ
LED Resistor Value	1	1	10	KΩ

* CMOS output drive recommended

DC Characteristics

$V_{DD} = V_{MIN}$ to V_{MAX}, V_{SS} = OV, $T_A = T_{MIN}$ to T_{MAX}

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply Current	I_{DD}	V_{DD}=5.25V	-	195	mA

TTL Input/Output

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
TTL Input High Voltage	V_{IH}	VDD=5V, VSS=0V	2.0	-	V
TTL Input Low Voltage	V_{IL}	VDD=5V, VSS=0V	-	0.8	V
TTL Output High Voltage	V_{OH}	VDD=5V, VSS=0V	2.4	-	V
TTL Output Low Voltage	V_{OL}	VDD=5V, VSS=0V	-	0.4	V
TTL Driving CMOS, Output High Voltage	V_{OH}	VDD=5V, VSS=0V	3.68	-	V
TTL Driving CMOS, Output Low Voltage	V_{OL}	VDD=5V, VSS=0V	-	0.4	V
TTL/CMOS Output Sink Current	I_{OL}	VDD=5V, VSS=0V	8	-	mA
TTL/CMOS Output Source Current	I_{OH}	VDD=5V, VSS=0V	-	-0.4	mA

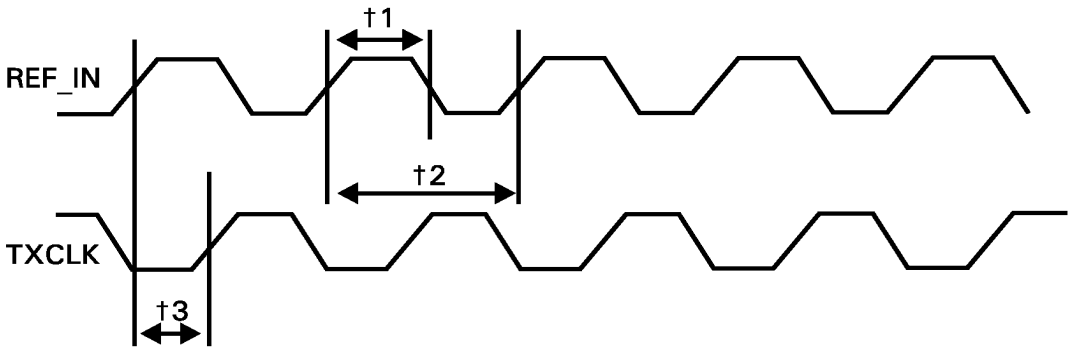
REF_IN Input

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{IH}	VDD=5V, VSS=0V	3.5	-	V
Input Low Voltage	V_{IL}	VDD=5V, VSS=0V	-	1.5	V

Note: REF_IN Input switch point is 50% of VDD.

PARAMETER (condition)	MIN	TYP	MAX	UNITS
MII Input Pin Capacitance	-	8	-	pF
MII Output Pin Capacitance	-	14	-	pF
MII Output Pin Impedance	-	38	-	Ohms

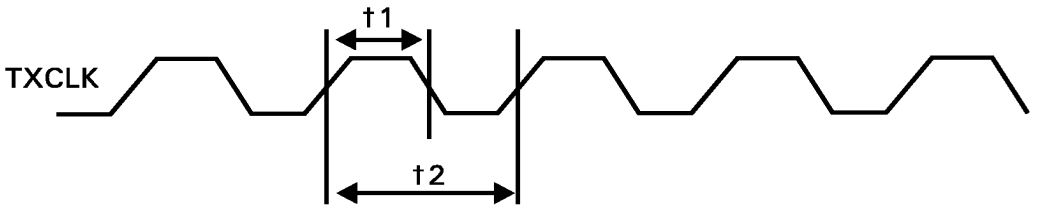
Clocks - Reference In (REF_IN)To Transmit Clock (TXCLK)



Note: REF_IN switching point is 50% of VDD.

T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	REF_IN Duty Cycle	40	50	60	%
t2	REF_IN Period	-	40	-	ns
t3	REF_IN rise to TXCLK rise	-	-	-	ns

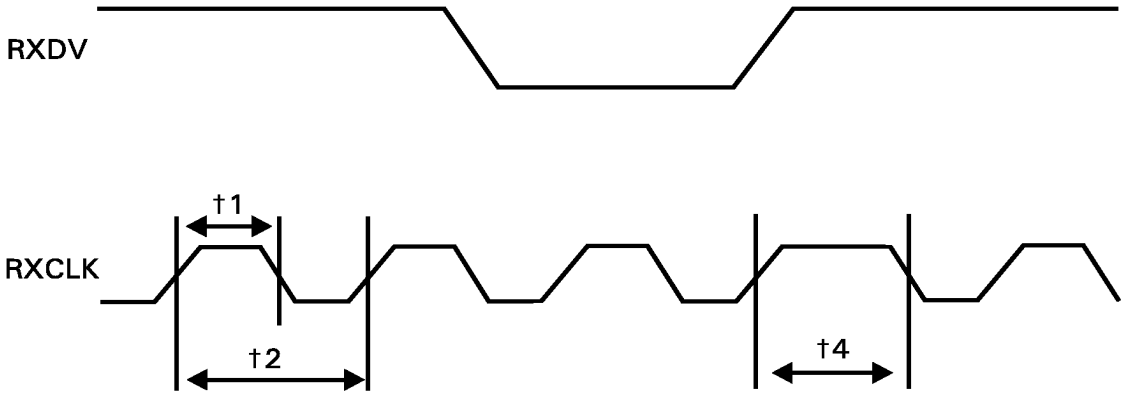
MII -Transmit Clock Tolerance



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TXCLK Duty Cycle	35	50	65	%
t2a	TXCLK Period (100Base-T/MII Interface)	-	40	-	ns

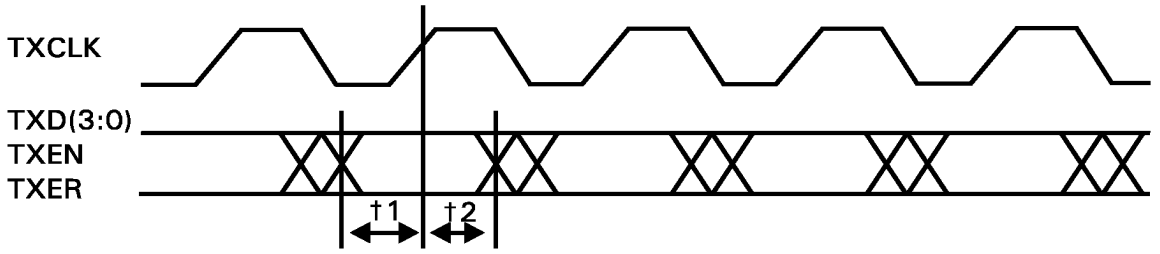
Note: TXCLK Duty Cycle = REF_IN Duty Cycle ±5%.

MII - Receive Clock Behavior



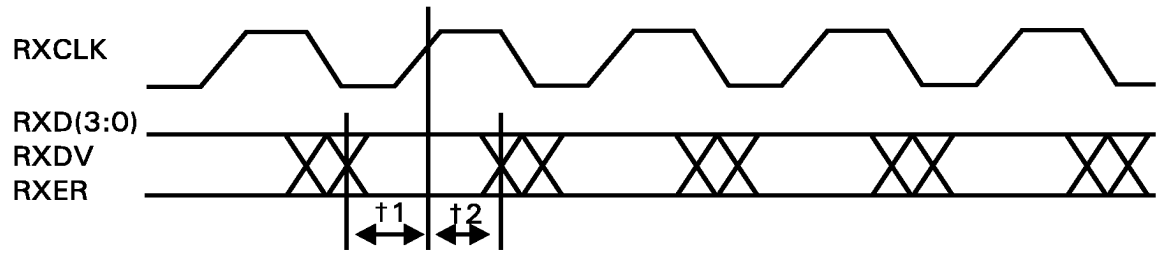
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	RXCLK Duty Cycle	45	50	55	%
t2a	RXCLK Period (100Base-T/MII Interface)	-	40	-	ns
t3	RXDV De-asserted Recovered Clock to Nominal Clock Cycle Extension (No Extension)	-	-	-	-
t4	RXDV Asserted Nominal Clock to Recovered Clock Cycle Extension	-	-	65	ns

MII/5-Bit Symbol Interface - Synchronous Transmit Timing



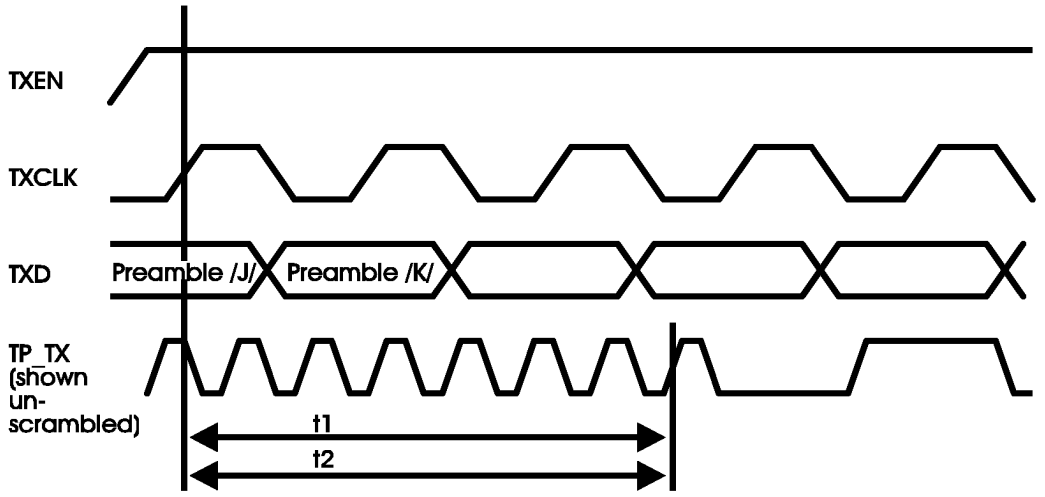
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TXD, TXEN, TXER Setup to TXCLK rise	10	-	-	ns
t2	TXD, TXEN, TXER Hold after TXCLK rise	0	-	-	ns

MII/5-Bit Symbol Interface - Synchronous Receive Timing



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	RXD, RXDV, RXER Setup to RXCLK rise	13.0	-	-	ns
t2	RXD, RXDV, RXER Hold after RXCLK rise	12.5	-	-	ns

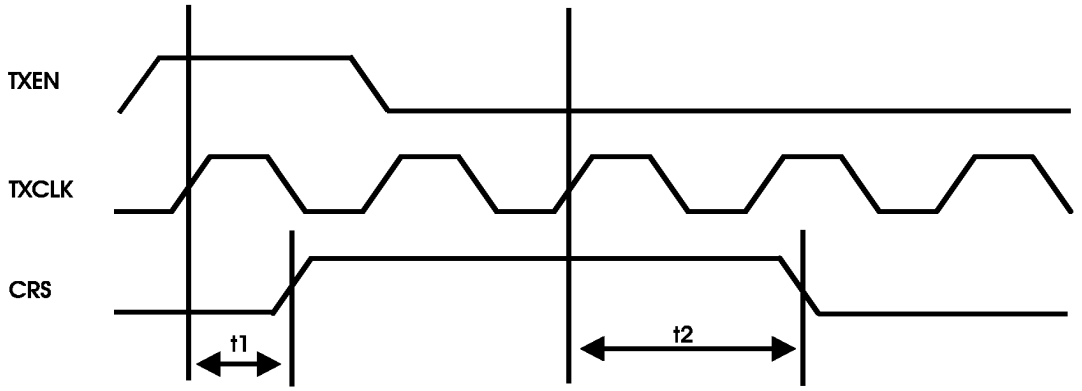
Transmit Latency (MII/5-Bit Symbol Interface)



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TXEN sampled to MDI Output 1st bit of /J/ (MII IF)*	-	-	38nS/4BT	
t2	TXD sampled to MDI Output of 1st bit (100M Stream IF)	-	-	5	bits

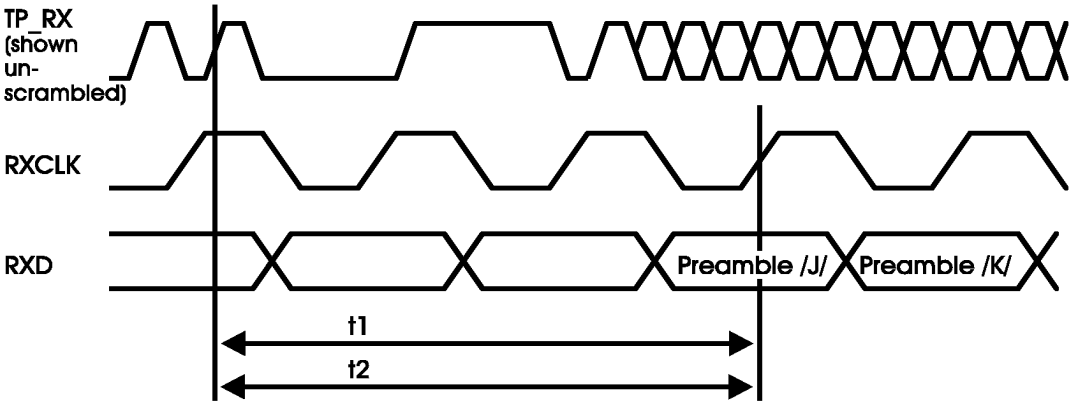
* Note that the IEEE maximum is 18 bits.

MII - Carrier Assertion/De-assertion on Transmission



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	TXEN sampled to CRS assert	0	-	4	bits
t2	TXD sampled to CRS de-assert	0	-	4	bits

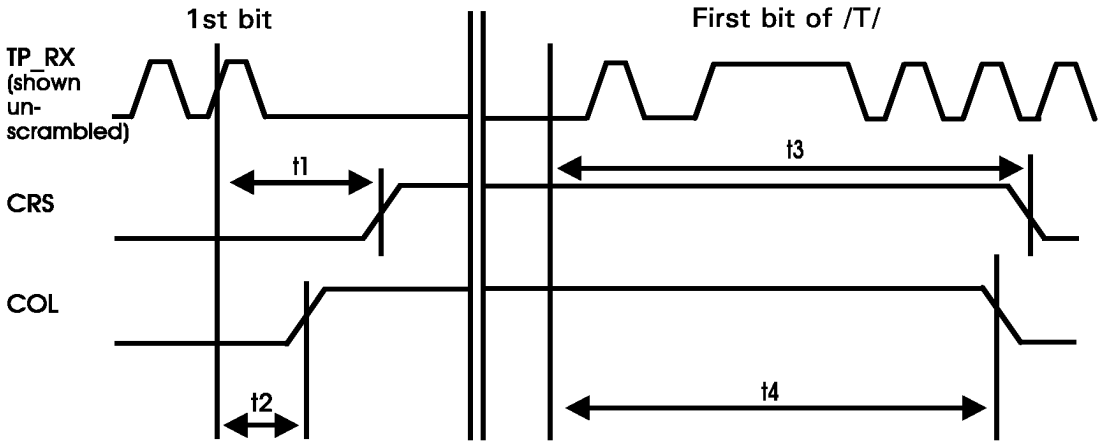
MII - Receive Latency (MII/5-Bit Symbol Interface)



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	1st bit of /J/ into TP_RX to /J/ on RXD (MII IF)	-	-	189nS/19BT	
t2	1st bit of /J/ into TP_RX to /J/ on RXD (5-Bit Symbol IF)	-	-	12.5	bits

* Note that the IEEE maximum is 23 bits.

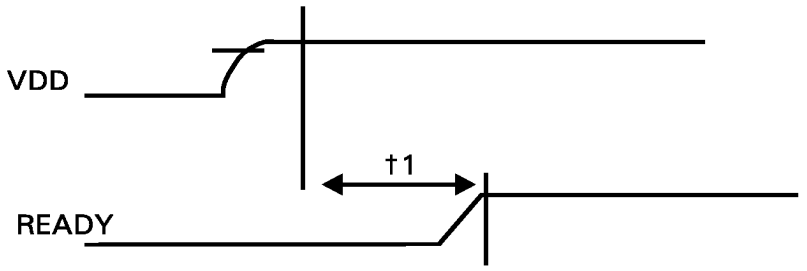
MDI Input to Carrier Assertion/De-assertion



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	1st bit of /J/ into TP_RX to CRS assert*	-	-	124ns/13BT	
t2	1st bit of /J/ into TP_RX while transmitting data to COL assert (Half Duplex Mode)*	-	-	13	bits
t3	First bit of /T/ into TP_RX to CRS de-assert**	-	-	130ns/13BT	
t4	First bit of /T/ received into TP_RX to COL de-assert (Half Duplex Mode)**	-	-	14	bits

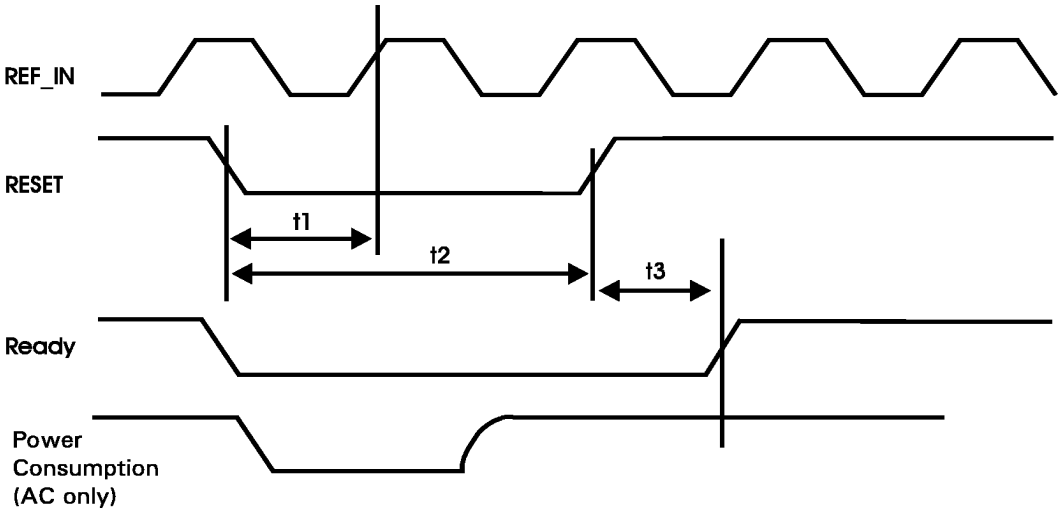
* Note that the IEEE maximum is 20 bit times.

Reset - Power on Reset

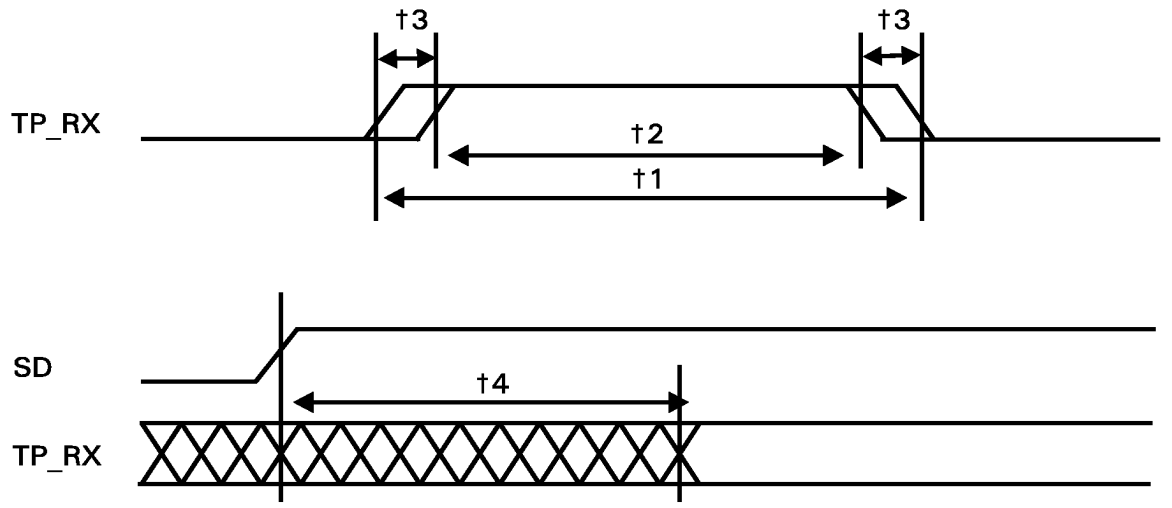


T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	VDD to 4V to Reset Complete	-	-	20	µs

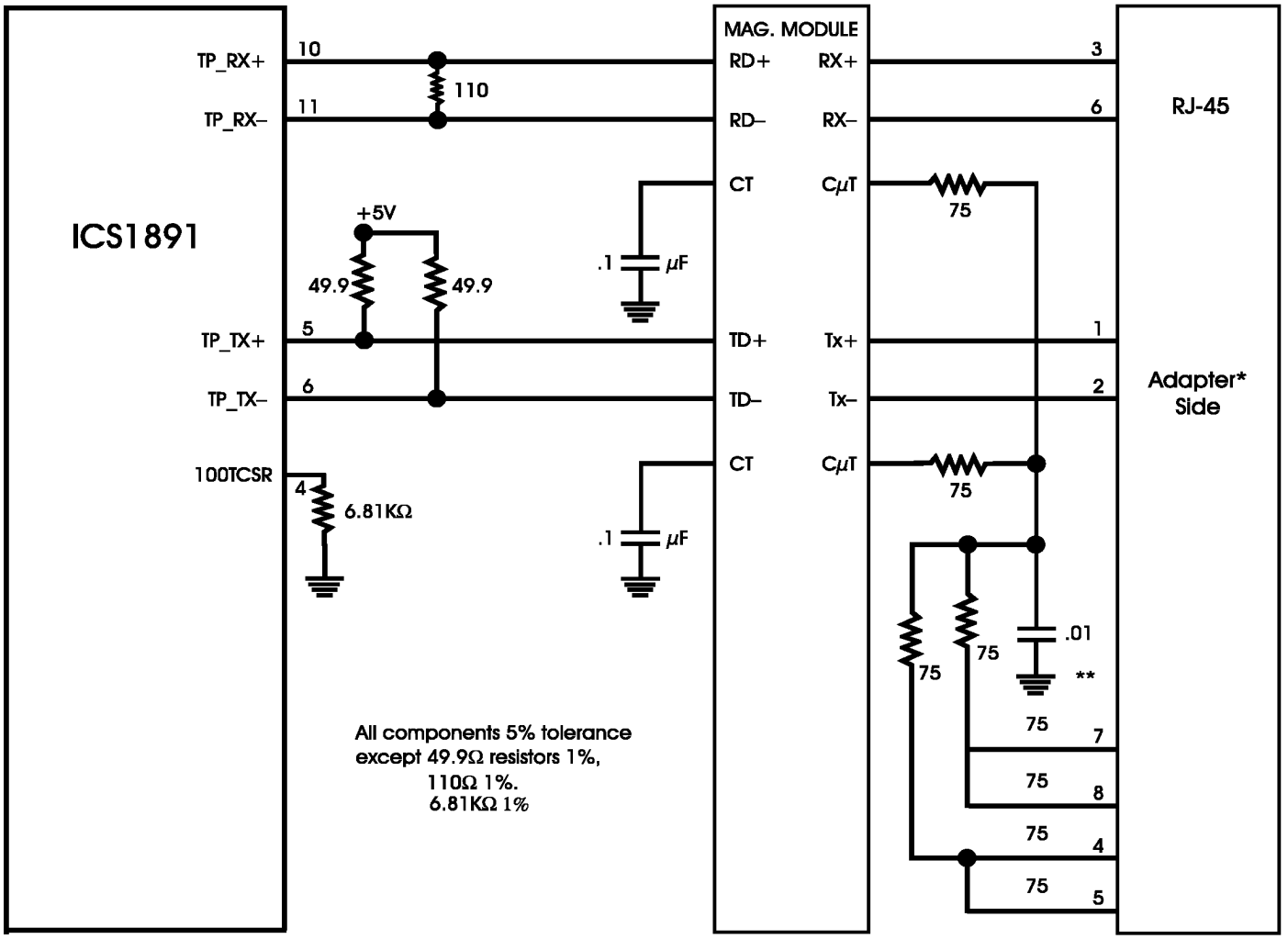
Reset - Hardware Reset & Power-down



T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	RESET active to device isolation and initialization	-	-	200	ns
t2	Minimum RESET pulse width	80	-	-	ns
t3	RESET released to device ready	-	-	640	ns



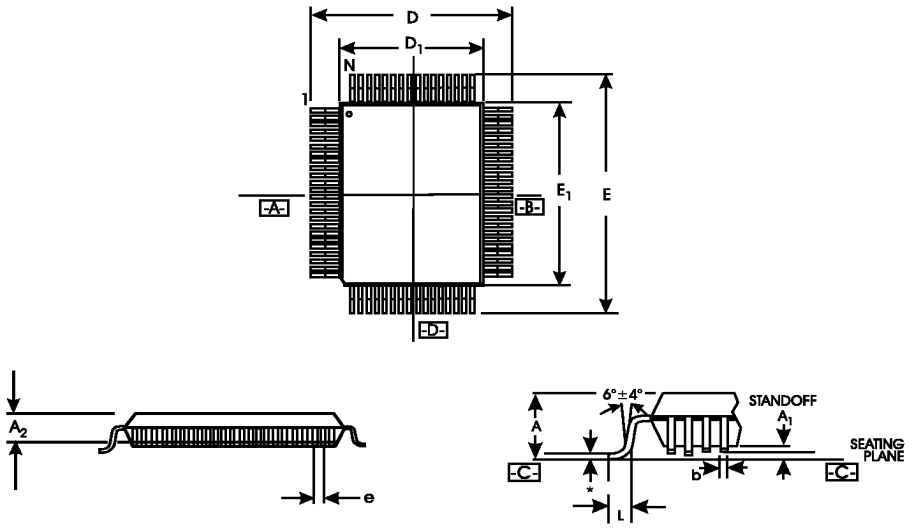
T#	PARAMETER (condition)	MIN	TYP	MAX	UNITS
t1	Ideal data recovery window	-	-	8	ns
t2	Actual data recovery window	6	-	8	ns
t3	Data recovery window truncation	0	-	1	ns
t4	SD assert to data acquired	-	-	100	ns



PRELIMINARY - SUBJECT TO CHANGE

* Repeaters and Hubs are generally responsible for including a cable crossover. One way of doing this is to exchange transmit (1 & 2) and receive (3 & 6) connections to the RJ-45.

**A minimum of 2kV capacitor should be used to make the connection to the chasis ground to meet isolation requirements.



QFP Package

DIMENSION NAME	LEAD COUNT (N)		64L
	BODY THICKNESS Nominal		1.4 - 2.7
	FOOTPRINT (BODY+) Nominal		3.20
	DIMENSIONS	TOLERANCE	
Full Package Height	A	MAX.	3.00
Package Standoff	A_1	MAX.	0.25
Package Thickness	A_2	+0.10/-0.05	1.4 - 2.7
Tip-to-Tip Width	D	±0.25	17.20
Body Width	D_1	±0.10	14.00
Tip-to-Tip Width	E	±0.25	17.20
Body Width	E1	±0.10	14.00
Footlength	L	+0.10/-0.10	0.88
Lead Pitch	e	BASIC	0. 80
Lead Width w/Plate	B	+0.10/-0.05	0.35
Lead Height w/Plate	*	MAX.	0.23

Dimensions in millimeters.

Ordering Information

ICS1891

Example:

ICS XXXXY

Package Type
Y=QFP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.