

HFD3020-002/XXX

TTL Output Receiver

FEATURES

- Converts fiber optic input signals to TTL digital outputs
- Typical sensitivity 500 nW peak (-33 dBm)
- Wide variety of cable options, operates with 50/125, 62.5/125, and 100/140 μ m cables
- Edge detection circuitry gives 20 dB minimum dynamic range, low Pulse Width Distortion
- Operates up to 10 Mbps NRZ
- Designed to operate with Honeywell 850 nm LEDs
- Single 5 V supply requirement
- Wave solderable
- Mounting options
 - SMA single hole
 - ST single hole
 - SMA PCB
 - ST PCB
 - SMA 4 hole

DESCRIPTION

The HFD3020-002/XXX is a sensitive differentiating optical receiver designed for use in short distance, 850 nm fiber optic systems. The receiver uses a hybrid construction consisting of a PIN photodiode, bipolar integrated receiver circuit with internal voltage regulation and external bypass capacitor. The TTL output allows the HFD3020-002/XXX to be interfaced directly with standard TTL circuits.

APPLICATION

Digital HFD3020-002/XXX fiber optic receivers convert the optical signal in a point to point data communications fiber optic link to a TTL output. The HFD3020-002/XXX consists of a base fiber optic component (HFD3020) which is mounted in a fiber optic connector.

Electrical isolation is important in obtaining the maximum performance of this high sensitivity receiver. A 0.1 μ F ceramic capacitor must be connected between pin #1 and pin #4. This minimizes external noise on the power leads. Shielding can reduce coupled noise and allow the maximum sensitivity to be obtained. This can include the use of ground planes in the PCB, shielding around the device, and shielding around the leads. The specified maximum operating temperature of 100°C allows the HFD3020-002/XXX to be designed into a broad variety of applications.

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APPLICATION (continued)

Honeywell also offers companion transmitters designed to operate in conjunction with the HFD3020-002/XXX.

Optical power (photons) from the fiber strikes the photodiode and is converted to electrical current. This current is then converted into a voltage in the transimpedance preamplifier. The postamplifier is a voltage gain stage with excellent temperature tracking. The edge detection circuit includes an operational amplifier configured as a differentiator, whose output is proportional to the rate of change of the optical signal. A latch retains the most recent edge transition and an inverting buffer drives the TTL output. For example, a light On to light Off transition of the input produces a TTL high output logic level.

Bandwidth has been limited to minimize noise problems. Reduced pulse width distortion (PWD) is a by-product of the bandwidth limitation. The output of the differentiator has a fixed settling time, assuring good PWD in most applications. Another effect of fixed settling time is the increase of PWD with increased optical power. Very high input optical power may overdrive the differentiator, causing high PWD due to the settling time. The accompanying curves illustrate how PWD increases with increased optical power, increased temperature, and decreased duty cycle.

PWD manifests itself as an increase in the width of the TTL low portion of an output waveform, with the TTL high portion decreasing by a like amount. The amount of PWD that a given system can tolerate without an error due to a missing bit of information, is dependant upon system considerations. The output of the HFD3020-002/XXX will typically connect to the input of some form of a Serial Interface Adaptor IC. The specifications for that IC govern the amount of PWD that can be tolerated in that system.

The edge detection circuit monitors the output of the differentiator, and triggers when its output exceeds preset levels. These levels are established to be sufficiently above the worst case RMS noise level to allow excellent bit error rate and are low enough to give high sensitivities which permit operation over long link lengths. This circuitry recognizes the polarity of the change of the optical signal, setting the latch to a "1" when the optical input decreases.

Note: the final output stage inverts the polarity. When initially powered up, the output state is set to a "1". After setting of the device occurs, incoming edge transitions are recognized and logic switching occurs.

Because the HFD3020-002/XXX reacts to transitions in the optical signal rather than DC levels, it shows excellent stability versus temperature and other operating conditions. Also, the device is much less sensitive to the absolute level of the optical signal than DC coupled receivers, allowing for a large range of optical source powers and/or link distances to be directly interfaced.

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ELECTRO-OPTICAL CHARACTERISTICS ($V_{CC} = 5.0$ VDC, $T_C = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Minimum Input Sensitivity	P_{IN} (Peak)		0.5	1.0	μW	$f = 2.5$ MHz, 100 μm core fiber $\lambda = 850$ nm, Duty Cycle = 50%
High Level Logic Output Voltage	V_{OH}	2.4	3.3		V	$P_{IN} \leq 0.1$ μW , $I_O \leq 0.8$ mA
Low Level Logic Output Voltage	V_{OL}			0.4	V	$P_{IN} \geq 1.0$ μW , $I_O \leq 0.8$ mA
Power Supply Current	I_{CC}		15	20	mA	$P_{IN} \geq 1.0$ μW , $V_{CC} = 5$ V
Rise/Fall Time	t_R		12		ns	$P_{IN} = 1.0$ μW peak $\lambda = 850$ nm
	t_F		3		ns	
Pulse Width Distortion	PWD				%	$f = 2.5$ MHz, Duty Cycle = 50%
			5	10		$P_{IN} = 1.0$ μW peak
			20	25		$P_{IN} = 100$ μW peak

ABSOLUTE MAXIMUM RATINGS

($T_{Case} = 25^\circ\text{C}$ unless otherwise noted)

Storage temperature -40 to $+100^\circ\text{C}$

Operating temperature -40 to $+100^\circ\text{C}$

Lead solder temperature 260°C for 10 s

Junction temperature 150°C

Supply voltage $+6.0$ V

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Operating temperature -40 to $+85^\circ\text{C}$

Supply voltage $+4.5$ to $+5.5$ V

Optical input power 1.0 to 100 μW

Input signal pulse width > 100 ns

Optical signal edges (10 to 90%) < 20 ns

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ORDER GUIDE

Description	Catalog Listing
Fiber Optic TTL Receiver	HFD3020-002/XXX

MOUNTING OPTIONS

Substitute XXX with one of the following 3 letter combinations

SMA single hole	- AAA
ST single hole	- BAA
SMA PCB	- ABA
ST PCB	- BBA
SMA 4 hole	- ADA

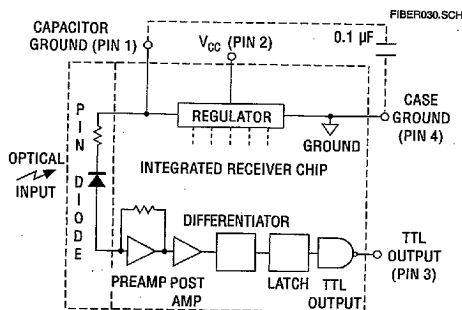
Dimensions on page 441

CAUTION

The inherent design of this component causes it to be sensitive to electrostatic discharge (ESD). To prevent ESD-induced damage and/or degradation to equipment, take normal ESD precautions when handling this product.



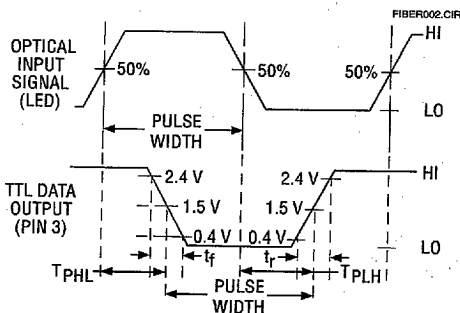
BLOCK DIAGRAM



FIBER INTERFACE

Honeywell detectors are designed to interface with multimode fibers with sizes (core/cladding diameters) ranging from 50/125 to 200/230 microns. Honeywell performs final tests using 100/140 micron core fiber. The fiber chosen by the end user will depend upon a number of application issues (distance, link budget, cable attenuation, splice attenuation, and safety margin). The 50/125 and 62.5/125 micron fibers have the advantages of high bandwidth and low cost, making them ideal for higher bandwidth installations. The use of 100/140 and 200/230 micron core fibers results in greater power being coupled by the transmitter, making it easier to splice or connect in bulkhead areas. Optical cables can be purchased from a number of sources.

SWITCHING WAVEFORM



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Fig. 1 Pulse Width Distortion vs Temperature

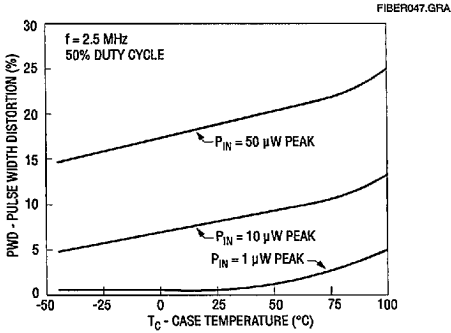


Fig. 2 Pulse Width Distortion vs Frequency

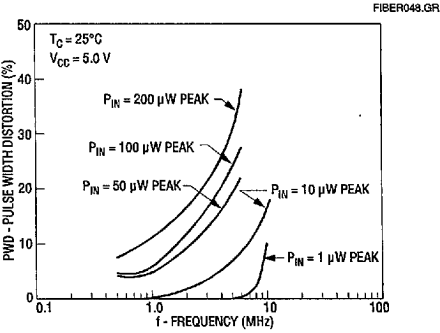


Fig. 3 Pulse Width Distortion vs Optical Input Power

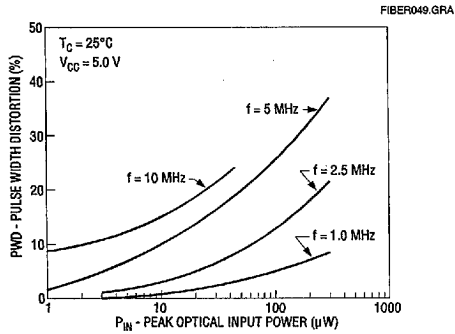


Fig. 4 Propagation Delay vs Optical Input Power

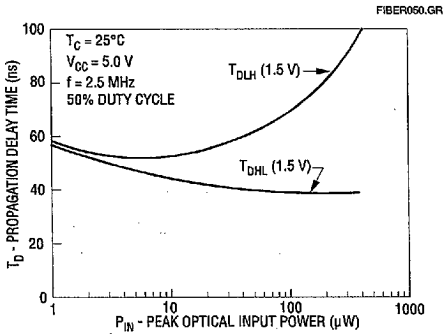


Fig. 5 Supply Current vs Temperature

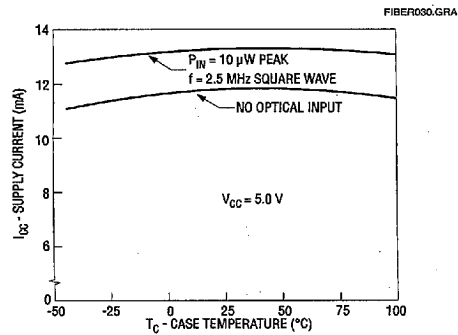
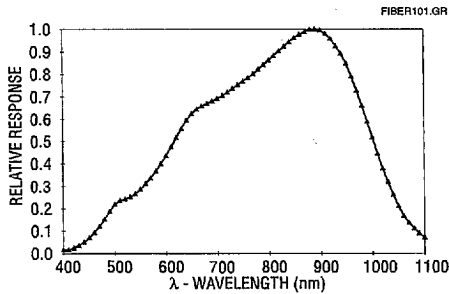


Fig. 6 Spectral Responsivity



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