HUGHES
SOLID STATE PRODUCTS
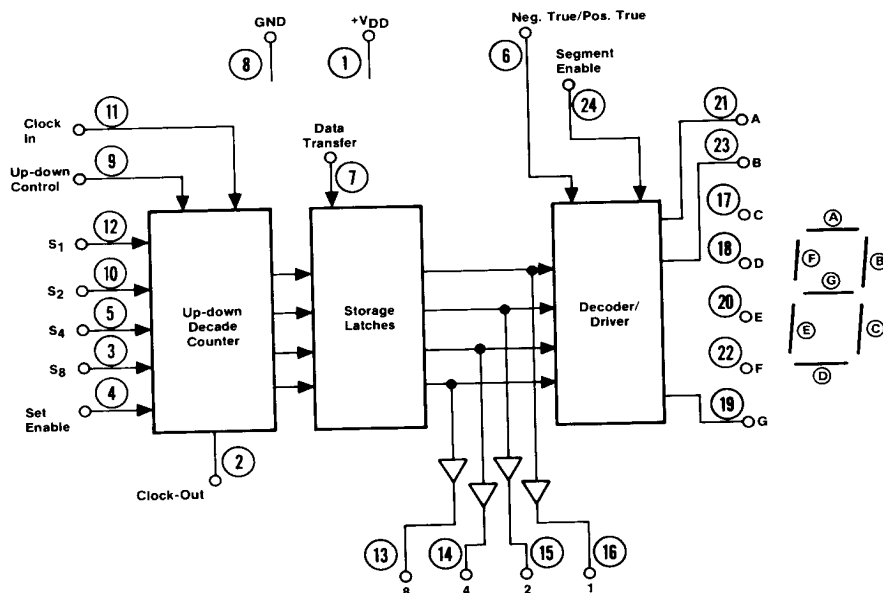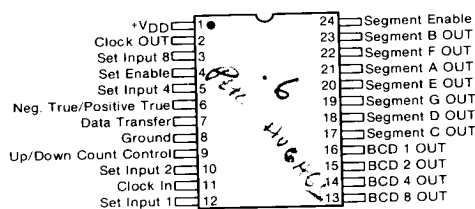
C MOS Decade Counter/ Latch/Decoder/Driver

HCTR 0200D/
HCTR 0200P

DESCRIPTION

The Hughes HCTR 0200 Decade Counter/Latch/Decoder/Driver is a TTL compatible, Positive True Logic circuit for driving 7 segment light emitting diode displays, liquid crystal displays, incandescent displays and bipolar transistor base currents. A modified version for driving electroluminescent tubes is also available by special order.

The HCTR 0200 is an up-down, presettable, decade counter with storage latches which hold the BCD state of the counter on command. The stored information appears in numeric form at the seven segment driver outputs.

FEATURES

- 7 Segment outputs drive LED's directly without Bipolar interface
- Up-down presettable BCD Counter
- Count Independent Storage Latches
- All inputs TTL compatible
- Low Power Dissipation
- Units may be cascaded
- BCD and Clock Outputs will drive one worst case TTL load
- All inputs static charge protected.

TERMINAL CONNECTIONS

Pin	Name	Pin	Name
1	+VDD	24	Segment Enable
2	Clock OUT	23	Segment B OUT
3	Set Input 8	22	Segment F OUT
4	Set Enable	21	Segment A OUT
5	Set Input 4	20	Segment E OUT
6	Neg. True/Positive True	19	Segment G OUT
7	Data Transfer	18	Segment D OUT
8	Ground	17	Segment C OUT
9	Up/Down Count Control	16	BCD 1 OUT
10	Set Input 2	15	BCD 2 OUT
11	Clock In	14	BCD 4 OUT
12	Set Input 1	13	BCD 8 OUT

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ELECTRICAL CHARACTERISTICS OVER
FULL TEMPERATURE VARIATIONS

CHARACTERISTICS	CONDITIONS	TYPICAL VALUES			UNITS
		MIN	TYP	MAX	
Operating Voltage, V_{DD}		2	5	10	V
All Inputs	(All following at +V_{DD} = 5V unless otherwise stated)				
Logic "High", V_{INH}		2.4		5	V
Logic "Low", V_{INL}		GND		1.0	V
Capacitance	V_{in} = 0, F_{in} = MHz		3		PF
Input Leakage, I_I				1.0	A
Set Enable Pulse, T_{SEH} Width		200			nS
Data Transfer Pulse, T_{DXH} Width		250			nS
Set Input Valid Time, T_{SIH}		200			nS
Necessary Delay from Count Control change to Positive Clock Transition		400			nS
Clock Input					
Clock Frequency, F_{MAX}		2			MHz
Rise, Fall Times, $T_{r,f}$				200	nS
Pulse Width in "High", T_{CLPW} State or "Low" State		250			nS
Clock Output					
Logic "High", V_{OCH}	I_L = 200 μA	4		5	V
Logic "Low", V_{OCL}	I_L = 1.6 mA	GND		0.4	V
BCD Outputs					
Logic "High", V_{OH}	I_L = -200 μA	4		5	V
Logic "Low", V_{OL}	I_L = 1.6 mA	GND		0.4	V
Display Outputs					
Logic "High" (Source), V_{ODH}	I_L = -1 mA	4.5	4.8*		V
Logic "Low" (Sink), V_{ODL}	I_L = 2 mA	0.5	0.2*		V
Logic "High" (Source), V_{ODH}	I_L = -1.5 mA	9.5	9.8*		V
Logic "Low" (Sink), V_{ODL}	I_L = 3mA	0.5	0.2*		V

*At 25° C

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For driving electroluminescent displays a special mask option is available which will modify the circuit to provide single ended segment output drivers for interfacing with high-voltage electroluminescent tubes.

An option for a 16 Pin package is available. The 16 Pin version is similar to the 24 Pin version except that the BCD OUTPUTS and SET INPUTS are not bonded out. In this version, the SET ENABLE input becomes a RESET input. Other bonding options, with even fewer pins are feasible.

The chip contains an additional power input pad which is not bonded out in the Standard 24 Pin version. The additional power input permits TTL compatible BCD OUTPUTS while operating the segment outputs at voltages higher than the standard TTL 5V supply voltage. Bonding out the additional power input pads can be done by eliminating (i.e. not bonding out) one of the standard pin functions and bonding out the additional power input instead. (Note: This may require a different pin — out for the other pins.)

TYPICAL TIMING DIAGRAM

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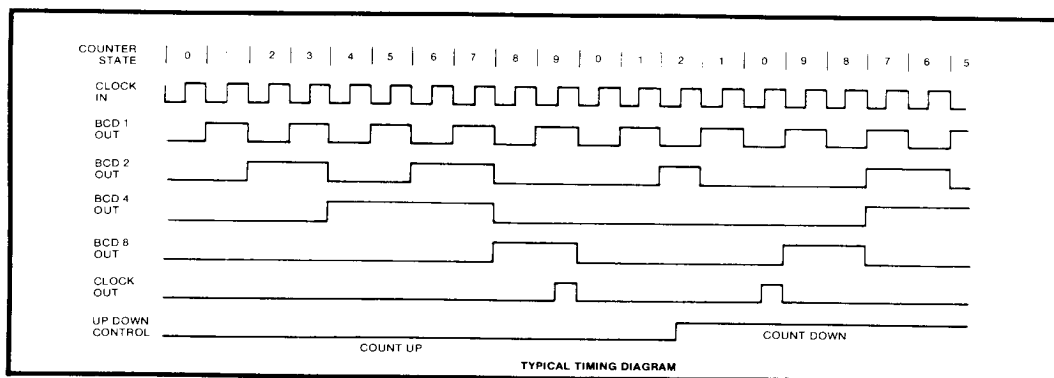
MAXIMUM RATINGS

Voltage, any pin (+V_{DD} = 5V)	+5.3 to -10.0V
Power Dissipation	350 mw
Operating Temperature	0° C to +70° C
Storage Temperature	-65° C to +125° C

NOTE: These ratings are limiting values above which the serviceability of the device may be impaired.

PACKAGES

24 Pin Ceramic DIP (HCTR 0200D)
24 Pin Plastic DIP (HCTR 0200P)

OPERATING NOTES

PRESETTING

When the Set Enable is a "high" the clock input is disabled and the flip-flops in the counter are set by the Set Inputs (S_1, S_2, S_4, S_8). When the Set Input is "low", the Set Inputs are disabled and the counter is enabled to respond to pulses on the Clock In input.

DATA TRANSFER:

When the Data Transfer is a "high", the storage flip-flops and all outputs follow the count. When a "low" input is applied, the storage flip-flops lock up at the last count without interrupting the counter. The outputs will not change until this goes in a "high".

CLOCK IN:

The flip-flops toggle on the falling (High to Low) edge of CLOCK IN.

CLOCK OUT:

When counting up and the count of "9" is reached, the next clock pulse in generates a CLOCK OUT pulse having the same width as the input pulse. When counting down, and the count of "0" is reached, the next clock pulse in generates a CLOCK OUT pulse. When cascading counters, connect the CLOCK OUT terminal to the CLOCK IN terminal of the following counter.

SET INPUTS:

The Set Inputs are positive true logic. Refer to presetting note.

UP-DOWN CONTROL:

The Up-Down Count Control determines the operating mode.

UP   = Logic "low"
DOWN   = Logic "high"

NOTE: For cascaded counters, the Up-Down Count Control should not be changed when the CLOCK-IN is "high".

BCD OUTPUTS:

The BCD outputs are positive true logic. Each BCD output can drive one standard power TTL load.
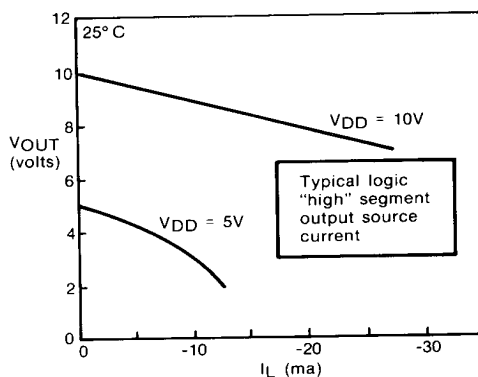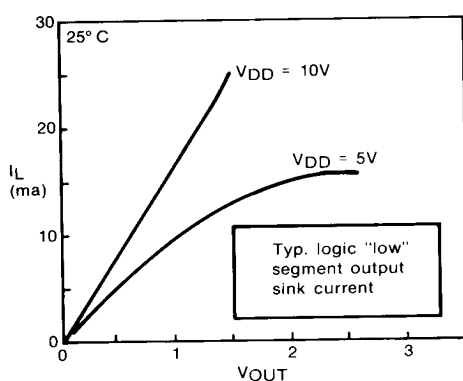
7-SEGMENT OUTPUTS:

The 7-Segment Outputs form numbers by connecting the outputs to the appropriate decoder driver outputs. The "true" state of the segment outputs is controlled by the NEGATIVE TRUE/POSITIVE TRUE input as follows:

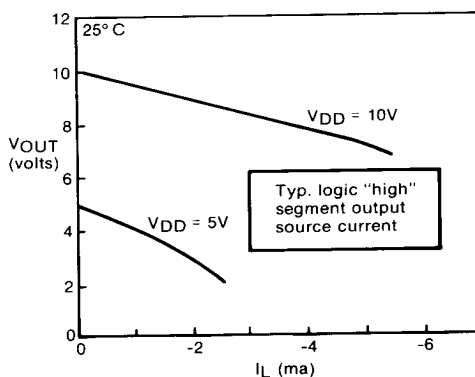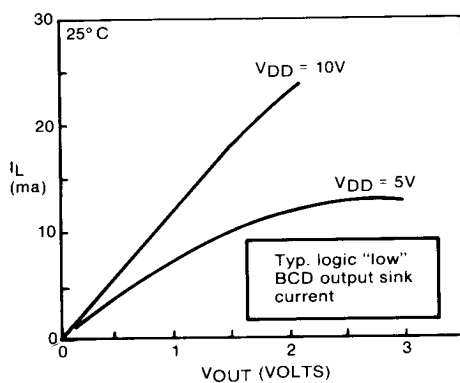| NEGATIVE TRUE/ POSITIVE TRUE Input	7-Segment Output "True" State
"low"	"high" (Low impedance to +V_{DD})
"high"	"low" (Low impedance to GROUND)

A logic "low" on the SEGMENT ENABLE input will cause the SEGMENT OUTPUTS to "float" i.e. all segment outputs will have a high impedance to V_{DD} and to GROUND. The high impedance "float" state is independent of the NEGATIVE TRUE/POSITIVE TRUE input. A logic "high" on the SEGMENT ENABLE will allow the decoder segment driver outputs to operate in the low impedance driver mode.

For Liquid Crystal Displays, requiring AC drive signals, the NEGATIVE TRUE/POSITIVE TRUE input can be driven with the back plane signal.

HCTR 0200 TYPICAL SEGMENT OUTPUT CHARACTERISTICS

25° C
V_{DD} = 10V
V_{DD} = 5V
I_L (ma)
Typ. logic "low" segment output sink current
V_{OUT}

25° C
V_{DD} = 10V
V_{DD} = 5V
V_{OUT} (volts)
Typical logic "high" segment output source current
I_L (ma)

HCTR 0200 TYPICAL BCD OUTPUT CHARACTERISTICS

25° C
V_{DD} = 10V
V_{DD} = 5V
I_L (ma)
Typ. logic "low" BCD output sink current
V_{OUT} (VOLTS)

25° C
V_{DD} = 10V
V_{DD} = 5V
V_{OUT} (volts)
Typ. logic "high" segment output source current
I_L (ma)

Represented By

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