SONY CXB1541Q-Y

Hex 2 : 1 Multiplexer with D-F.F.

Description

The CXB1541Q-Y is an ultra high speed monolithic ECL IC, which contains six 2 : 1 multiplexers followed by D type flip flops. The data select (SEL) input determines which data is enabled. The selected data is transferred to the flip flops output by the positive transition of clock (C1,C2) inputs. The Master Reset (MR) overrides all other control inputs and turns Q outputs to LOW.

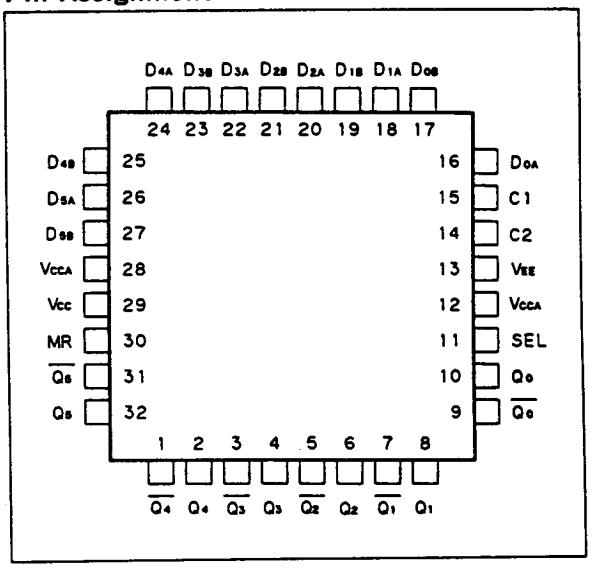
Features

- Typical clock rate up to 2.3 GHz
- Differential outputs
- Internal pull down resistors or input pins to maintain logic LOW level with the pins lest open.
- ECL 100K compatible I/O levels

Pin Names

D_{nA}, D_{nB}	Data inputs
Qn, $\overline{Qn}$	Data outputs
SEL	Data select input
Cn	Clock inputs
MR	Direct Master Reset input
V_{CC}	Circuit ground
V_{CCA}	Circuit ground for outputs
V_{EE}	Negative power supply

Pin Assignment



Truth Table

Select input	Outputs
SEL	Qn
L	D_{nA}
H	D_{nB}

Note : H ; HIGH voltage level
L ; LOW voltage level

DC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}		−196	−144	−100	mA

AC Characteristics

$V_{EE}=-4.5V\pm0.3V$, $V_{CC}=V_{CCA}=GND$, $V_{TT}=-2.0V$, $T_C=0°C$ to $+85°C$, $R_T=50\Omega$ to V_{TT}

Item	Symbol	Input	Output	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time	T_{PLH}	Cn	Qn		650	920	1230	ps
	T_{PHL}				670	950	1270	
	T_{PLH}	MR			780	1100	1470	
	T_{PHL}				780	1100	1470	
Gate-to-Gate skew	T_{SG-G}	Cn				100	200	
Set up time	Ts	D, Cn			100			
		SEL, Cn			300			
Hold time	Th	Cn, D			150			
		Cn, SEL			−50			
Release time	T_R	MR, Cn			340			
Min. Pulse width	T_{PW}	MR			610			
Max. Clock frequency	f_{MAX}	Cn			1.6	2.3		GHz
Rise time	T_{TLH}			20% to 80%		370	520	ps
Fall time	T_{THL}					340	480	

Block Diagram