Field programmable logic array (18 × 42 × 10) — 82S153A (PLS153A)

DESCRIPTION

The 82S153A is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 directional control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I,B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The 82S153A is field programmable, enabling the use to quickly generate custom patterns using standard programming equipment.

FEATURES

- Field-Programmable (Ni-Cr links)
- 8 inputs
- 42 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active-High or -Low outputs
- 42 Product Terms:
  - 32 Logic Terms
  - 10 Control Terms
- I/O propagation delay: 42ns (max)
- Input loading: -150μA (max)
- Power dissipation: 650mW (typ.)
- 3-State outputs
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A^* B^* C^* D^* \ldots$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L

$\overline{Z} = \overline{P0} + \overline{P1} + \overline{P2} + \ldots$

$Z = \overline{P0}^* \overline{P1}^* \overline{P2} \ldots$

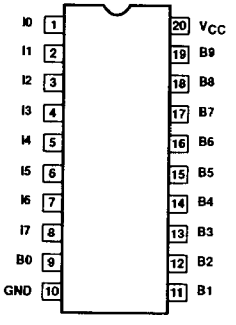
NOTES:

1. For each of the 10 outputs, either function Z (active-high) or Z (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

ORDERING INFORMATION

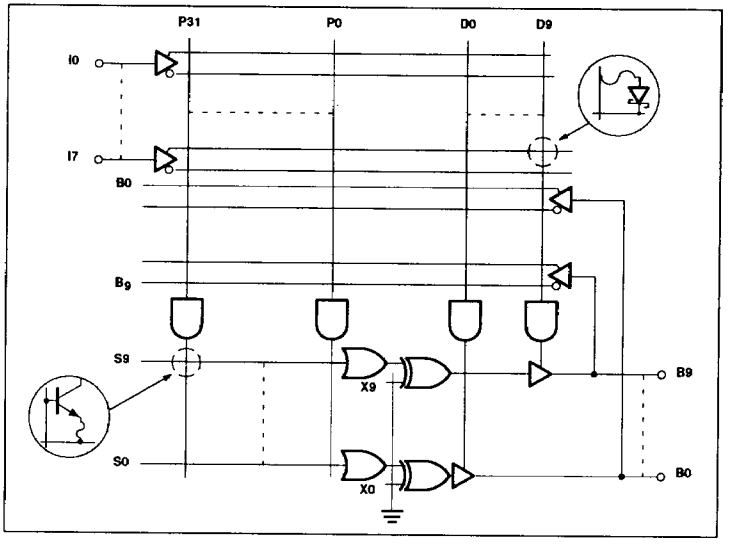
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP 300mil-wide	82S153A/BRA
20-Pin Ceramic FlatPack	82S153A/BSA
20-Pin Ceramic LLCC	82S153A/B2A

PIN CONFIGURATION

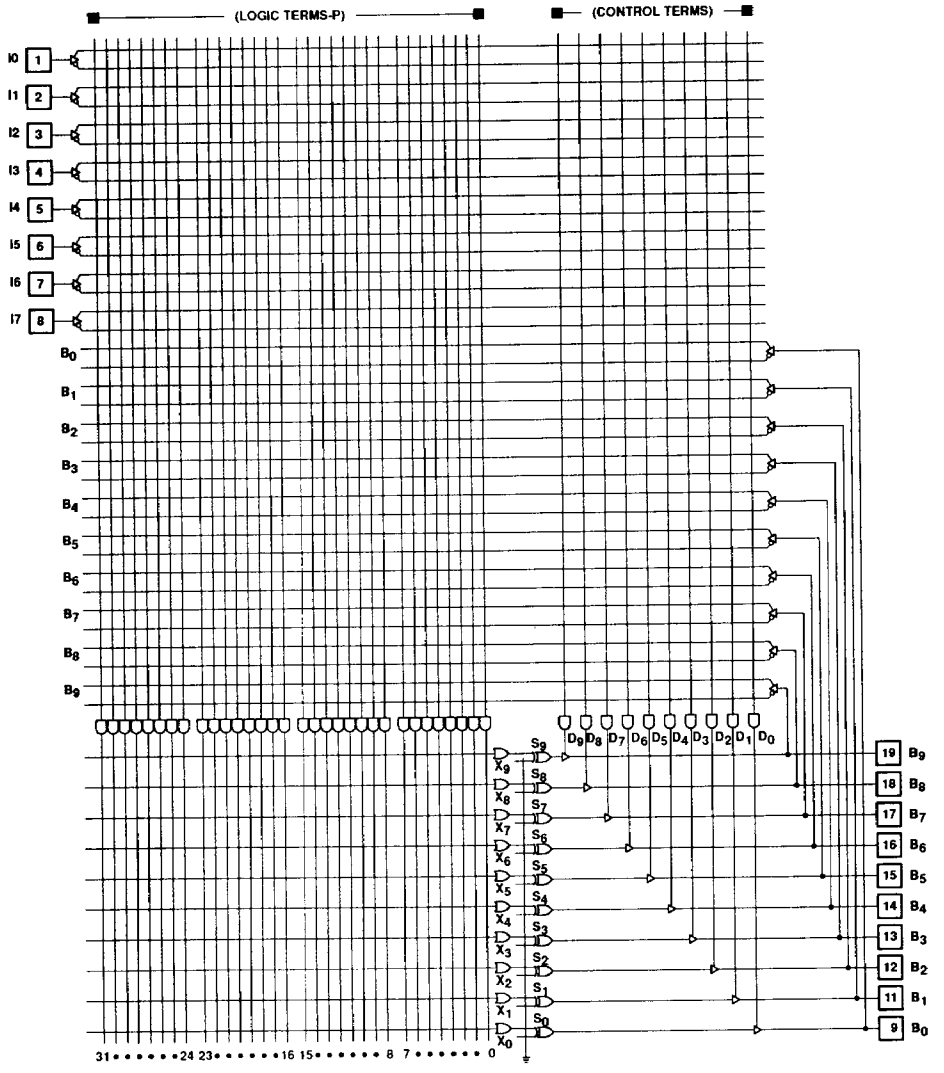


For LLCC pin assignments, see Package Section

FUNCTIONAL DIAGRAM



FPLA LOGIC DIAGRAM



NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. Programmable connection.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		MIN	MAX	
V_{CC}	Supply Voltage		+7	V_{DC}
V_I	Input voltage		+10.0	V_{DC}
V_O	Output voltage		+5.5	V_{DC}
I_I	Input currents	-30	+30	mA
I_O	Output currents		+100	mA
T_{amb}	Operating Temperature Range	-55	+125	°C
T_{STG}	Storage Temperature Range	-65	+150	°C

DC ELECTRICAL CHARACTERISTICS

$-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[3]			UNIT
			MIN	TYP[2]	MAX	
Input Voltage						
V_{IL}	Low	V_{CC} = 4.5V			0.80	V
V_{IH}	High	V_{CC} = 5.5V	2.0			V
V_{IK}	Clamp[4]	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output Voltage						
V_{OL}	Low[5]	V_{CC} = 4.5V I_{OL} = 12mA			0.5	V
V_{OH}	High[6]	I_{OH} = 2mA	2.4			V
Input current						
	Input pins only	V_{CC} = 5.5V				
I_{IL1}	Low	V_I = 0.45V			-150	µA
I_{IH1}	High	V_I = 5.5V			50	µA
	I/O pins only	V_{CC} = 5.5V				
I_{IL2}	Low	V_I = 0.45V			±210	µA
I_{IH2}	High	V_I = 5.5V			±110	µA
Output current						
$I_{O(OFF)}$	Hi-Z state[10]	V_{CC} = 5.5V V_O = 5.5V			±110	µA
		V_O = 0.45V			±210	µA
I_{OS}	Short circuit[4, 6, 7]	V_O = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = 5.5V		130	165	mA
Capacitance[12]						
		V_{CC} = 5V				
C_{IN}	Input	V_I = 2.0V		8	13	pF
C_B	I/O	V_B = 2.0V		15	20	pF

AC ELECTRICAL CHARACTERISTICS

$-55°C \leq T_{amb} \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					MIN	TYP[2]	MAX	
t_{PD}	Propagation delay	Output ±	Input ±	C_L = 30pF		20	45	ns
t_{OE}	Output enable	Output ±	Input ±			20	40	ns
t_{OD}	Output disable[9, 11]	Output ±	Input ±	C_L = 5pF		20	40	ns

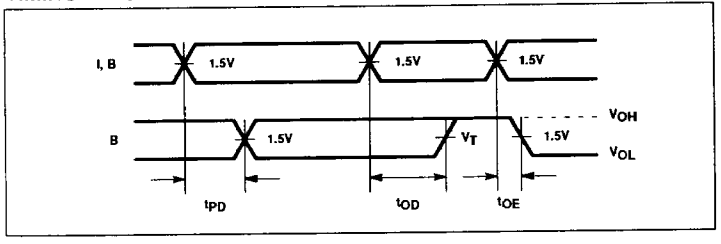
NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with +10V applied to I_7.
6. Measured with +10V applied to I_{0-7}. Output sink current is supplied through a resistor to V_{CC}.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with $I_{0,1}$ grounded, I_{2-7} and B_{0-9} at 4.5V.
9. Measured at $V_T = V_{OL} + 0.5V$.
10. Leakage values are a combination of input and output leakage.
11. Not testable on unprogrammed device.
12. Guaranteed, but not tested.

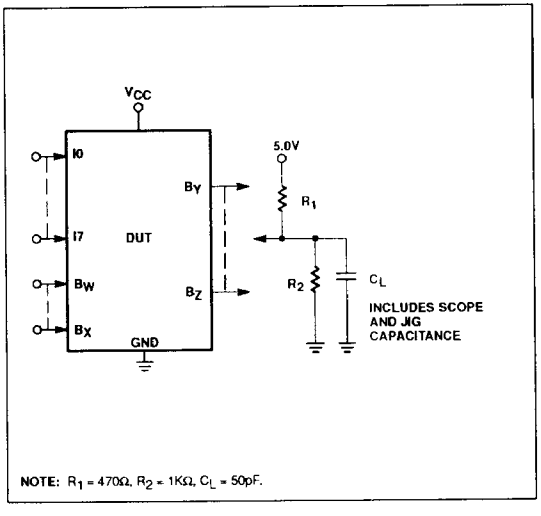
TIMING DEFINITIONS

SYMBOL	PARAMETER
T_{PD}	Propagation delay between input and output.
T_{DD}	Delay between input change and when output is off (Hi-Z or High).
T_{DE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAMS

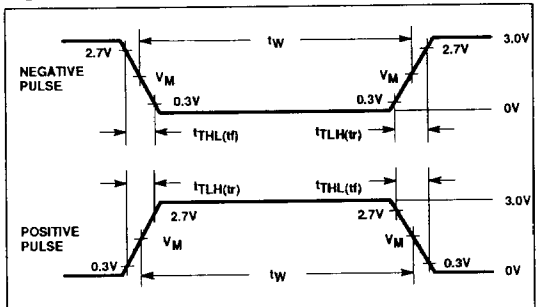


TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Field programmable logic array (18 × 42 × 10) 82S153A (PLS153A)

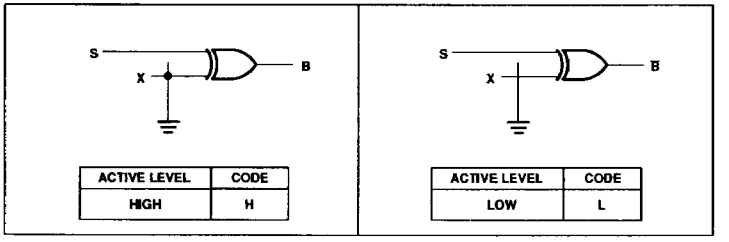
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this table the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

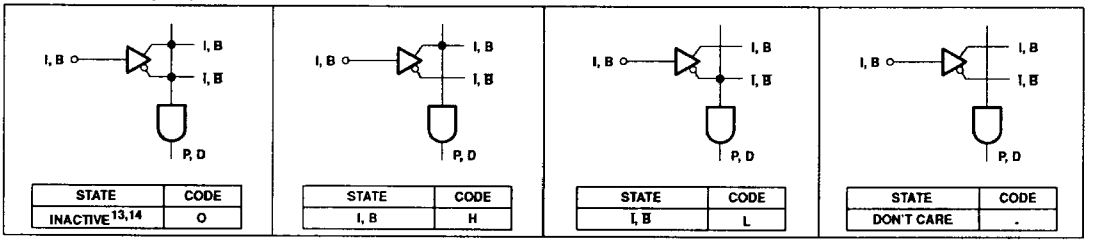
OUTPUT POLARITY - (B)



ACTIVE LEVEL	CODE
HIGH	H

ACTIVE LEVEL	CODE
LOW	L

AND ARRAY - (I, B)



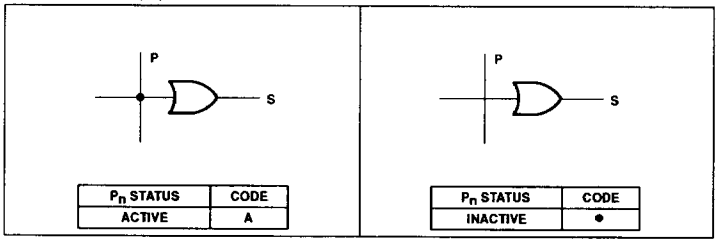
STATE	CODE
INACTIVE[13,14]	O

STATE	CODE
I, B	H

STATE	CODE
$\overline{I}$, $\overline{B}$	L

STATE	CODE
DON'T CARE	-

OR ARRAY - (B)



P_n STATUS	CODE
ACTIVE	A

P_n STATUS	CODE
INACTIVE	•

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditioanlly inhibited if both the True and Complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:
1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

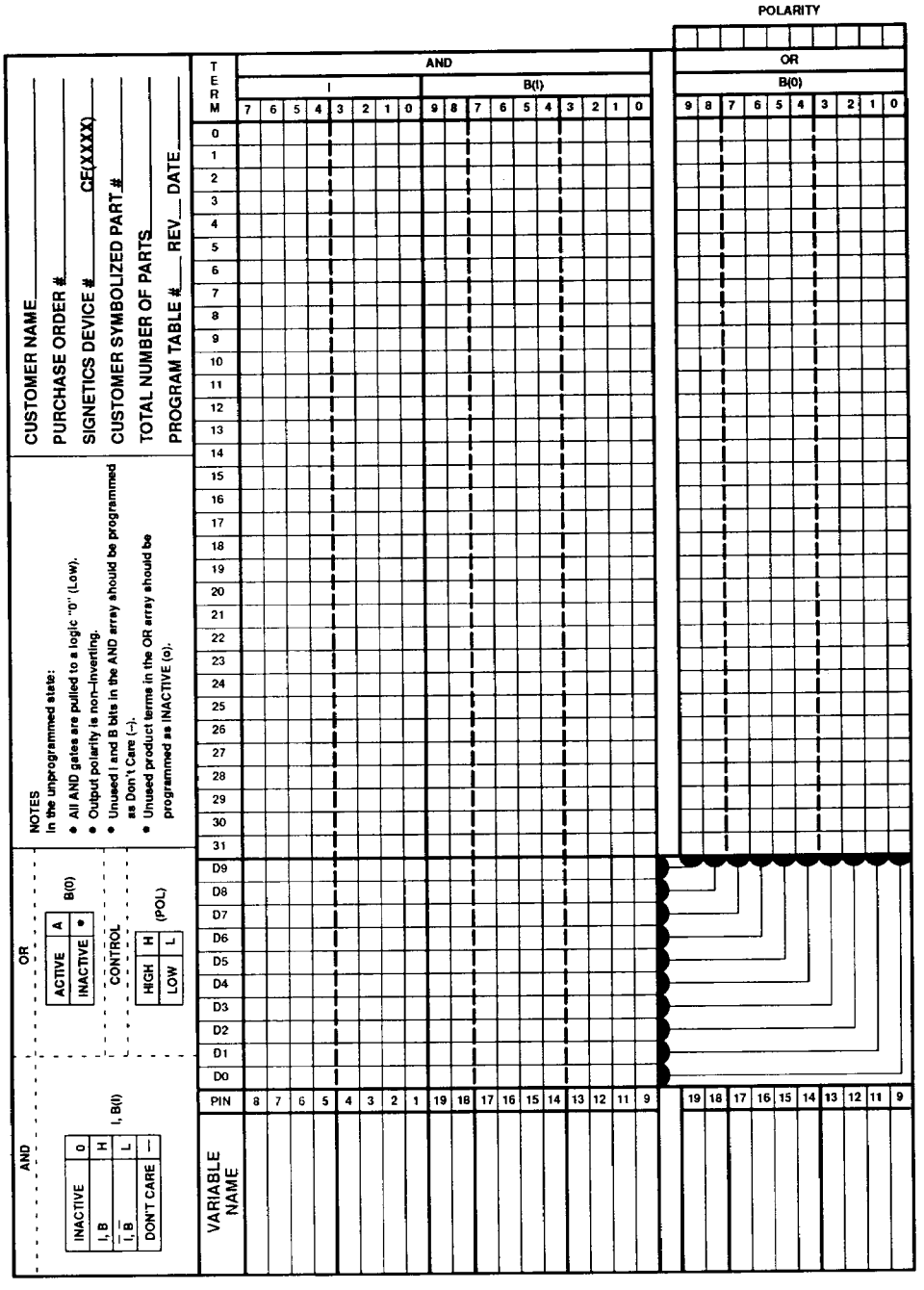
CAUTION: 82S153A TEST COLUMNS

The 82S153A incorporates two columns not shown in the logic block diagram. These columns are used for in-house testing of the device in the unprogrammed state. These columns must be disabled prior to using the 82S153A in your application. If you are using a Signetics-approved programmer, the disabling is accomplished during the device programming sequence. If these columns are not disabled, abnormal operation is possible.

Field programmable logic array (18 × 42 × 10)

82S153A (PLS153A)

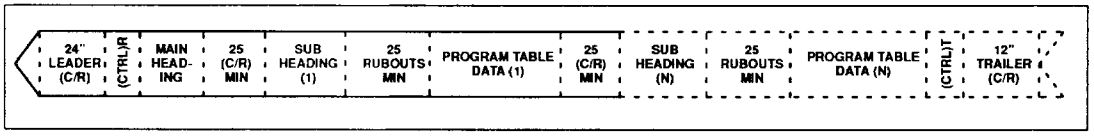
FPLA PROGRAM TABLE



TWX TAPE CODING (LOGIC FORMAT)

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however, limit tape length to a roll of 1.75 inch inside diameter and 4.25 outside diameter.



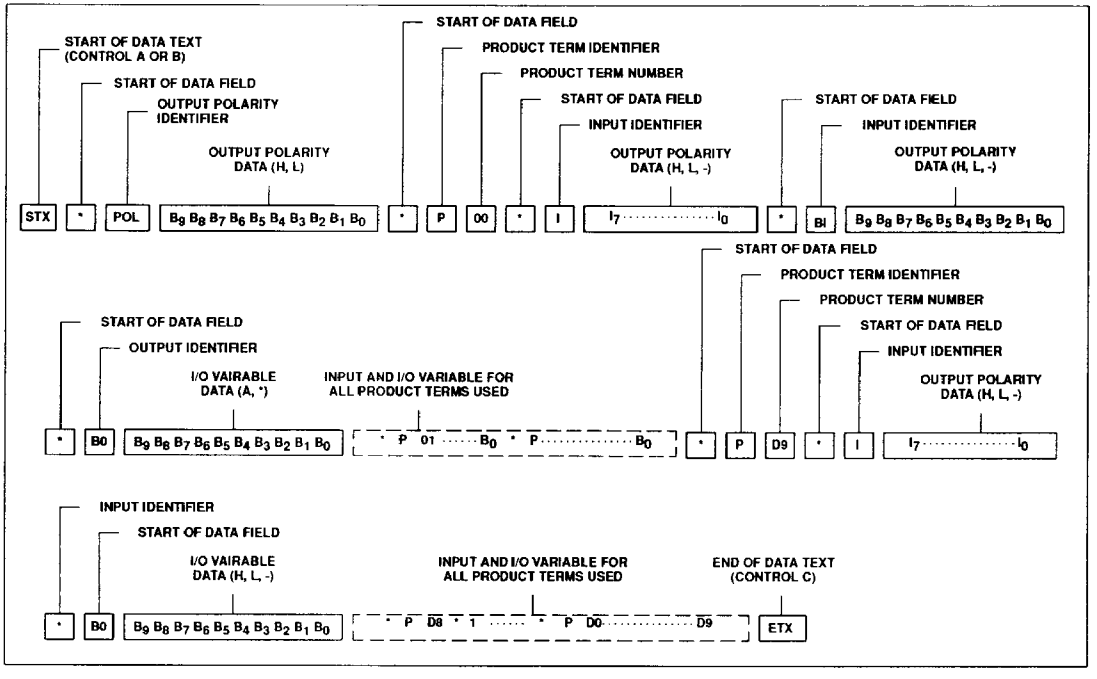
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

____1. Customer Name_____
____2. Customer TWX No._____
____3. Date_____
____4. Purchase Order No._____
____5. Number of Program Tables_____
____6. Total Number of Parts_____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

____1. Signetics Device No._____
____2. Program Table No._____
____3. Revision_____
____4. Date_____
____5. Customer Symbolized Part No._____
____6. Number of Parts_____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of output polarity, product term, and output information separated by appropriate identifiers in accordance with the following format. Entries for the data fields correspond to those defined in the Logic PROGRAM TABLE:



Packaging Information

T-90-20

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

Packaging Information

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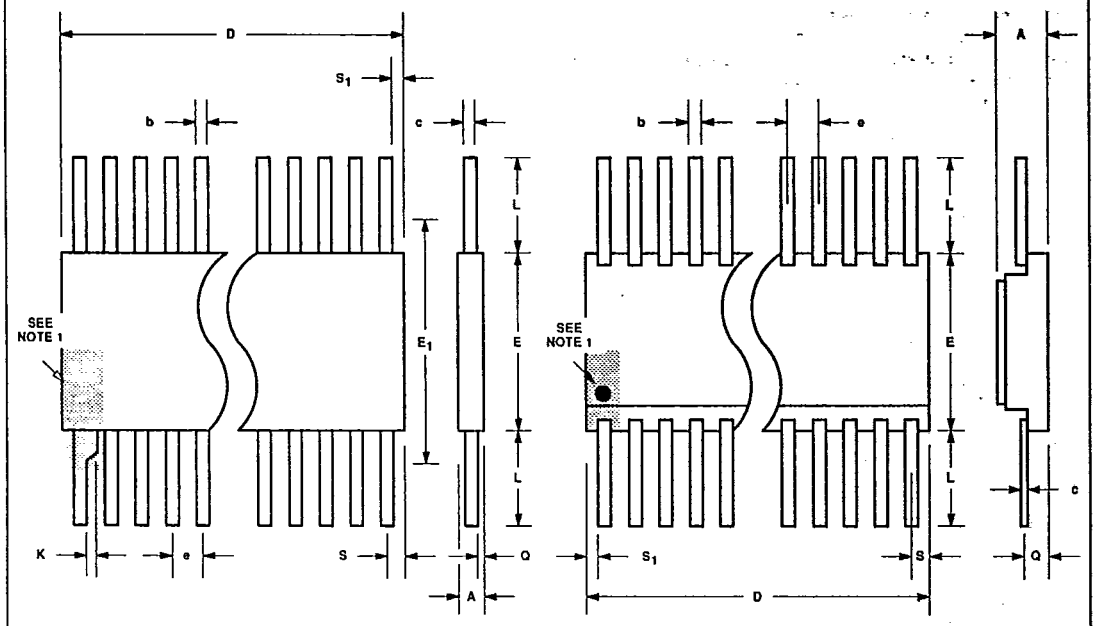
CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1

Configuration 2

NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counter-clockwise (as viewed from the top of the device.
2. This dimension allows for off-center lid, meniscus and glass overrun.
3. The reference pin spacing is 0.050 between center-lines. Each pin centerline is located within ±0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	–	1.330	2
E	0.620	0.660	
e	0.050BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	–	0.045	5
S1	0.005	–	5

Packaging Information

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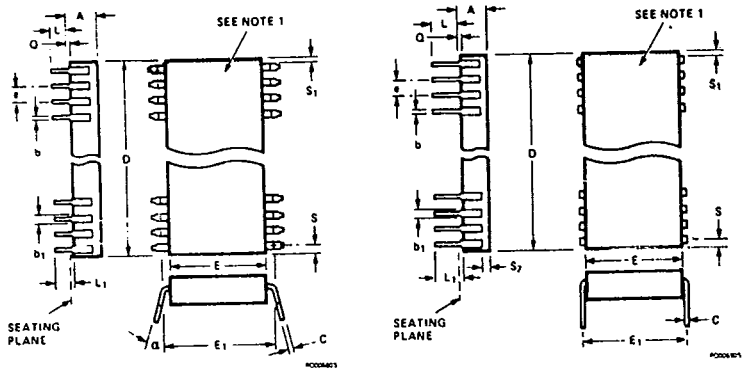
CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1

Configuration 2

1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

Packaging Information

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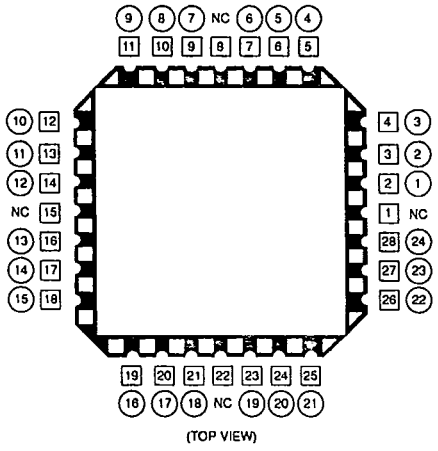
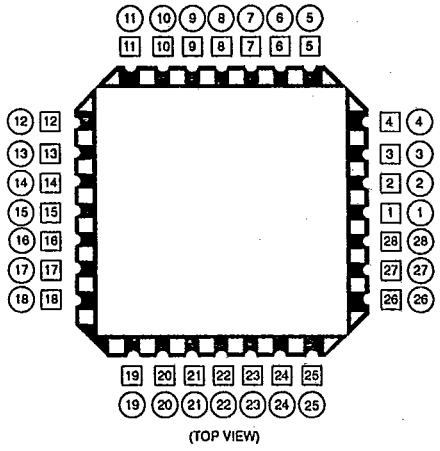
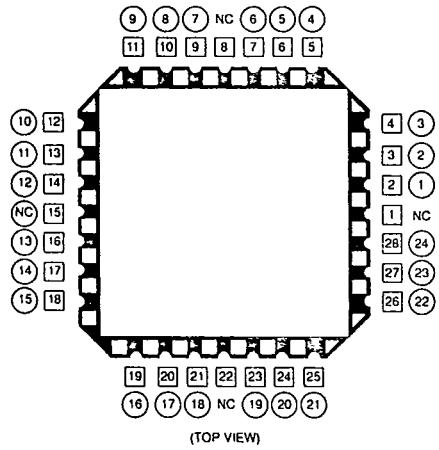
LEADLESS CHIP CARRIER (LLCC) PINOUTS



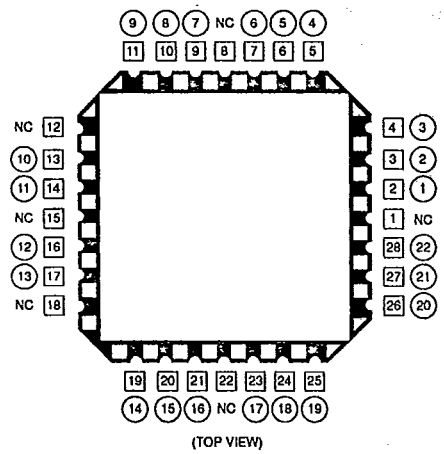
24-Lead Logic Pinout for 28 Terminal Chip Carrier



28-Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24-Lead Memory Pinout for 28 Terminal Chip Carrier



22-Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect

Packaging Information

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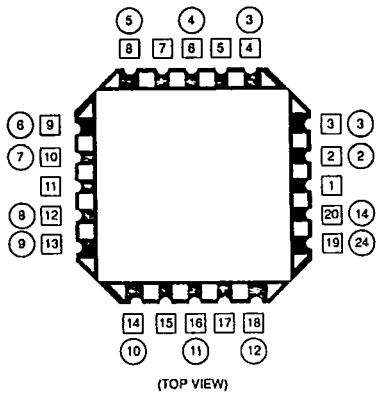
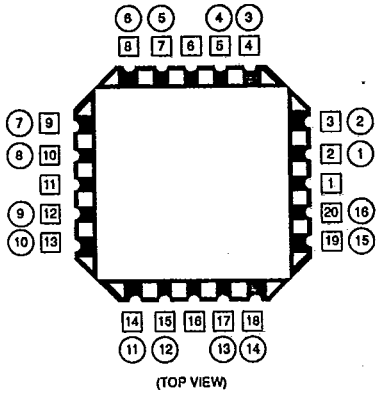
LEADLESS CHIP CARRIER (LLCC) PINOUTS



14-Pin Logic Pinout for 20 Terminal Chip Carrier



16-Pin Logic Pinout for 20 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number