REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19														
REV STATUS OF SHEETS	REV																		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-10-04

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, ARINC 429 MULTICHANNEL RECEIVER/TRANSMITTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-95518**

SHEET 1 OF 19

DESC FORM 193
JUL 94

5962-E029-95

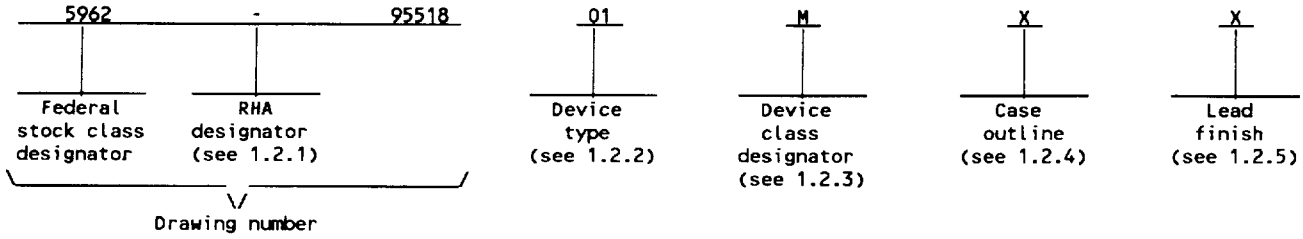
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0014143 345

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68C429A	CMOS Arinc 429 multichannel receiver/transmitter

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-P84	84	pin grid array
Y	CQCC1-G132	132	gullwing lead chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range, referenced to ground (V_{CC})	-0.3 V dc to +7.0 V dc
Input voltage	-0.3 V dc to +7.0 V dc
Storage temperature range	-55°C to 150°C
Maximum power dissipation (P_D)	400 mW
Lead temperature (soldering, 10 seconds)	+270°C
Maximum operating junction temperature (T_J)	+170°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	2°C/W
Case Y	3°C/W
Thermal resistance, junction-to-ambient (Θ_{JA}):	
Case X	28°C/W
Case Y	27°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage range (V_{IH})	2.25 V to 5.8 V
Low level input voltage range (V_{IL})	-0.3 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) . . . . . XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Managemaent (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 100 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}		1, 2, 3	All	2.25	V_{CC} +0.3	V
Input low voltage	V_{IL}		1, 2, 3	All	-0.5	0.8	V
Output high voltage	V_{OH}	(except $\overline{IRQRX}$, $\overline{IRQTX}$: open drain outputs)	1, 2, 3	All	2.7		V
Output low voltage	V_{OL}		1, 2, 3	All		0.5	V
Output source current (except IRQRX, IRQTX: open drain outputs)	I_{OH}	$V_{OUT} = 2.7\ V$	1, 2, 3	All		-8	mA
Output sink current	I_{OL}	$V_{OUT} = 0.5\ V$	1, 2, 3	All		8	mA
Input leakage current	I_{LI}	$V_{IN} = 0$ to V_{CC}	1, 2, 3	All		±20	µA
Dynamic current	I_{DD}	$T_{CASE} = T_{min}$, 2/ $V_{DD} = V_{max}$	1, 2, 3	All		65	mA
Input capacitance	C_{IN}	See 4.4.1c	4	All		10	pF
Hi-Z output capacitance	C_{OUT}	See 4.4.1c	4	All		20	pF
Functional test		See 4.4.1b $V_{CC} = 4.5\ V$, 5.5 V	7, 8				
Clock period	t_{CYCS}	$V_{CC} = 4.5\ V$ and 5.5 V	9, 10, 11	All	50	2000	ns
Clock pulse width	$\frac{t_{CLS}}{t_{CHS}}$	$V_{CC} = 4.5\ V$ and 5.5 V	9, 10, 11	All	20		ns
Rise and fall times	$\frac{t_{CRS}}{t_{CFS}}$	$V_{CC} = 4.5\ V$ and 5.5 V	9, 10, 11	All		5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0$ V ±10% unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Cycle time	t_{CYCA}	V_{CC} = 4.5 V and 5.5 V	9, 10, 11	All	200	8000	ns
Clock pulse width	t_{CLS} / t_{CHA}	V_{CC} = 4.5 V and 5.5 V	9, 10, 11	All	240		ns
Rise and fall times	tCR_A / t_{CFA}	V_{CC} = 4.5 V and 5.5 V	9, 10, 11	All		5	ns
Address valid to $\overline{CS}$ low	1	See figure 3	9, 10, 11	All	0		ns
R/W valid to $\overline{CS}$ low	2	See figure 3	9, 10, 11	All	0		ns
Data in valid to $\overline{LDS}/\overline{UDS}$ low	3	See figure 3	9, 10, 11	All	0		ns
CS, $\overline{LDS}/\overline{UDS}$, $\overline{IACKxx}$ valid to CLK-SYS low	4	See figure 3	9, 10, 11	All	5		ns
CLK-SYS low to $\overline{DTACK}$ low	5	See figure 3	9, 10, 11	All		45	ns
CLK-SYS low to data out valid	6	See figure 3	9, 10, 11	All		50	ns
$\overline{DTACK}$ low to data out valid	7	3/ See figure 3	9, 10, 11	All		10	ns
CS or $\overline{LDS}/\overline{UDS}$ or $\overline{IACKxx}$ high to DTACK high	8	3/ See figure 3	9, 10, 11	All		35	ns
$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ or $\overline{IACKxx}$ high to DTACK hi-z	9	3/ See figure 3	9, 10, 11	All		50	ns
$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ or $\overline{IACKxx}$ high to data out hi-z	10	3/ See figure 3	9, 10, 11	All		25	ns
$\overline{IEIxx}$ or $\overline{IACKxx}$ low to $\overline{IEOxx}$ low	11	See figure 3	9, 10, 11	All		35	ns
$\overline{IACKxx}$ high to $\overline{IEOxx}$ high	12	See figure 3	9, 10, 11	All		40	ns

See footnotes at the end of table.

TABLE I. Electrical performance characteristics. - continued

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{IEIxx}$ low to $\overline{DTACK}$ low	13	See figure 3	9, 10, 11	All		40	ns
$\overline{IEIxx}$ low to data out valid	14	See figure 3	9, 10, 11	All		45	ns
$\overline{CS}$, $\overline{IACKxx}$, $\overline{LDS}/\overline{UDS}$ inactive time	15	See figure 3	9, 10, 11	All	15		ns
$\overline{DTACK}$ low to $\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ or IACKxx high	16	3/ See figure 3	9, 10, 11	All	0		ns
$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ high to address hold time	17	3/ See figure 3	9, 10, 11	All	0		ns
$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ high to R/$\overline{W}$ invalid	18	3/ See figure 3	9, 10, 11	All	0		ns
$\overline{DTACK}$ low to data in hold time	19	3/ See figure 3	9, 10, 11	All	0		ns
$\overline{CS}$ or $\overline{LDS}/\overline{UDS}$ or $\overline{IACKxx}$ high data out hold time	20	3/ See figure 3	9, 10, 11	All	0		ns

1/ All testing performed using worst-case test conditions unless otherwise specfied.

2/ I_{DD} is measured with all I/O pins at 0 V, all input pins at 0 V except CLK-SYS and CLK-ARINC which run at t_{CYC} minimum.

3/ Guaranteed, but not tested.

Case X

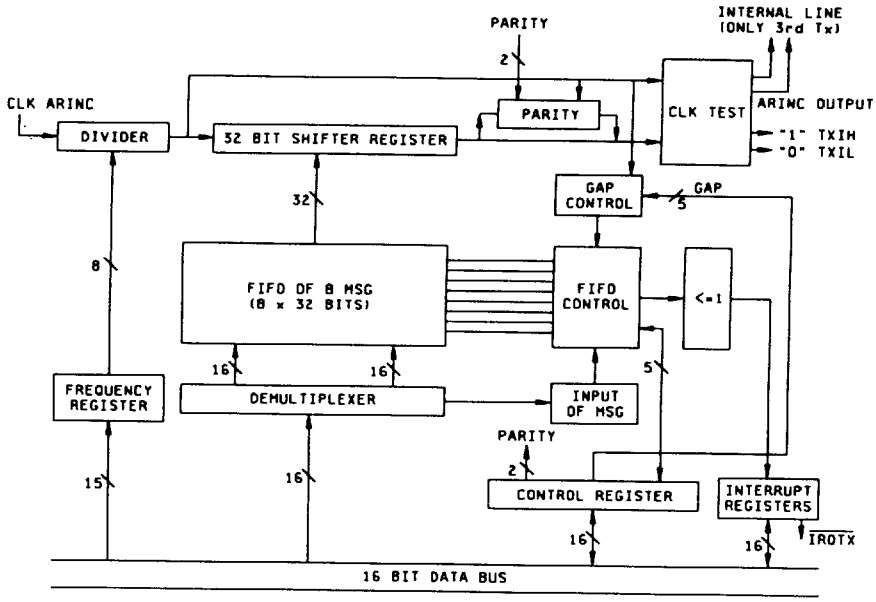
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	GND	C11	RX6H	J5	A5
A2	V_{DD}	D1	D4	J6	A6
A3	TX1H	D2	D3	J7	$\overline{LDS}$
A4	TX2H	D10	RX6L	J10	$\overline{IACKTX}$
A5	TX3L	D11	RX7H	J11	$\overline{IACKRX}$
A6	TX2L	E1	D7	K1	D15
A7	RX1L	E2	D6	K2	V_{DD}
A8	RX3H	E3	V_{DD}	K3	CLK-SYS
A9	RX4H	E9	GND	K4	A0
A10	RX4L	E10	RX8H	K5	A3
A11	V_{DD}	E11	RX8L	K6	A2
B1	D1	F1	D8	K7	$\overline{UDS}$
B2	V_{DD}	F2	D5	K8	$\overline{CS}$
B3	GND	F3	GND	K9	CLK-ARINC
B4	TX1L	F9	$\overline{DTACK}$	K10	$\overline{IEITX}$
B5	TX3H	F10	V_{DD}	K11	$\overline{IEIRX}$
B6	RX1H	F11	RX7L	L1	GND
B7	RX2H	G1	D9	L2	GND
B8	RX3L	G2	D10	L3	V_{DD}
B9	GND	G3	D11	L4	A1
B10	GND	G9	$\overline{IRQTX}$	L5	A4
B11	RX5L	G10	$\overline{IEOTX}$	L6	A7
C1	D2	G11	GND	L7	A8
C2	D0	H1	D12	L8	R/$\overline{W}$
C5	V_{DD}	H2	D13	L9	$\overline{RESET}$
C6	GND	H10	$\overline{IRQRX}$	L10	V_{DD}
C7	RX2L	H11	$\overline{IEORX}$	L11	GND
C9	NC	J1	D14		
C10	RX5H	J2	V_{DD}		

FIGURE 1. Terminal connections.

Case Y

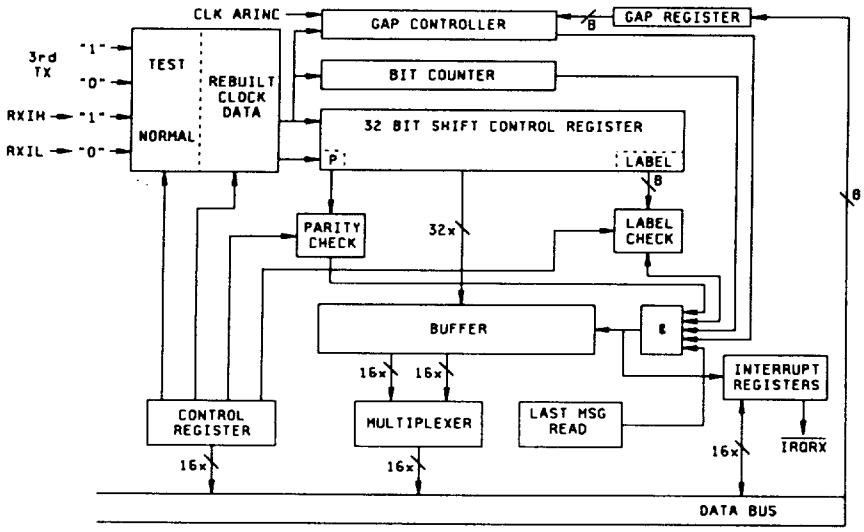
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	34	NC	67	NC	100	NC
2	NC	35	NC	68	NC	101	NC
3	NC	36	NC	69	NC	102	NC
4	V_{DD}	37	V_{DD}	70	V_{DD}	103	V_{DD}
5	GND	38	GND	71	GND	104	GND
6	D0	39	CLK-SYS	72	$\overline{IEITX}$	105	GND
7	D1	40	GND	73	$\overline{IACKTX}$	106	RX4L
8	NC	41	NC	74	$\overline{IEIRX}$	107	RX4H
9	D2	42	V_{DD}	75	$\overline{IACKRX}$	108	RX3L
10	D3	43	A0	76	$\overline{IRQRX}$	109	RX3H
11	D4	44	A1	77	$\overline{IEORX}$	110	RX1H
12	V_{DD}	45	V_{DD}	78	V_{DD}	111	V_{DD}
13	GND	46	GND	79	GND	112	NC
14	D6	47	A5	80	$\overline{IEOIX}$	113	RX2H
15	D7	48	A3	81	GND	114	RX1L
16	D5	49	A4	82	NC	115	RX2L
17	GND	50	A2	83	$\overline{IRQIX}$	116	GND
18	D11	51	A6	84	$\overline{DTACK}$	117	TX2L
19	D9	52	$\overline{LDS}$	85	RX7L	118	TX3L
20	V_{DD}	53	V_{DD}	86	NC	119	V_{DD}
21	GND	54	GND	87	GND	120	GND
22	D10	55	A8	88	RX8L	121	TX3H
23	D8	56	$\overline{UDS}$	89	RX8H	122	V_{DD}
24	D12	57	A7	90	GND	123	TX2H
25	D13	58	R/$\overline{W}$	91	RX7H	124	TX1L
26	D14	59	$\overline{CS}$	92	RX6L	125	TX1H
27	D15	60	$\overline{RESET}$	93	RX6H	126	NC
28	V_{DD}	61	V_{DD}	94	V_{DD}	127	V_{DD}
29	GND	62	GND	95	GND	128	GND
30	NC	63	CLK-ARINC	96	RX5L	129	GND
31	NC	64	GND	97	RX5H	130	NC
32	NC	65	NC	98	V_{DD}	131	NC
33	NC	66	NC	99	NC	132	NC

FIGURE 1. Terminal connections. - continued



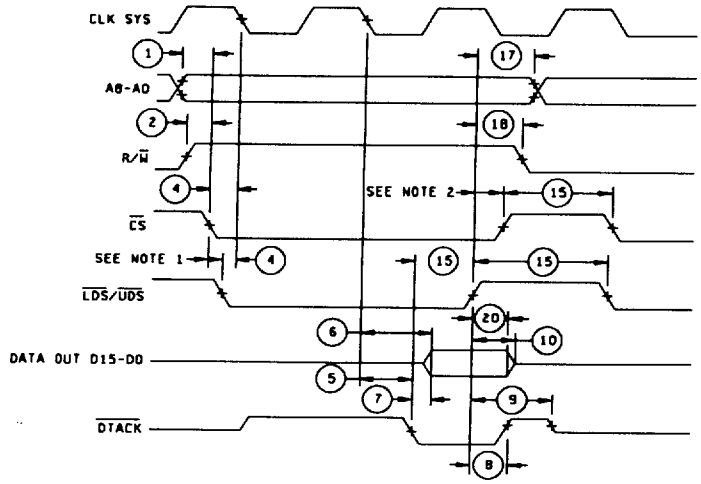
Transmitter channel block diagram

FIGURE 2. Block diagram.



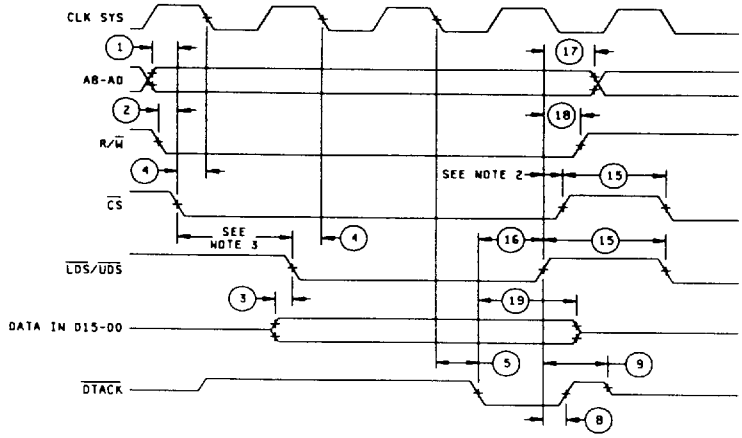
Receiver channel block diagram

FIGURE 2. Block diagram. - continued



Read cycle

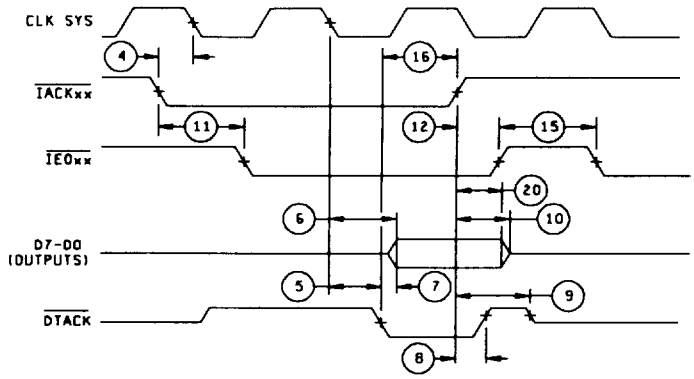
NOTE 1. LDS/UDS can be asserted on the next CLK-SYS period after CS goes low bit (4) must be met for the next period.
NOTE 2. The cycle ends when the first of CS, LDS/UDS goes high.



Write cycle

NOTE 3. LDS/UDS can be asserted on the same CLK-SYS priod as CS but (4) must be met.

FIGURE 3. Timing waveforms.

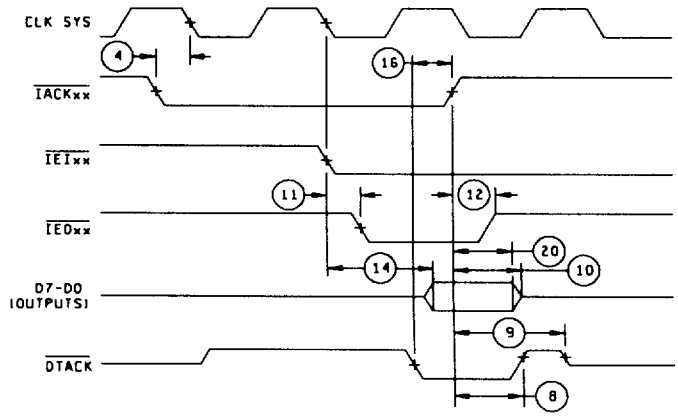


Interrupt cycle ($\overline{IEIxx}$ = 0).

NOTE:

If $\overline{UDS}$ = 1, D15-D8 stay hi-z else D15-D8 drive the bus with a stable unknown value.

If $\overline{IEOxx}$ goes low, nor vector neither $\overline{DTACK}$ are generated, else $\overline{IEOxx}$ stays inactive and a vector is generated (D7-D0 and $\overline{DTACK}$).



Interrupt cycle ($\overline{IEIxx}$ = 1)

FIGURE 3. Timing waveforms. - continued

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, or C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionallity of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} measurment) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, or C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1/1,2,3,7,8,9,10,11	1/1,2,3,7,8,9, 10,11	2/1,2,3,7,8, 9,10,11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8,9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3,	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5765, or telephone (513) 296-8525.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

Bit	Function	Comments
Bit 15	Channel enable	0: channel is out of service 1: channel is in service
Bit 14	Test mode	0: external ARINC lines as input (normal operation) 1: third transmitter lines as input (test mode)
Bit 13	Label control	0: no control, all the labels are accepted 1: automatic check of the label according to the label control matrix
Bit 12	LCMWE label control matrix write enable	0: receiving mode (write to the matrix are disabled) 1: programmation mode for labels control matrix
Bit 11	Parity control	0: even parity check 1: odd parity check
Bit 10	Paraity control	0: parity ckeck is disable 1: parity check is enable
Bit 9 Bit 8	Not used Not used	
Bit 7	Wrong parity: this feature is enable only if self test register bit 0 is set to 1	0: received message parity is correct if read, reset wrong , wrong parity flag if written 1: an incorrect received message parity has been detected (the corresponding message is lost) (set by hardware)
Bit 6 Bit 5 Bit 4	Not used Not used Not used	
Bit 0 to 3	Channel priority: order	The lowest value will give the highest priority. Each channel must have a unique channel priority order. If several messages are pending, the interrupt vector will account for highest priority channel

This read/write register controls the function of the related receiver channel.
The lowest value will give the highest priority. If two channels have the same priority, one of them will never be able to send its interrupt vector to the microprocessor. Each channel must have a unique channel priority order.

Receiver control register.

Bit	Function	Comments
Bit 15	Enable transmission	0: channel out of service (stops on going transmission) 1: channel in service 1 to 0: transition is not allowed at the same time as an 1 to 0 transition of the bit 4
Bit 14	Test (only 3rd channel)	0: normal operating 1: test, output are only driven on internal lines for input testing
Bit 13 to 12	Not used	
Bit 11	Parity control	0: even parity calculation 1: odd parity calculation
Bit 10	Parity control	0: parity disable. Bit 32 of the message stays unchanged 1: parity enable. Bit 32 of the message will be forced by parity control
Bit 9 to 5	Transmission gap	"transmission gap" which is the delay between two 32 bit ARINC messages (in ARINC bit)
Bit 4	Reset FIFO	- write a 0 in this bit, reset the FIFO counter - this bit must be set to 1 before any write in the transmit buffer - 1 to 0: transition is not allowed at the same time as an 1 to 0 transition of the bit 15
Bit 3 to 0	Number of msg	these four bits contain the number of messages within the FIFO

Transmitter control register

Bit	Function	Comments
Bit 15, 13, 11	FIFO channel 3, 2, 1	0: FIFO not empty 1: FIFO empty
Bit 14, 12, 10	Transmission on channel 3, 2, 1	0: Transmission occurs 1: No transmission actually
Bit 8	RX wrong parity. This feature is available only if self-test register bit 0 is set to 1. This bit must be reset to 0 by user when needed	0: No wrong parity received 1: At least one receiver has received a message with wrong parity (set by hardware)
Bit 7, 6, 5, 4, 3, 2, 1, 0	Receiving channel 8, 7, 6, 5, 4, 3, 2, 1	0: Waiting for message 1: Received correct message

Logical control unit status register

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.