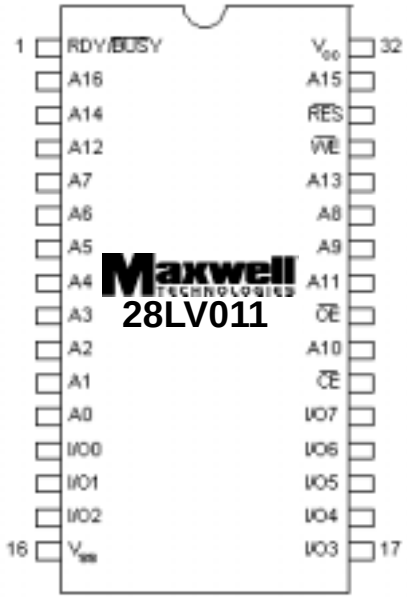
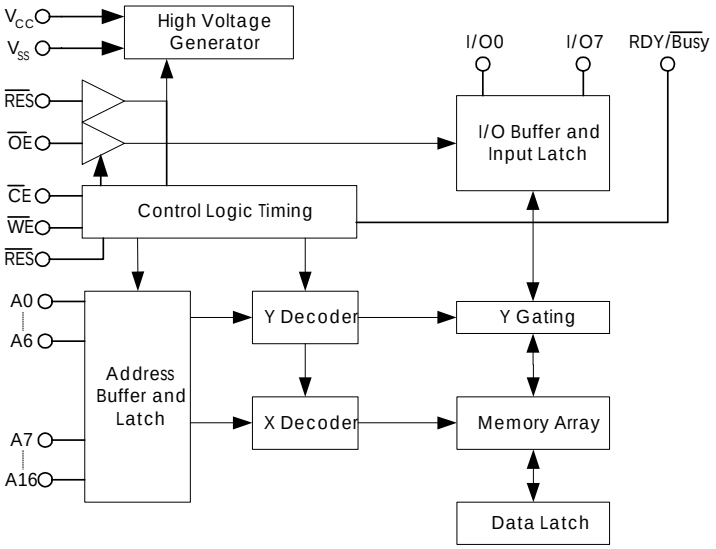
28LV011
3.3V 1 Megabit (128K x 8-Bit) EEPROM





Logic Diagram

FEATURES:

- 3.3V low voltage operation 128K x 8 Bit EEPROM
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Excellent Single Event Effects:
  - SEL_{TH} > 84 MeV/mg/cm^2
  - SEU_{TH} > 37 Mev/mg/cm^2 (read mode)
  - SEU saturated cross section = 3E-6 cm^2 (read mode)
  - SEU_{TH} = 11.4 Mev/mg/cm^2 (write mode)
  - SEU saturated cross section = 5E-3 cm^2 (write mode) with hard errors
- Package:
  - 32 Pin RAD-PAK® flat pack
  - 32 Pin RAD-PAK® DIP
  - JEDEC-approved byte-wide pinout
- Address Access Time:
  - 200, 250 ns Access times available
- High endurance:
  - 10,000 erase/write (in Page Mode), 10-year data retention
- Page write mode:
  - 1 to 128 bytes
- Automatic programming
  - 15 ms automatic page/byte write
- Low power dissipation
  - 20 mW/MHz active current (typ.)
  - 72 µW standby (maximum)

DESCRIPTION:

Maxwell Technologies' 28LV011 high density, 3.3V, 1 Megabit EEPROM microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The 28LV011 is capable of in-system electrical Byte and Page programmability. It has a 128-Byte Page Programming function to make its erase and write operations faster. It also features Data Polling and a Ready/Busy signal to indicate the completion of erase and programming operations. In the 28LV011, hardware data protection is provided with the RES pin, in addition to noise protection on the WE signal and write inhibit on power on and off. Meanwhile, software data protection is implemented using the JEDEC-optional Standard algorithm. The 28LV011 is designed for high reliability in the most demanding space applications.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

Note:The recommended form of data protection during power on/off is to hold the RES pin to V_{SS} during power up and power down. This may be accompanied by connecting the RES pin to the CPU reset line. Failure to provide adequate protection during power on/off may result in lost or modified data.

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TABLE 1. 28LV011A PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
12-5, 27, 26, 23, 25, 4, 28, 3, 31, 2	A0-A16	Address
13-15, 17-21	I/O0 - I/O7	Input/Output
24	$\overline{OE}$	Output Enable
22	$\overline{CE}$	Chip Enable
29	$\overline{WE}$	Write Enable
32	V_{CC}	Power Supply
16	V_{SS}	Ground
1	RDY/$\overline{BUSY}$	Ready/Busy
30	$\overline{RES}$	Reset

TABLE 2. 28LV011 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage (Relative to Vss)	V_{CC}	-0.6	7.0	V
Input Voltage (Relative to Vss)	V_{IN}	-0.5 [1]	7.0	V
Operating Temperature Range	T_{OPR}	-55	125	°C
Storage Temperature Range	T_{STG}	-65	150	°C

1. V_{IN} min = -3.0 V for pulse width ≤ 50 ns.

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
$I_{CC}1$	±10%
$I_{CC}2$	±10%
$I_{CC}3A$	±10%
$I_{CC}3B$	±10%

TABLE 4. 28LV011 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	3.0	3.6	V
Input Voltage $\overline{RES}$_PIN	V_{IL} V_{IH} V_H	-0.3 [1] 2.0 [2] V_{CC}-0.5	0.8 V_{CC}+0.3 V_{CC} +1	V
Operating Temperature Range	T_{OPR}	-55	+125	°C

1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. V_{IH} min = 2.2 V for V_{CC} = 3.6 V.

TABLE 5. 28LV011 CAPACITANCE

(T_A = 25°C, F = 1MHz)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Capacitance: V_{IN} = 0V [1]	C_{IN}	--	6	pF
Output Capacitance: V_{OUT} = 0V [1]	C_{OUT}	--	12	pF

1. Guaranteed by design.

TABLE 6. 28LV011 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3, T_A = -55 TO +125°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SUBGROUPS	SYMBOL	MIN	MAX	UNIT
Input Leakage Current	V_{CC} = 3.6V, V_{IN} = 3.6V	1, 2, 3	I_{LI}	--	2	µA
Output Leakage Current	V_{CC} = 3.6V, V_{OUT} = 3.6V/0.4V	1, 2, 3	I_{LO}	--	2	µA
Standby V_{CC} Current	$\overline{CE}$ = V_{CC} $\overline{CE}$ = V_{IH}	1, 2, 3	I_{CC1} I_{CC2}	-- --	20 1	µA mA
Operating V_{CC} Current	I_{OUT} = 0mA, Duty = 100%, Cycle = 1 µs @ V_{CC} = 3.3V I_{OUT} = 0mA, Duty = 100%, Cycle = 250 ns @ V_{CC} = 3.3V	1, 2, 3	I_{CC3}	-- --	6 15	mA
Input Voltage		1, 2, 3	V_{IL} V_{IH} V_H	-- 2.0[1] V_{CC}-0.5	0.8 -- --	V
Output Voltage	I_{OL} = 2.1 mA I_{OH} = -400 µA	1, 2, 3	V_{OL} V_{OH}	-- V_{CC}x0.8	0.4 --	V

1. V_{IH} min = 2.2V for V_{CC} = 3.6V.

TABLE 7. 28LV011 AC CHARACTERISTICS FOR READ OPERATION[1]

(V_{CC} = 3.3V ± 10%, T_A = -55 TO +125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SUBGROUPS	SYMBOL	MIN	MAX	UNIT
Functional Test	Verify Truth Table	7, 8A, 8B	All			
Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$	9, 10, 11	t_{ACC}			ns
-200				--	200	
-250				--	250	
Chip Enable Access Time	$\overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$	9, 10, 11	t_{CE}			ns
-200				--	200	
-250				--	250	
Output Enable Access Time	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$	9, 10, 11	t_{OE}			ns
-200				0	110	
-250				0	120	
Output Hold to Address Change	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$	9, 10, 11	t_{OH}			ns
-200				0	--	
-250				0	--	
Output Disable to High-Z[2]	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$	9, 10, 11	t_{DF}			ns
-200	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$			0	50	
-250				0	50	
Output Disable to High-Z	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$	9, 10, 11	t_{DFR}			ns
-200	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$			0	300	
-250				0	350	
$\overline{RES}$ to Output Delay [3]	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{WE} = V_{IH}$	9, 10, 11	t_{RR}			ns
-200				0	525	
-250				0	550	

1. Test conditions: Input pulse levels - 0.4V to 2.4V; input rise and fall times < 20 ns; output load - 1 TTL gate + 100 pF (including scope and jig); reference levels for measuring timing - 0.8V/1.8V.
2. t_{DF} and t_{DFR} is defined as the time at which the output becomes an open circuit and data is no longer driven.
3. Guaranteed by design.

TABLE 8. 28LV011 AC ELECTRICAL CHARACTERISTICS FOR ERASE AND WRITE OPERATIONS

(V_{CC} = 3.3V ± 10%, T_A = -55 TO +125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNIT
Address Setup Time	9, 10, 11	t_{AS}			ns
-200			0	--	
-250			0	--	
Chip Enable to Write Setup Time ($\overline{WE}$ controlled)	9, 10, 11	t_{CS}			ns
-200			0	--	
-250			0	--	
Write Pulse Width ($\overline{CE}$ controlled)	9, 10, 11	t_{CW}			ns
-200			200	--	
-250			250	--	
Write Pulse Width ($\overline{WE}$ controlled)	9, 10, 11	t_{WP}			ns
-200			200	--	
-250			250	--	
Address Hold Time	9, 10, 11	t_{AH}			ns
-200			125	--	
-250			150	--	
Data Setup Time	9, 10, 11	t_{DS}			ns
-200			100	--	
-250			100	--	
Data Hold Time	9, 10, 11	t_{DH}			ns
-200			10	--	
-250			10	--	
Chip Enable Hold Time ($\overline{WE}$ controlled)	9, 10, 11	t_{CH}			ns
-200			0	--	
-250			0	--	
Write Enable to Write Setup Time ($\overline{CE}$ controlled)	9, 10, 11	t_{WS}			ns
-200			0	--	
-250			0	--	
Write Enable Hold Time ($\overline{CE}$ controlled)	9, 10, 11	t_{WH}			ns
-200			0	--	
-250			0	--	
Output Enable to Write Setup Tim	9, 10, 11	t_{OES}			ns
-200			0	--	
-250			0	--	
Output Enable Hold Time	9, 10, 11	t_{OEH}			ns
-200			0	--	
-250			0	--	
Write Cycle Time [1,2]	9, 10, 11	t_{WC}			ms
-200			--	15	
-250			--	15	

TABLE 8. 28LV011 AC ELECTRICAL CHARACTERISTICS FOR ERASE AND WRITE OPERATIONS

(V_{CC} = 3.3V ± 10%, T_A = -55 TO +125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNIT
Byte Load Cycle	9, 10, 11	t_{BLC}			µs
-200			1	30	
-250			1	30	
Data Latch Time[2]	9, 10, 11	t_{DL}			ns
-200			700	--	
-250			750	--	
Byte Load Window [2]	9, 10, 11	t_{BL}			µs
-200			100	--	
-250			100	--	
Time to Device Busy	9, 10, 11	t_{DB}			ns
-200			100	--	
-250			120	--	
Write Start Time	9, 10, 11	t_{DW}			ns
-200			250	--	
-250			250	--	
$\overline{RES}$ to Write Setup Time[2]	9, 10, 11	t_{RP}			µs
-200			100	--	
-250			100	--	
V_{CC} to $\overline{RES}$ Setup Time [2]	9, 10, 11	t_{RES}			µs
-200			1	--	
-250			1	--	

1. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{BSY}$ are used. This device automatically completes the internal write operation within this value.
2. Guaranteed by design.

TABLE 9. 28LV011 MODE SELECTION[1,2]

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{BUSY}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z --> V_{OL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	--	--
	X	V_{IL}	X	X	--	--
Data Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O7)
Program	X	X	X	V_{IL}	High-Z	High-Z

1. X = Don't care.
2. Refer to the recommended DC operating conditions.

FIGURE 1. READ TIMING WAVEFORM

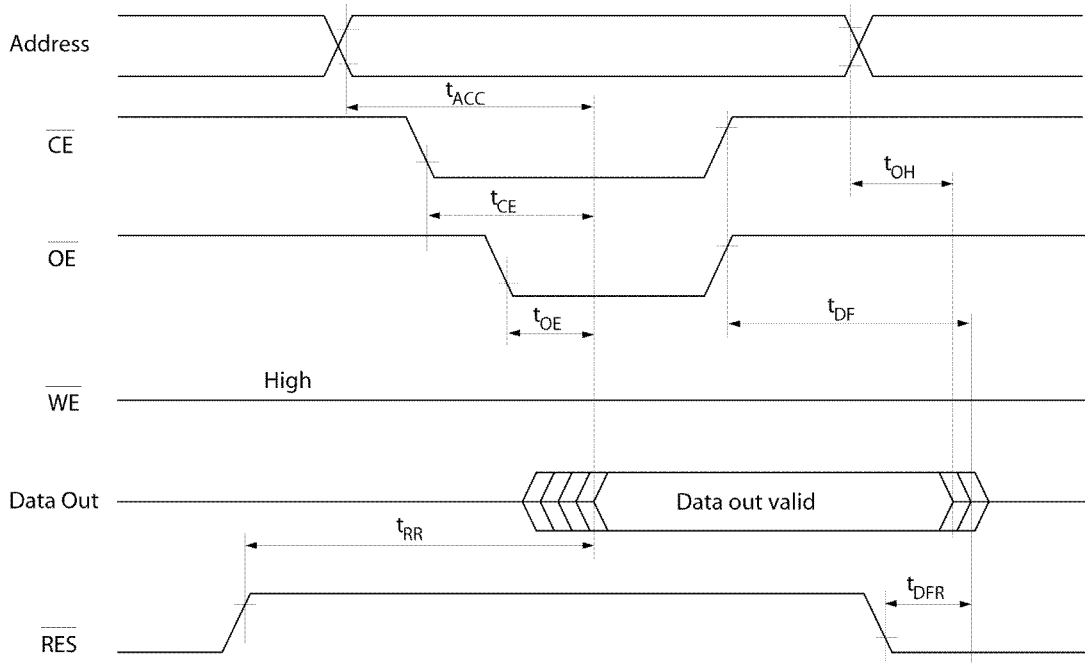


FIGURE 2. BYTE WRITE TIMING WAVEFORM(1) ($\overline{WE}$ CONTROLLED)

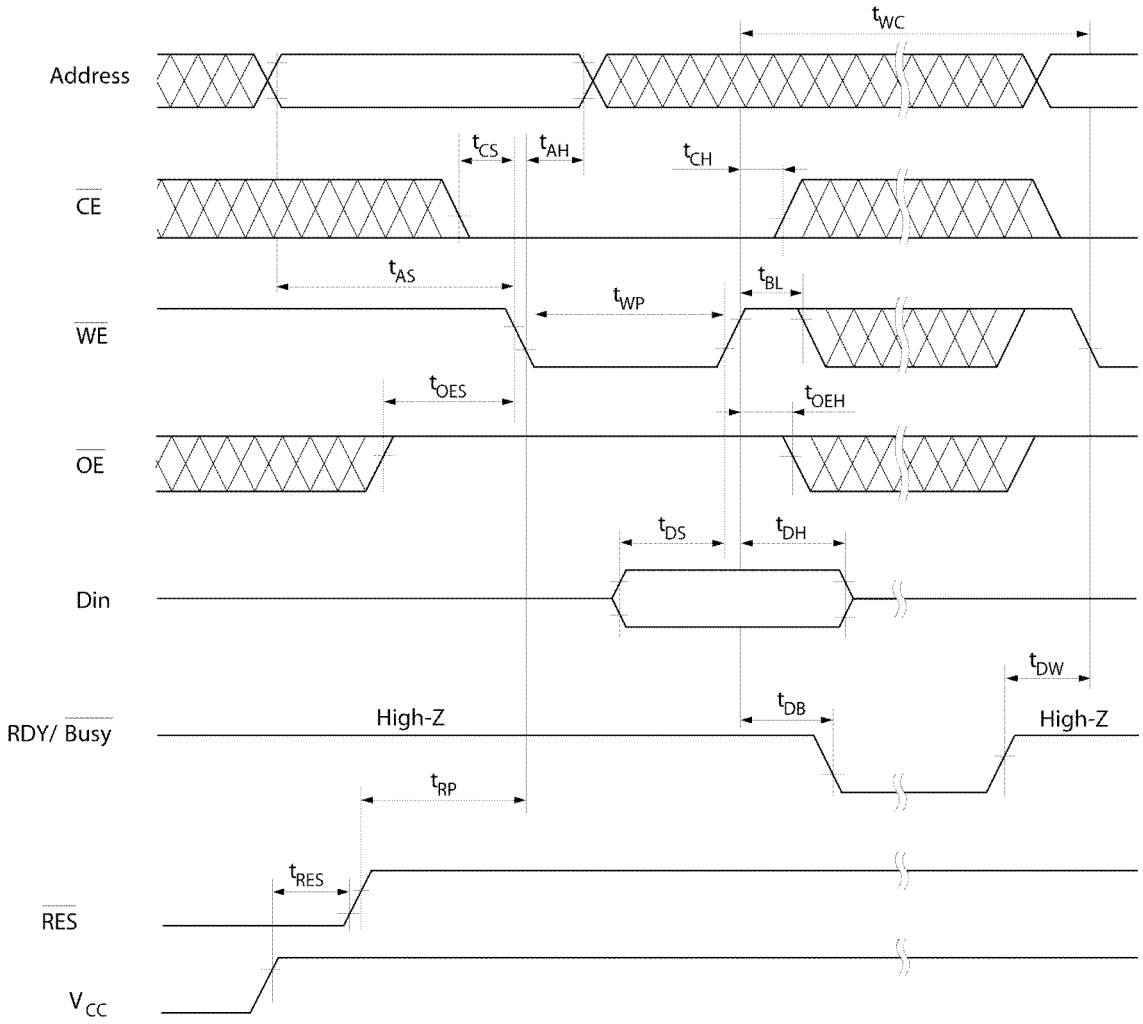


FIGURE 3. BYTE WRITE TIMING WAVEFORM (2) ($\overline{CE}$ CONTROLLED)

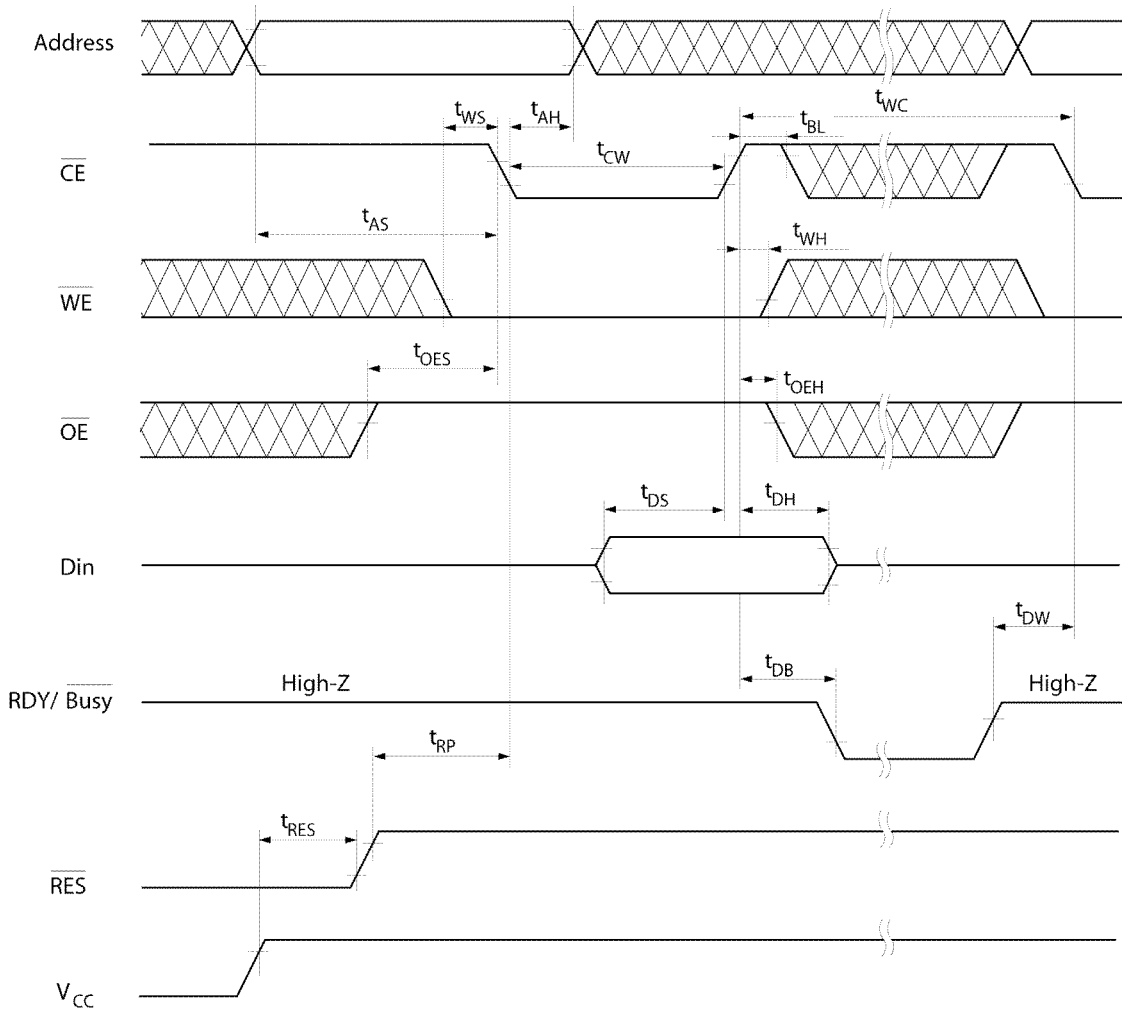


FIGURE 4. PAGE WRITE TIMING WAVEFORM(1) ($\overline{WE}$ CONTROLLED)

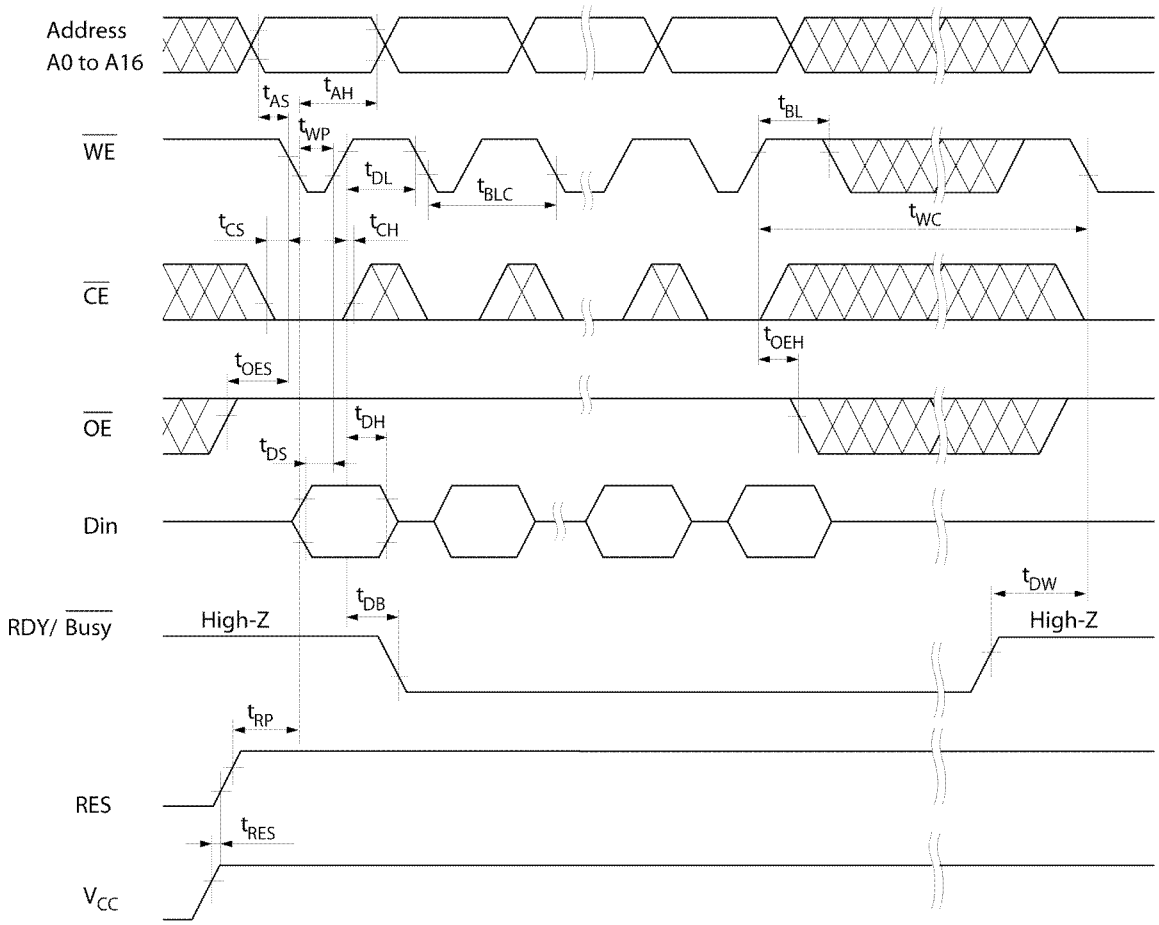


FIGURE 5. PAGE WRITE TIMING WAVEFORM(2) ($\overline{CE}$ CONTROLLED)

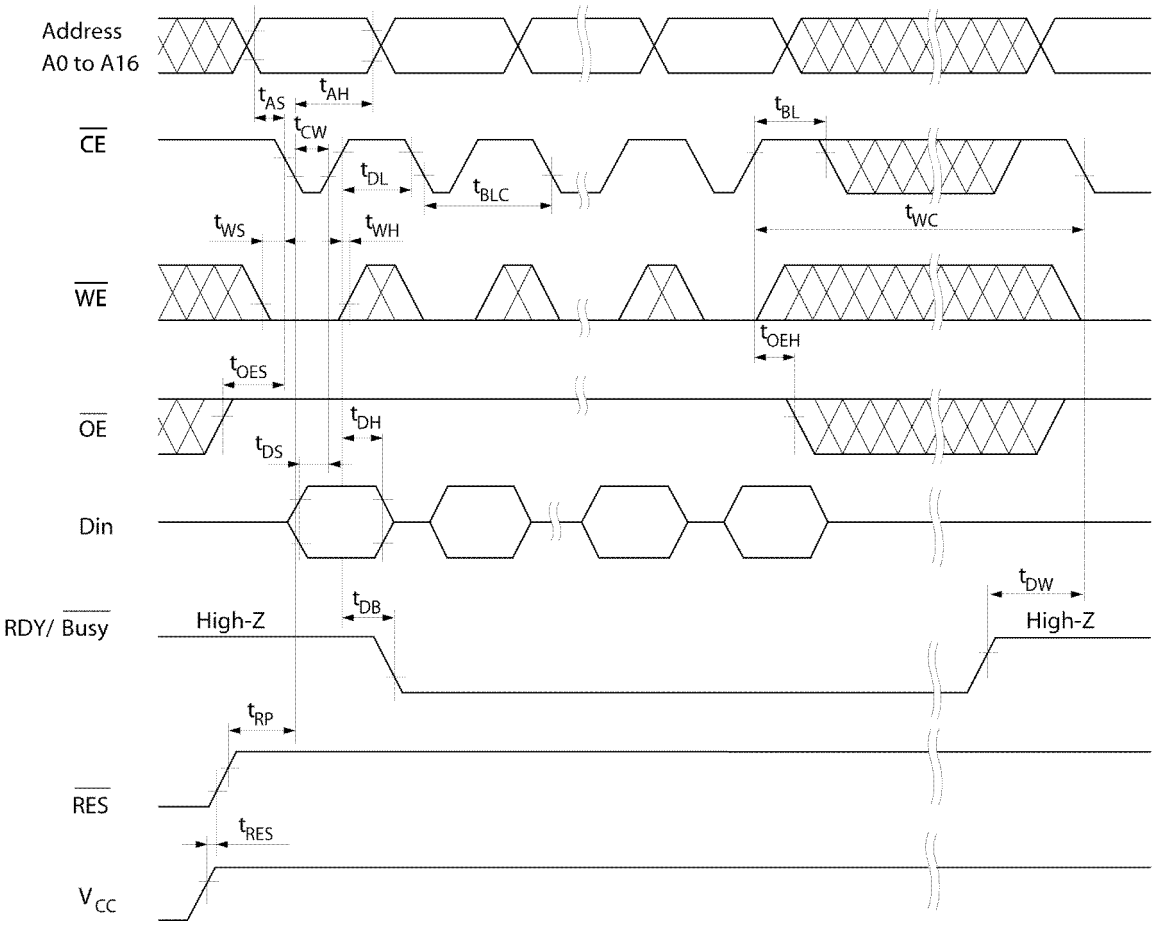
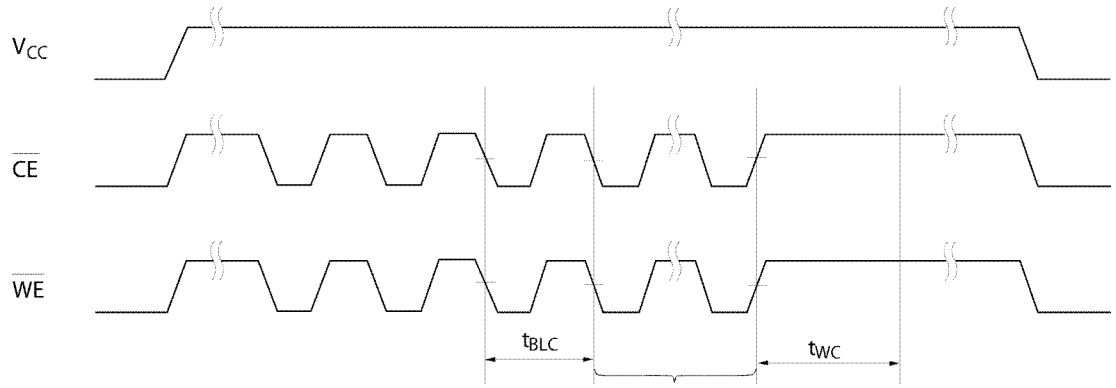


FIGURE 6. SOFTWARE DATA PROTECTION TIMING WAVEFORM(1) (IN PROTECTION MODE)



Address	5555	AAAA or 2AAA	5555	Write address
Data	AA	55	A0	Write data

FIGURE 7. SOFTWARE DATA PROTECTION TIMING WAVEFORM(2) (IN NON-PROTECTION MODE)

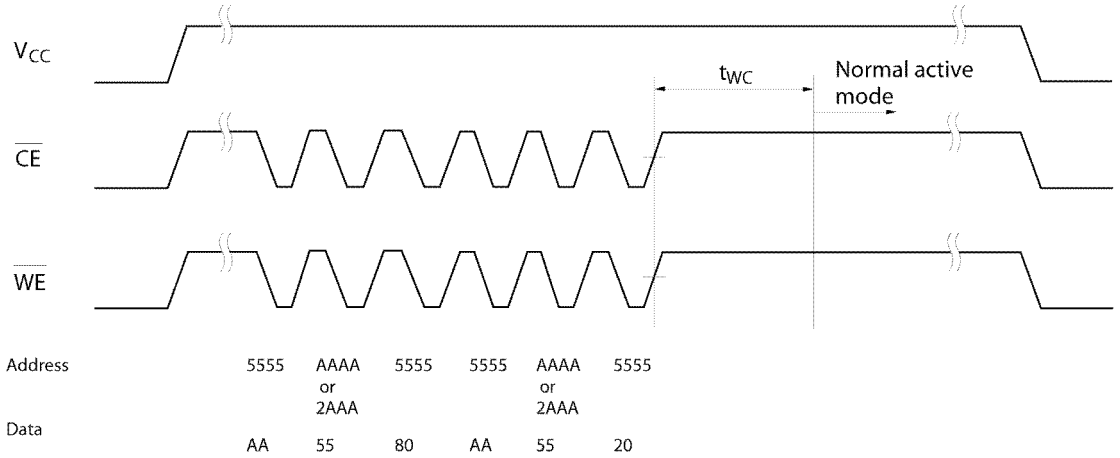


FIGURE 8. $\overline{\text{DATA}}$ POLLING TIMING WAVEFORM

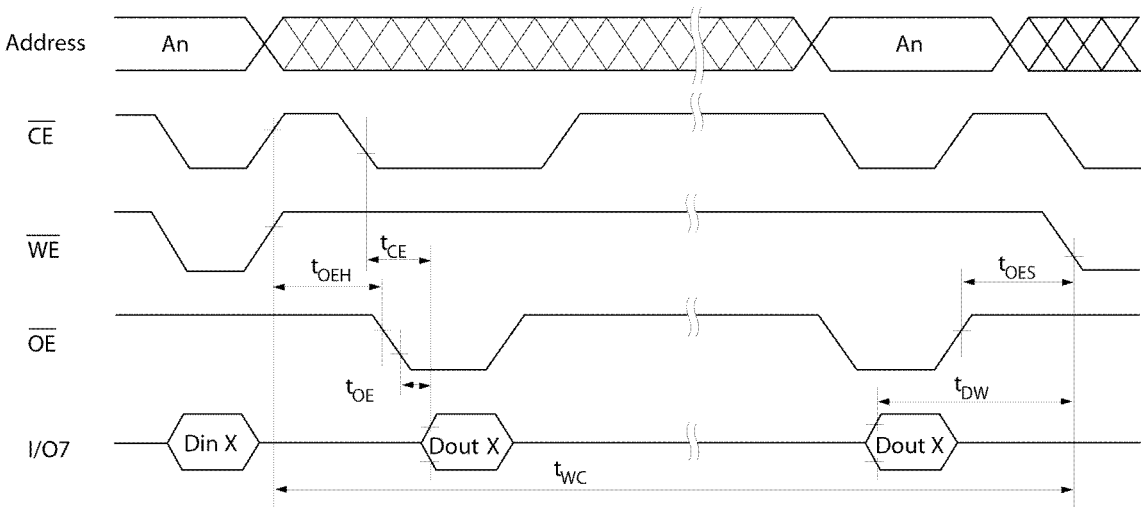


FIGURE 9. TOGGLE BIT WAVEFORM

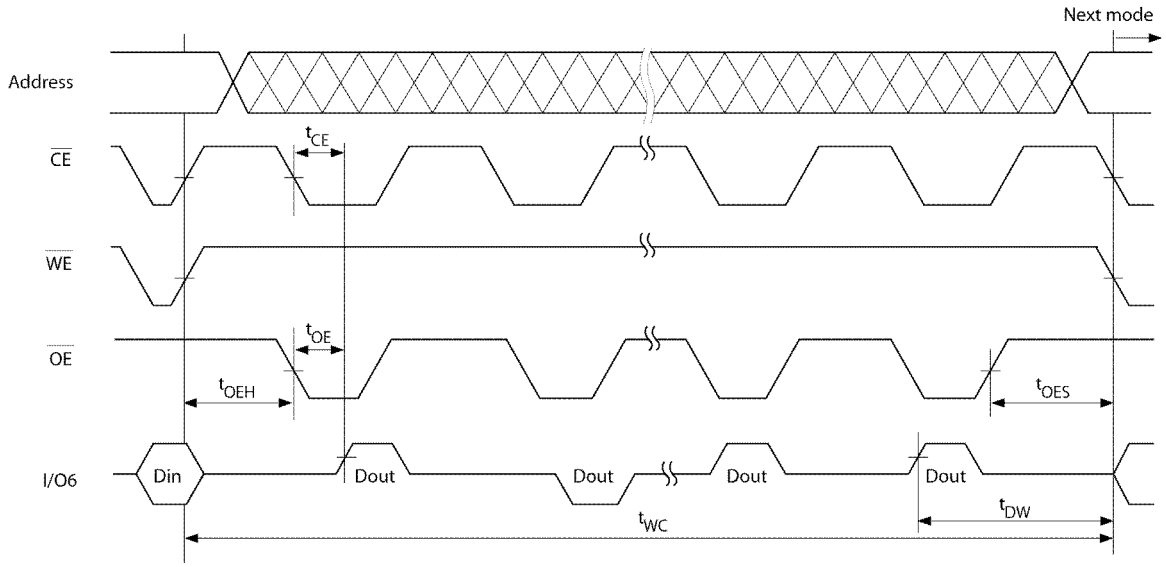


FIGURE 10. SEU SATURATED CROSS SECTION VALUES IN READ MODE

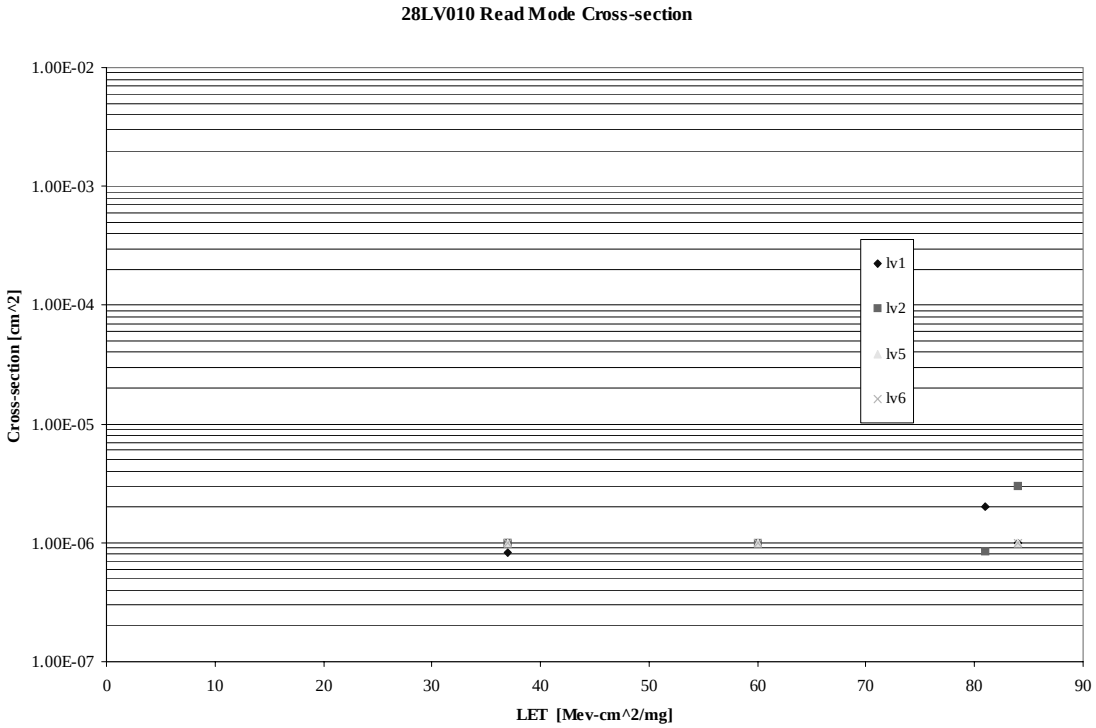
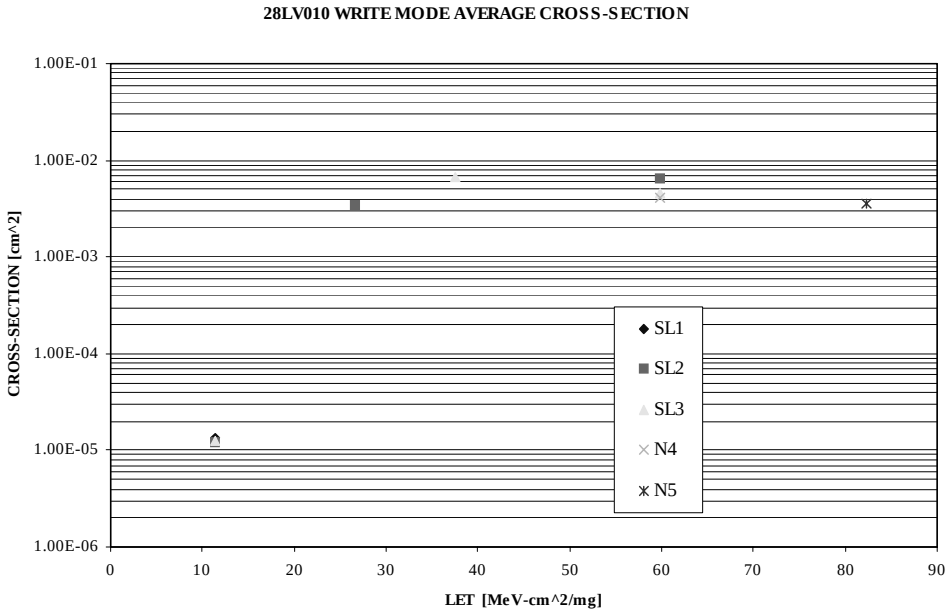


FIGURE 11. SEU SATURATED CROSS SECTION VALUES IN WRITE MODE



EEPROM APPLICATION NOTES

This application note describes the programming procedures for the EEPROM modules and with details of various techniques to preserve data protection.

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle, and allows the undefined data within 128 bytes to be written corresponding to the undefined address (A0 to A6). Loading the first byte of data, the data load window opens 30 µs for the second byte. In the same manner each additional byte of data can be loaded within 30 µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100s after data input, EEPROM enters erase and write mode automatically and only the input data are written into the EEPROM.

$\overline{WE}$ $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

$\overline{Data}$ Polling

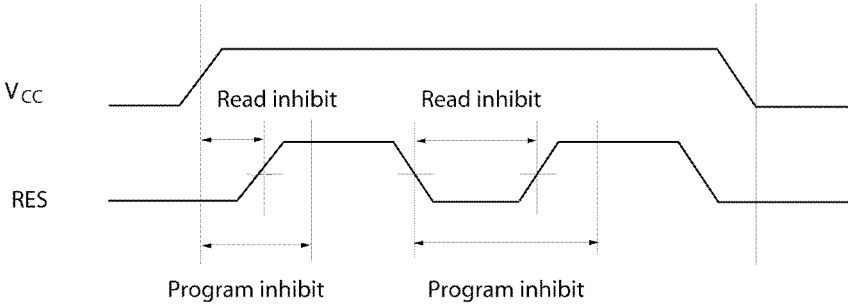
$\overline{Data}$ Polling function allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O 7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{\text{Busy}}$ Signal

RDY/$\overline{\text{Busy}}$ signal also allows a comparison operation to determine the status of the EEPROM. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the-end of a write cycle, the RDY/Busy signal changes state to high impedance.

$\overline{\text{RES}}$ Signal

When $\overline{\text{RES}}$ is LOW, the EEPROM cannot be read and programmed. Therefore, data can be protected by keeping $\overline{\text{RES}}$ low when V_{CC} is switched. $\overline{\text{RES}}$ should be high during read and programming because it doesn't provide a latch function.

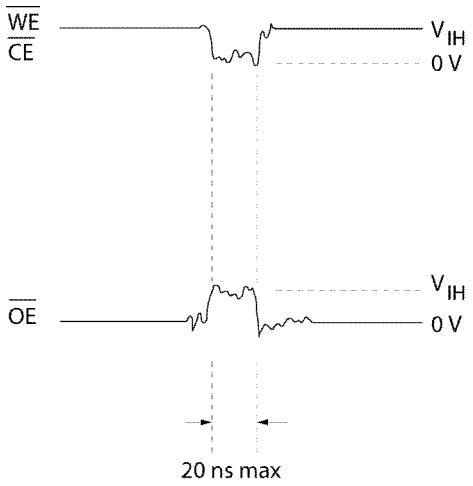


Data Protection

To protect the data during operation and power on/off, the EEPROM has the internal functions described below.

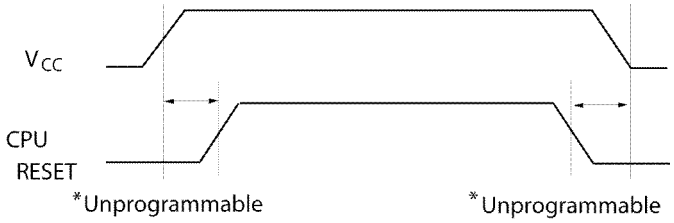
1. Data Protection against Noise of Control Pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during Operation.

   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the EEPROM has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.

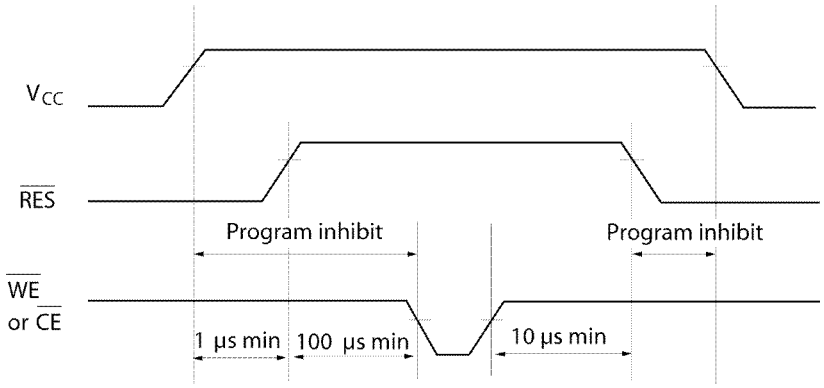


2. Data Protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits, such as CPUs, may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state during V_{CC} on/off by using a CPU reset signal to $\overline{RES}$ pin.



$\overline{RES}$ should be kept at V_{SS} level when V_{CC} is turned on or off. The EEPROM breaks off programming operation when $\overline{RES}$ become low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.



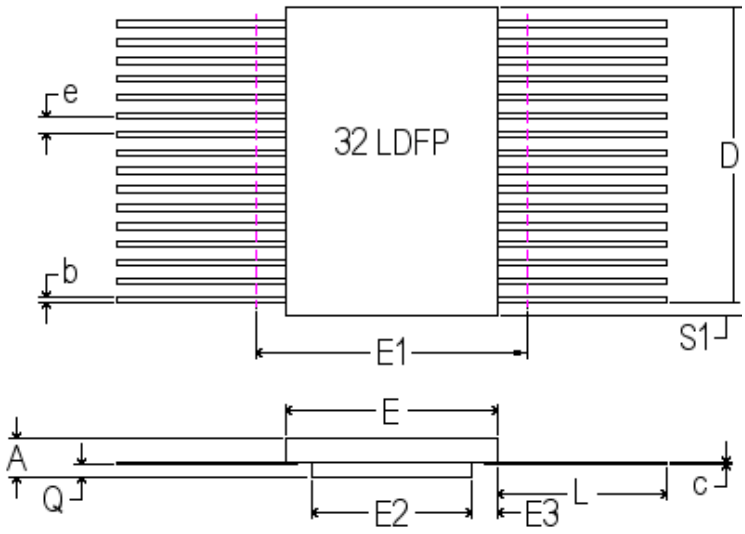
3. Software Data Protection

The software data protection function is to prevent unintentional programming caused by noise generated by external circuits. In software data protection mode, 3 bytes of data must be input before write data as follows. These bytes can switch the non-protection mode to the protection mode.

Address	Data	
5555	AA	
↓	↓	
AAAA or 2AAA	55	
↓	↓	
5555	A0	
↓	↓	
Write address	Write data }	Normal data input

Software data protection mode can be canceled by inputting the following 6 bytes. Then, the EEPROM turns to the non-protection mode and can write data normally. However, when the data is input in the canceling cycle, the data cannot be written.

Address	Data
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	20



32-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.117	0.130	0.143
b	0.015	0.017	0.022
c	0.003	0.005	0.009
D	--	0.820	0.830
E	0.404	0.410	0.416
E1	--	--	0.440
E2	0.234	0.240	--
E3	0.030	0.085	--
e	0.050BSC		
L	0.350	0.370	0.390
Q	0.020	0.035	0.045
S1	0.005	0.027	--
N	32		

F32-01
Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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