VLSI TECHNOLOGY, INC.

VL82C164

QUAD RASTER OP ALU

FEATURES

- Provides simultaneous hardware-assist for bit-mapped graphics operations on four independent memory planes. Includes two 32-bit barrel shifters in each Raster Op section.
- Performance increase over software implementations: 4 x (Planes) x Software
- Supports any type of raster image manipulation, including CRT displays and laser printers
- Implements 256 possible raster operations on source, destination, and pattern data
- 100-lead plastic quad flat pack (PJQFP) package; 5 V supply
- Low power CMOS technology

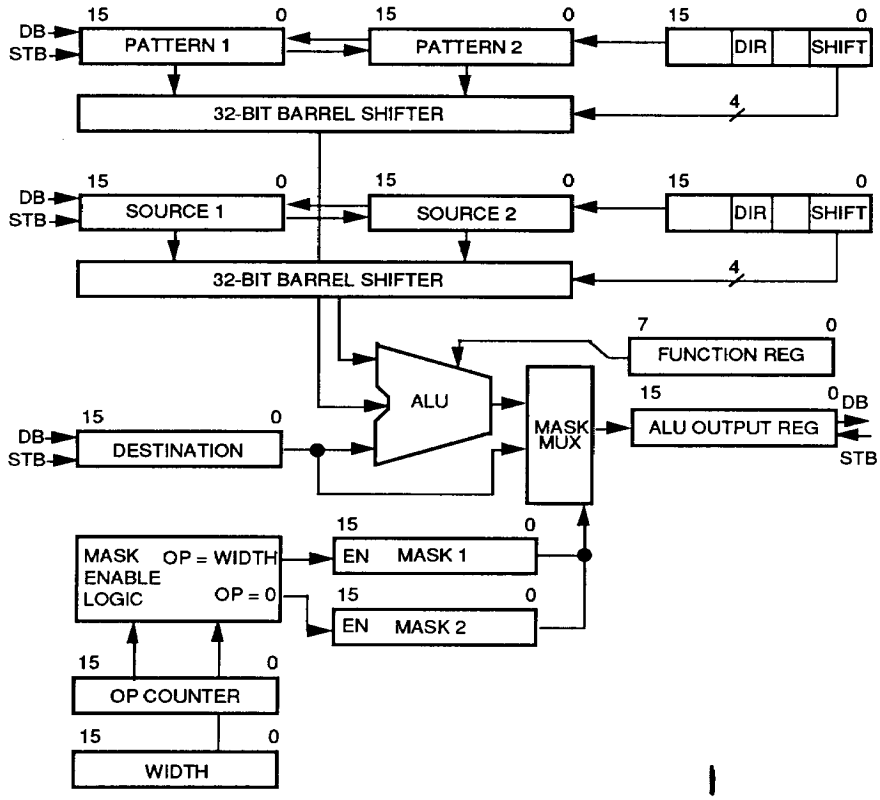
DESCRIPTION

The VL82C164 Quad Raster Op ALU (QRO) provides hardware-assisted performance enhancement for bit manipulation operations in bit-mapped graphics displays. These operations, called bit block translation (BITBLT), allow bit-mapped images to be combined and manipulated by logical operations. These operations include AND, OR, and XOR, as well as a wide range of others which can be arbitrarily defined by the user. The QRO also contains Mask Registers which provide automatic clipping capability at the boundaries of the image section being manipulated.

The BITBLT operation is applicable to a wide variety of graphics operations, including proportionally spaced text display using arbitrary fonts, attributes, and enhancements. Successive applications of BITBLT can perform such operations as scaling, filling, and texturing.

In a typical application, the QRO operates on display data in 16-bit words that are latched into input buffers by external hardware. Source, Destination, Pattern, and Output Registers have dedicated strobe signals, which eliminate the delays associated with address decode. Each of the four independent Raster Op sections has a dedicated chip select to allow maximum speed as well as allowing the same data to be loaded into multiple sections simultaneously. Each section can also be selected via a pair of address lines, allowing a linear address map for host access. For each cycle of operation, the Source and Destination Registers are loaded and the source is aligned according to a previously loaded shift count and combined with the destination and pattern data. The result is written back to the display memory via the dedicated strobe. The QRO can scan forward or backward through the display memory. For cases where only part of the memory word is to be modified, the QRO automatically applies the appropriate mask at each end of the scan.

BLOCK DIAGRAM (Three other Raster Op ALU's are identical.)



ORDER INFORMATION

Part Number	Package
VL82C164-FC	Plastic Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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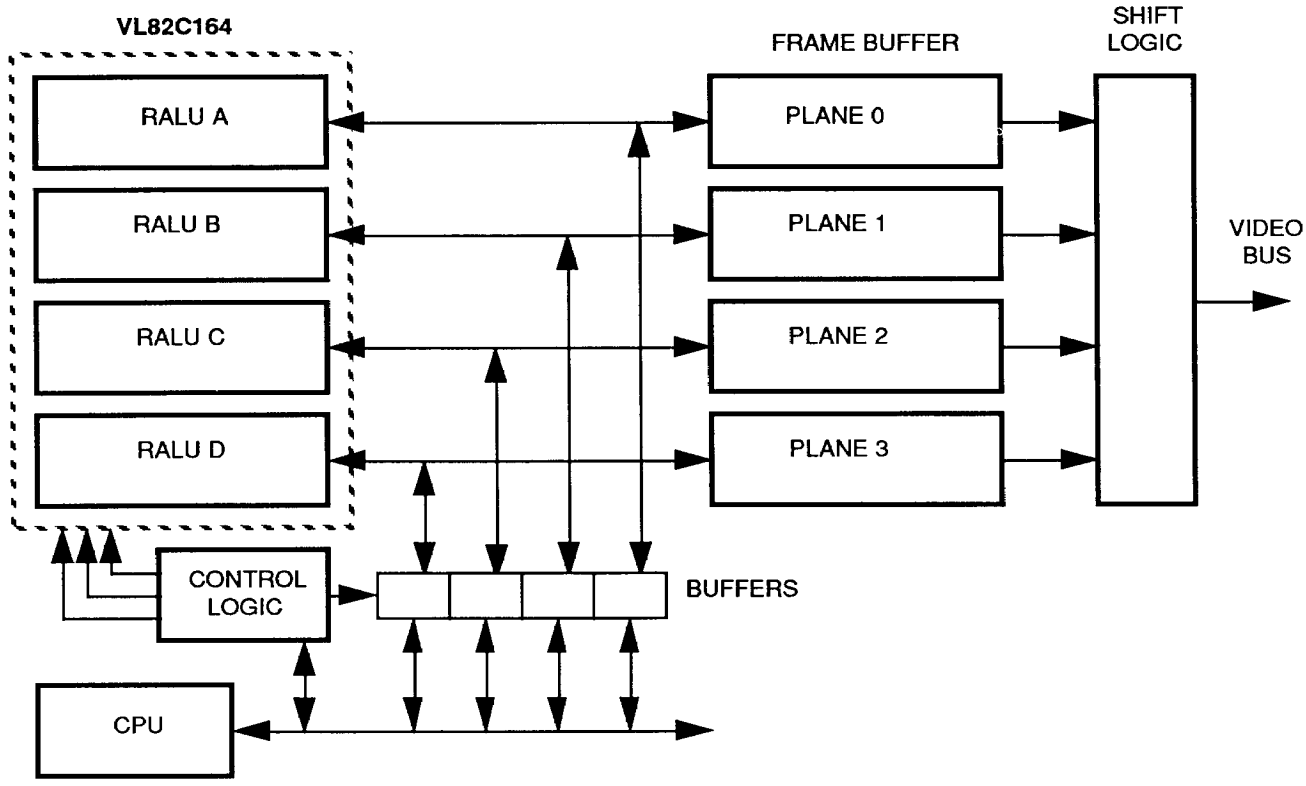
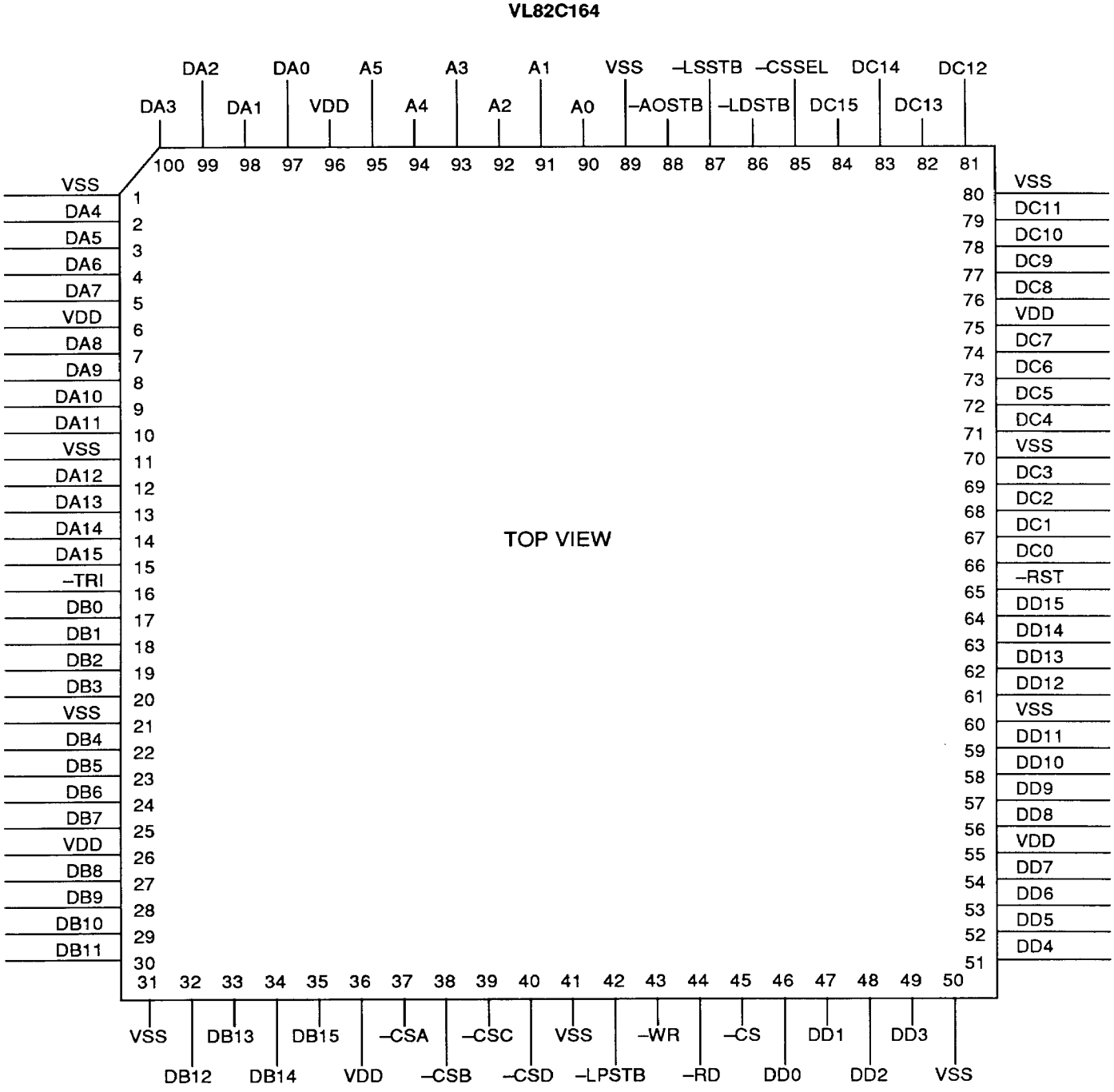
SYSTEM BLOCK DIAGRAM



PIN DIAGRAM

PLASTIC QUAD FLAT PACK (PJQFP)



SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
DA0-DA15	97-100, 2-5, 7-10, 12-15	I/O	Bidirectional data lines for Raster Op Section A enabled by –CSA or A0-A5 and –CS.
–TRI	16	I	Test Pin - Disables output drivers on all I/O lines when low. This pin has an internal pull up resistor.
DB0-DB15	17-20, 22-25, 27-30, 32-35	I/O	Bidirectional data lines for Raster Op Section B enabled by –CSB or A0-A5 and –CS.
–CSA	37	I	Chip Select A - Enables register I/O to Raster Op Section A.
–CSB	38	I	Chip Select B - Enables register I/O to Raster Op Section B.
–CSC	39	I	Chip Select D - Enables register I/O to Raster Op Section D.
–CSD	40	I	Chip Select C - Enables register I/O to Raster Op Section C.
–LPSTB	42	I	Load Pattern Strobe - Loads all four Pattern Registers from their associated data busses according to the Direction Bit in the Pattern Shift Register. The other Pattern Register in the Raster Op section is loaded with the previous contents of the register currently being loaded.
–WR	43	I	Write - Used in conjunction with A0-A5 and –CS to write data into any of the internal registers.
–RD	44	I	Read - Used in conjunction with A0-A5 and –CS to read data from any of the internal registers.
–CS	45	I	Chip Select - This is a General Chip Select signal used in conjunction with A0-A5 and –RD or –WR to access the internal registers.
DD0-DD15	46-49, 51-54, 56-59, 61-64	I/O	Bidirectional data lines for Raster Op Section D enabled by –CSD or A0-A5 and –CS.
–RST	65	I	Reset - This signal, when low, resets the Shift Count and Direction Bit to zero.
DC0-DC15	66-69, 71-74, 76-79, 81-84	I/O	Bidirectional data lines for Raster Op Section C enabled by –CSC or A0-A5 and –CS.
–CSSEL	85	I	CS Select - When low, the Direct Chip Selects (–CSA, –CSB, –CSC, –CSD) are used. When high, the Address Lines (A4,A5) and General Chip Select (–CS) are used.
–LDSTB	86	I	Load Destination Strobe - Loads all four Destination Registers from their associated data busses. The Op Counter is also decremented each time this signal is pulsed.
–LSSTB	87	I	Load Source Strobe - Loads all four Source Registers from their associated data busses according to the Direction Bit in the Shift Count Register. The other source register within the Raster Op section is loaded with the previous contents of the source register currently being loaded.
–AOSTB	88	I	ALU Output Strobe - When low, enables the output of the function decoder (ALU) onto the data bus pins of all four Raster Op sections. This signal should not be active when –CS and –RD or –WR are active.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Type	Signal Description
A0-A5	90-95	I	Register Address - Address inputs which specify which internal register to access for read or write operations. A0-A3 select individual registers within a section, A4 and A5 select which of four sections to access.
VDD	6, 26, 36, 55, 75, 96		Power - The power supply requirement is 5 V ± 5%.
VSS	1, 11, 21, 31, 41, 50, 60, 70, 80, 89		Ground

FUNCTIONAL DESCRIPTION

The VL82C164 contains four complete identical Raster Op sections. Each section consists of five basic components: Source Shifter, Pattern Shifter, Function Decoder, Op Counter, and Mask Registers. The internal data path is 16-bits wide, enabling all internal registers to be accessed easily for context saving and restoring. In normal operation, the Source and Pattern Shifters align the 32-bit source and pattern data from which 16-bit values are extracted and combined with the data in the Destination Register by the Function Decoder. The Op Counter is decremented and, whenever its value equals zero or a user defined width, one of the Mask Registers is activated to clip the resulting value at the BITBLT region boundary, if necessary. The Internal Block Diagram shows how the functional blocks relate to each other and the internal data bus. The System Block Diagram shows how the VL82C164 might be configured with a 16-bit CPU and 256K x 4 VRAMs to implement a high performance 16-color (4-plane) graphics subsystem capable of resolutions up to 2360 x 1770. The following paragraphs describe how each of the major functional subsections work.

SOURCE SHIFTER

The Source Shifter performs bit alignment on the concatenated data in the Source 1 and Source 2 Registers. The number of bits the data is shifted depends on the value in the Source Shift Register. When –LSSTB is strobed, the Source Shifter extracts 16 bits of contiguous data from the concatenated and shifted Source 1 and Source 2 Registers as follows:

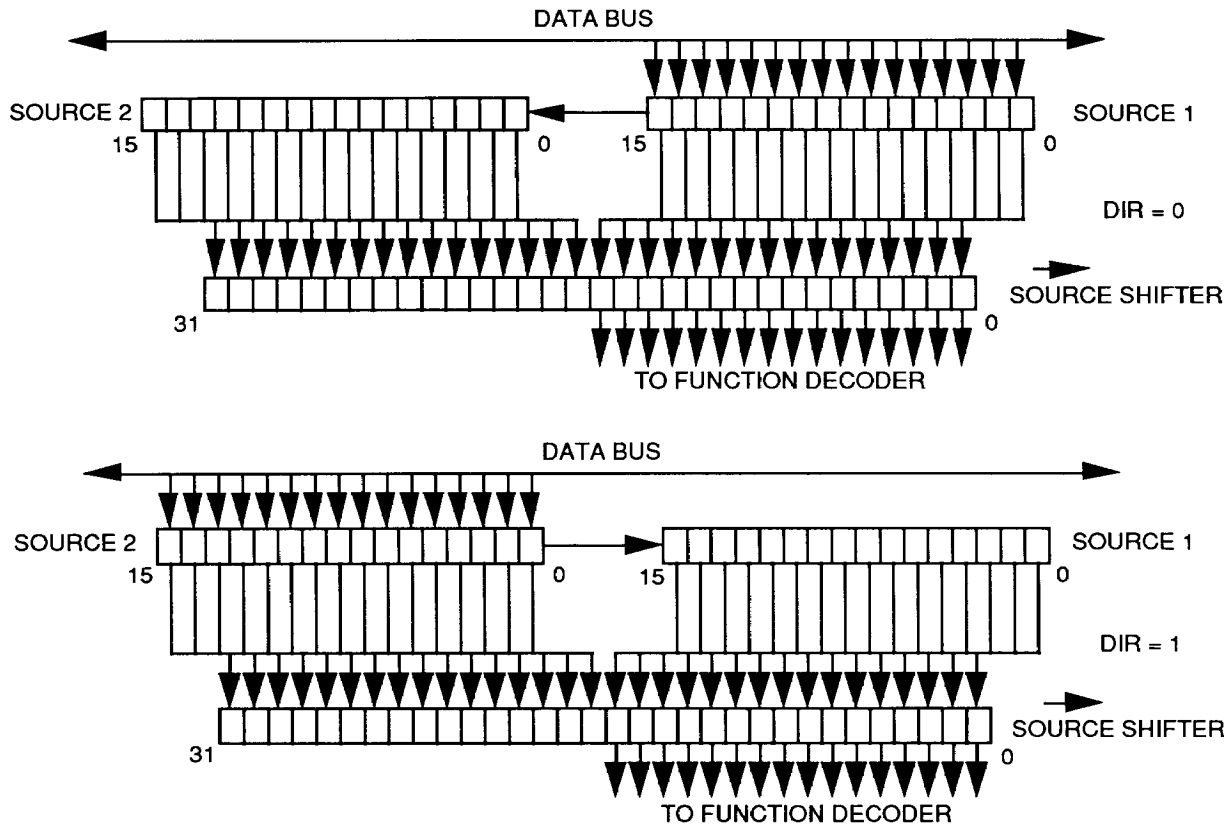
1. If the Direction Bit in the Source Shift Register is zero, each new data word is written to the Source 1 Register, and the previous data from the Source 1 Register is transferred to the Source 2 Register.
2. If the Direction Bit in the Source Shift Register is one, each new data word is written to the Source 2 Register, and the previous data from the Source 2 Register is transferred to the Source 1 Register.
3. Source Shift bits 0 through 3 form a 4-bit shift count. The shift count determines the amount of right shift applied to the 32-bit data in the concatenated Source Registers. The 16-bit result is always extracted from bits 0-15 of the shifter, which correspond to bits 0-15 of the Source 1 Register. The net effect is that if the Direction Bit is one and the shift count is zero, the data from Source 2 is shifted right 16 bits to the extraction point and ends up being passed through unchanged. If the Direction Bit is zero and the shift count is zero, the data from Source 1 is passed through unchanged. If the shift count is other than zero, the data is shifted right by the number of bits specified, regardless of the state of the Direction Bit. (See Figure 1.)

PATTERN SHIFTER

The Pattern Shifter performs bit alignment on the concatenated data in the Pattern 1 and Pattern 2 Registers. The number of bits the data is shifted depends on the value in the Pattern Shift Register. When –LSSTB is strobed, the Pattern Shifter extracts 16 bits of contiguous data from the concatenated and shifted Pattern 1 and Pattern 2 Registers as follows:

1. If the Direction Bit in the Pattern Shift Register is zero, each new data word is written to the Pattern 1 Register, and the previous data from the Pattern 1 Register is transferred to the Pattern 2 Register.
2. If the Direction Bit in the Pattern Shift Register is one, each new data word is written to the Pattern 2 Register and the previous data from the Pattern 2 Register is transferred to the Pattern 1 Register.
3. Pattern Shift bits 0 through 3 form a 4-bit shift count. The shift count determines the amount of right shift applied to the 32-bit data in the concatenated Pattern Registers. The 16-bit result is always extracted from bits 0-15 of the shifter, which corresponds to bits 0-15 of the Pattern 1 Register. The net effect is that if the Direction Bit is one and the shift count is zero, the data from Pattern 2 is shifted right 16 bits to the extraction point and ends up being passed through unchanged. If the Direction Bit is zero and the shift count is zero, the data from Pattern 1 is passed through unchanged. If the shift count is other than zero, the data is shifted right by the number of bits specified, regardless of the state of the Direction Bit. The Pattern Shift Register works essentially the

FIGURE 1. SOURCE SHIFTER



same way as the Source Shift Register. The only difference is that when the –RST input is low, the Pattern Shift Count is reset to zero.

FUNCTION DECODER

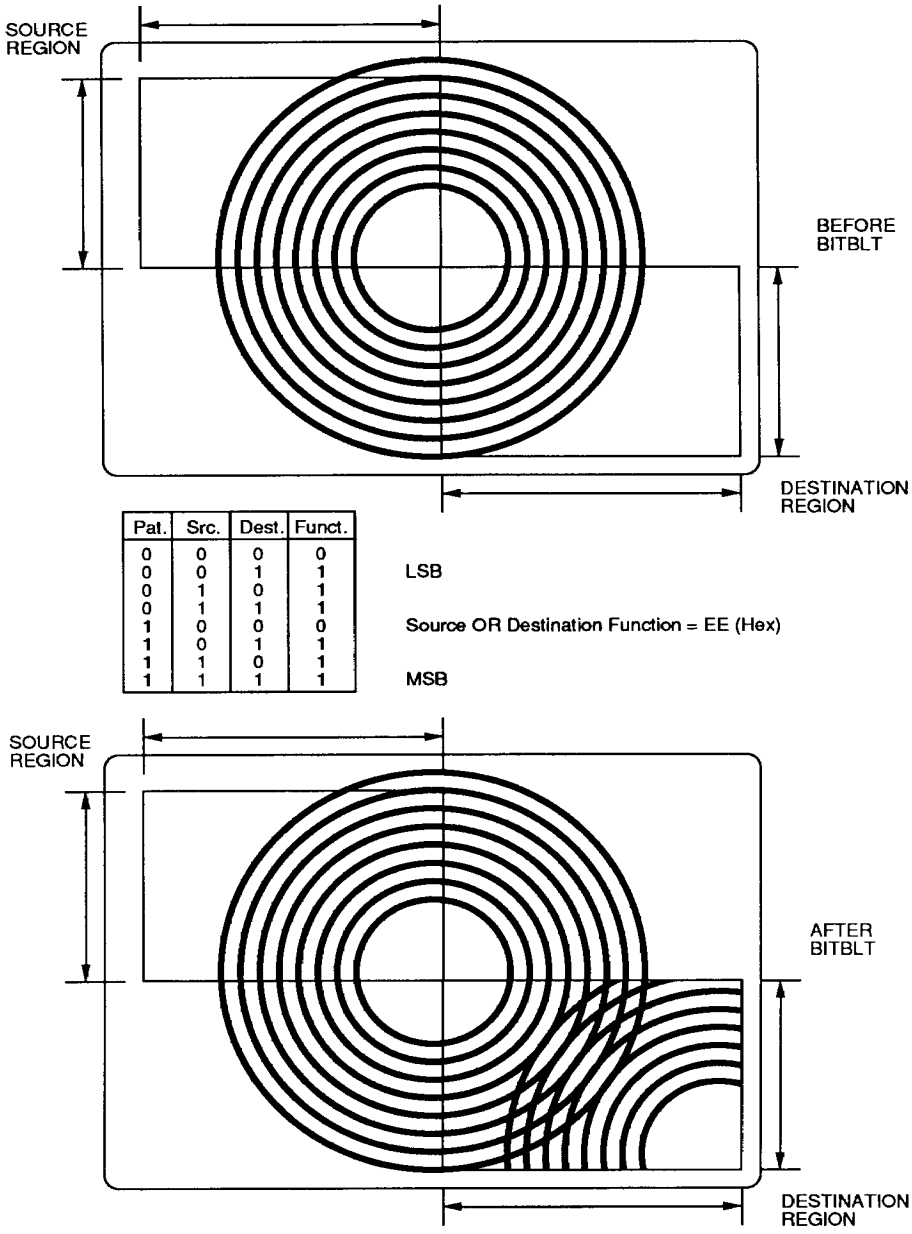
The Function Decoder performs a Boolean operation on the contents of the Destination Register, the output of the Pattern Shifter, and the output of the Source Shifter. The Boolean operation is specified by the Function Register. With the three operands, 256 different Boolean operations are possible. The result of the operation is available on the I/O bus when the –AOSTB control signal is active. The –AOSTB signal must not be active at the same time that –CS and –RD or –WR are active. The result of the Boolean operation is also available by reading the ALU Output Register.

To understand how the Function Decoder performs the desired Boolean operation, note again that with three operands (data in the Source, Pattern and Destination Registers) a total of 256 different Boolean operations are possible. The 8-bit Function Register defines which of the 256 possible functions to use as follows: each bit of the final result is formed as a Boolean combination of the corresponding bits from each of the three operands (Source, Pattern, and Destination). These three bits combine to form a value from 0 to 7 which is used to select a bit from the 8-bit Function Register. In this way, a three-input Boolean function of arbitrary complexity can be formed simply by storing an 8-bit value in the Function Register.

For example (see Figure 2), to "paint" a new image over an existing image requires the source data (image) to be ORed with the destination data (image). This means "Source Register OR the Destination Register". For each bit, there are four possible results of this operation between these two registers. However, since the Pattern Register is always included, even when it is a "don't care," a total of eight different possible results of this one Boolean operation is possible. These eight combinations define the "function code" for the overlay operation. Thus, the function code is really defined as the result (and the only result possible) of a Boolean combination of the Source, Destination, and Pattern Registers. In using the VL82C164, the application defines which of the 256 possible Boolean combinations of the Source, Destination and Pattern Registers define those "functions" required of the application. When that "function" is required, the corresponding function code is loaded into the Function Register.

The function codes required of an application are normally determined ahead of time by the user and stored in memory to be used as needed. The determination of the correct function

FIGURE 2. RASTER OPERATION EXAMPLE



Pat.	Src.	Dest.	Funct.
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

code is a matter of simply applying the definitions stated above (see Block Diagram), in a simple method. The truth table for Pattern, Source, and Destination Bits is written, with the desired output for each combination. This is read as the desired value of the Function Register, with the least significant bit as shown in the Block Diagram. Using this method, the software engineer can easily define a pattern to suit each specific need.

OP COUNTER

The Op Counter, in conjunction with the Width and Mask Registers, provides for masking of selected bits in the Destination Register. This masking prevents the VL16164 from modifying selected areas of display memory when performing BITBLT's. For example, clipping may be required at the edges of a window. The function of the Op Counter is to keep track of the beginning and end of each row, so that the Mask Registers can handle this clipping automatically, without additional processor intervention.

The Op Counter should be initialized to the same value as the Width Register prior to the beginning of a raster operation, and is internally clocked by the –LDSTB signal. Masking is enabled by the first –LDSTB pulse after loading the Op Counter. If context switching is utilized, reinitialization (including loading the Op Counter) is necessary upon re-entering a context in the middle of a BITBLT.

EXAMPLE

Figures 3, 4 and 5 illustrate how a single row from a block of pixels might be processed. Neither the source nor the destination regions are aligned on word boundaries, to show how the shift and mask logic works. There are three cases illustrated: the first and last word in the row, which are masked, and the remaining words, which are not masked. Figure 3 shows how the source and destination region boundaries relate to the memory word boundaries, how the Mask Registers relate to the destination boundaries, and how the shift value corresponds to the relative source and destination boundary positions. In this case, the shift value accounts for the entire horizontal displacement of the image, but this need not be the case. The true meaning of the shift value is relative to the destination word boundary, which may be anywhere in memory. Figure 3 also shows how the first word of the destination region is derived: source words 1 and 2 are concatenated and shifted to align the source region boundary with the destination region boundary, the existing destination word is combined with the resulting source word under Mask 1 and according the programmed function, and the modified destination word is written back into memory. Figure 4 shows how destination words 2 and 3 would be processed. This is exactly the same as for word 1 except that no masking is done, since no boundaries are involved. Figure 5 shows how the last word of the destination region is derived: source words 4

FIGURE 3. PIXEL ROW FIRST WORD

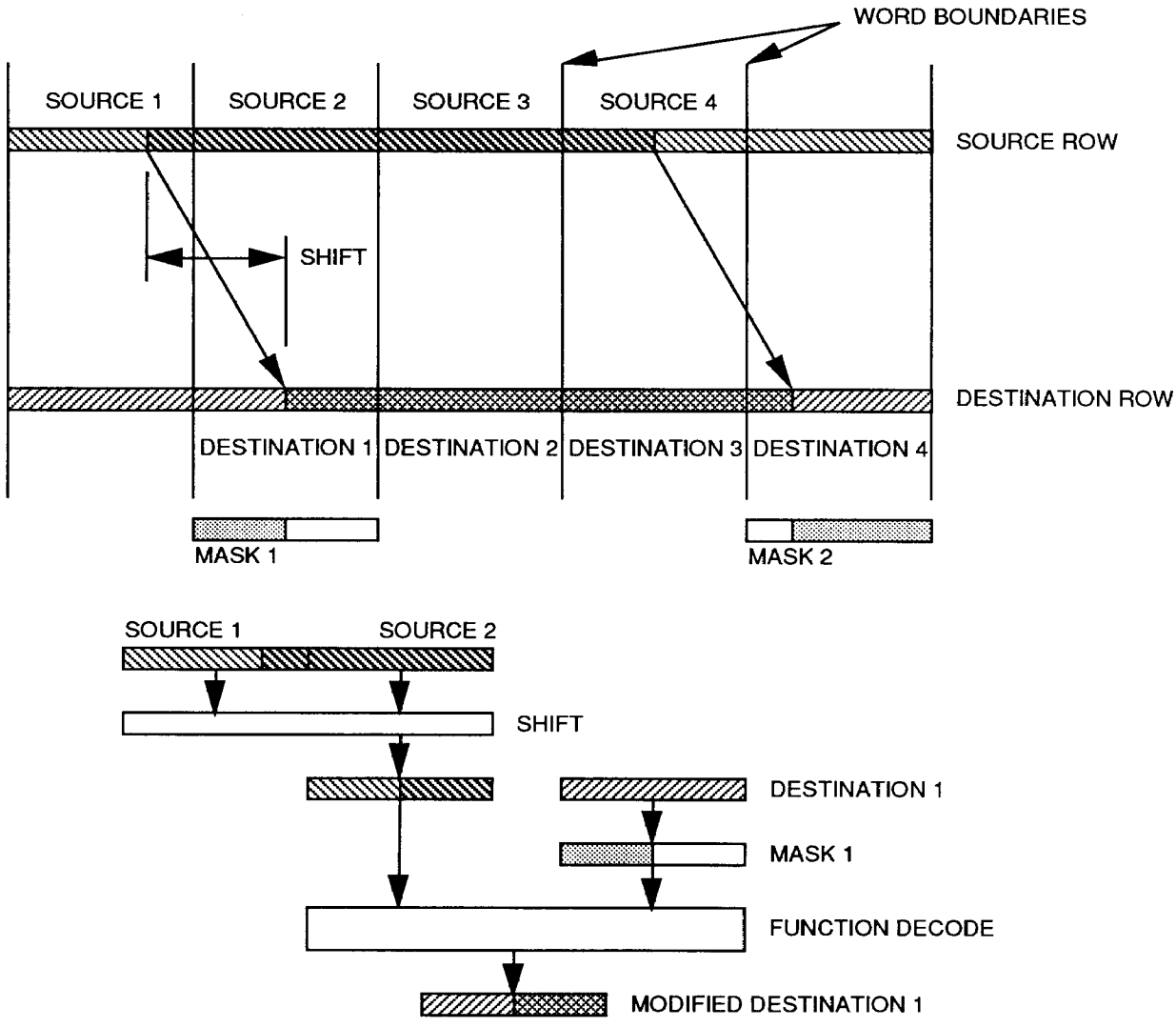


FIGURE 4. PIXEL ROW SECOND WORD

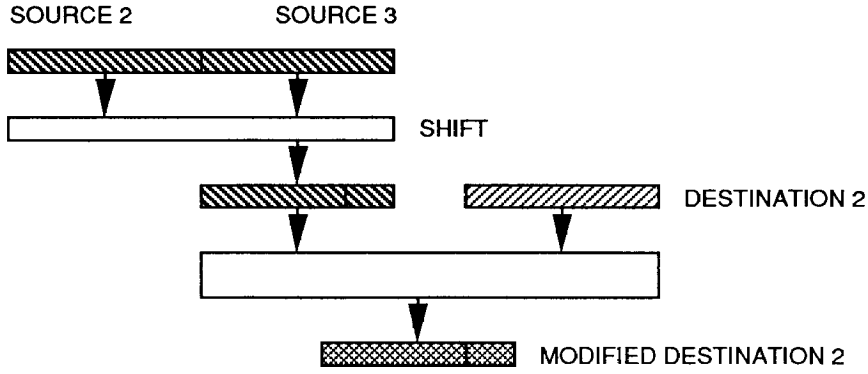
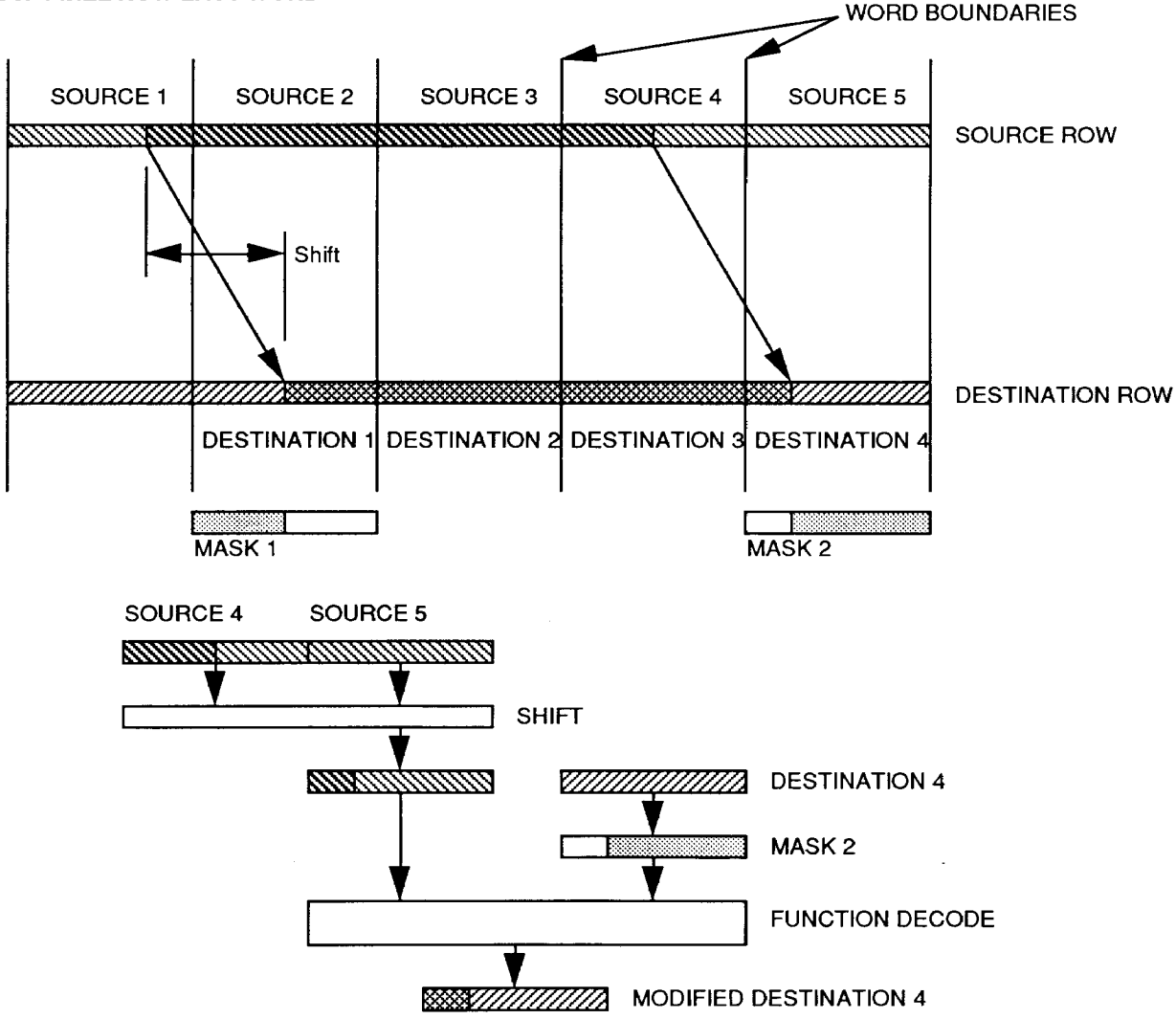


FIGURE 5. PIXEL ROW LAST WORD



and 5 are concatenated and shifted to align the source region boundary with the destination region boundary, the existing destination word is combined with the resulting source word under Mask 2 and according the programmed function, and the modified destination word is written back into memory. This whole process would then be repeated for every row in the block of pixels to be transferred.

REGISTER DESCRIPTIONS

As shown in the Block Diagram, each Raster Op segment consists of a number of registers, each connected to the internal 16-bit data path. Of these registers, four are used very often and are directly accessible from the data bus by the assertion of strobe signals.

SOURCE

The Source Register holds a 16-bit word of data to be modified by a raster operation. It is loaded from the data bus by the assertion of the –LSSTB signal.

PATTERN

The Pattern Register holds a 16-bit word of data to be combined with source and destination data. It is loaded from the data bus by the assertion of the –LPSTB signal.

DESTINATION

The Destination Register holds a word of data from the bit-mapped display that is modified by the source data and raster operation. It is loaded from the data bus when –LDSTB is asserted.

ALU OUTPUT

The ALU Output Register holds the result of the raster operation to be written back to memory. The contents may be put onto the data bus by the assertion of the –AOSTB signal.

The remainder of the registers are typically set up for a series of operations and are not changed until the end of a scan line.

SOURCE DIR / SHIFT

This register controls the direction of the raster operation (left-to-right or right-to-left). In addition, it specifies the number of bits to shift to align the source with the destination fields.

PATTERN DIR / SHIFT

This register controls the direction of the raster operation (left-to-right or right-to-left). In addition, it specifies the number of bits to shift to align the pattern with the destination fields.

MASK 1 AND 2

These registers are used to define the left and right boundaries of the area on the screen that is manipulated. (The Direction Bit affects which register corresponds to left versus right.) A bit set in these registers allows the corresponding bit in the Destination Register to pass through unaltered. When the Op Counter is equal to the Width Register (usually for the first raster operation on each scan line), the Mask 1 Register selects bits to be included in the operation. Masking is disabled until the Op Counter is zero (usually for the last operation on a scan line); at that time, the Mask 2 Register is used.

FUNCTION

This register contains the operator that is used to combine the source, destination, and pattern data.

OP COUNTER

The Op Counter Register specifies the current count of the operation in progress. The Op Counter is decremented each time –LDSTB is brought active. After the Op Counter goes to zero, the next –LDSTB causes the Op Counter to be reloaded with the value of the Width Register prior to the next operation.

WIDTH

The Width Register specifies the width of the line (in 16-bit words) on which raster operations will take place, minus one.

FLAG REGISTER

The Flag Register is uncommitted and can be used to temporarily store context information for multi-tasking implementations.

TABLE 1. REGISTER MAP

Register Address				Register Name
A3	A2	A1	A0	
0	0	0	0	Destination
0	0	0	1	Source 1
0	0	1	0	Source 2
0	0	1	1	Pattern 1
0	1	0	0	Mask 1
0	1	0	1	Mask 2
0	1	1	0	Source Shift
0	1	1	1	Function
1	0	0	0	Width
1	0	0	1	Op Count
1	0	1	0	ALU Output
1	0	1	1	Pattern 2
1	1	0	0	Pattern Shift
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Flag

TABLE 2. SECTION MAP

Section Address		Raster Op Section
A5	A4	
0	0	Raster Op A
0	1	Raster Op B
1	0	Raster Op C
1	1	Raster Op D

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ± 5%, VSS = 0 V, Capacitive Load = 50 pF

REGISTER READ TIMING (SEE FIGURE 6.)

Symbol	Parameter	Min.	Max.	Units	Condition
tD1	Data Valid after –CS Active and A0-A5 Valid	–	52	ns	(–RD Active)
tD2	Data Valid after –RD Active	–	45	ns	(–CS Active)
t3	–RD Signal Pulse Width	45	–	ns	
tH4	Data Hold after –RD, –CS Inactive	5	–	ns	

REGISTER WRITE TIMING (SEE FIGURE 7.)

Symbol	Parameter	Min.	Max.	Units	Condition
tSU5	–CS, A0-A5 Setup to –WR Active	5	–	ns	
t6	–WR Signal Pulse Width	30	–	ns	
tSU7	Data Setup to –WR Inactive	9	–	ns	
tH8	Data Hold after –WR Inactive	19	–	ns	
tH9	–CS, A0-A5 Hold after –WR Inactive	8	–	ns	

DIRECT STROBE CONTROL SIGNAL TIMING (SEE FIGURE 8.)

Symbol	Parameter	Min.	Max.	Units	Condition
t10	–LPSTB Pulse Width	10	–	ns	
t11	–LSSTB Pulse Width	9	–	ns	
t12	–LDSTB Pulse Width	10	–	ns	
tSU13	Data Setup to –LPSTB Inactive	10	–	ns	
tH14	Data Hold after –LPSTB Inactive	9	–	ns	
tSU15	Data Setup to –LSSTB Inactive	10	–	ns	
tH16	Data Hold after –LSSTB Inactive	9	–	ns	
tSU17	Data Setup to –LDSTB Inactive	10	–	ns	
tH18	Data Hold after –LDSTB Inactive	9	–	ns	
tD19	Output Valid after –AOSTB Active	–	44	ns	
tD20	Output Valid after –LDSTB Inactive	–	71	ns	
tD21	Output Valid after –LSSTB Inactive	–	80	ns	
tD22	Bus High Impedence after –AOSTB Inactive	–	25	ns	(Note 1)
t23	Time Between –LSSTB Pulses	89	–	ns	
t24	Time Between –LDSTB Pulses	89	–	ns	
t25	–LSSTB Inactive to –AOSTB Active	36	–	ns	
t26	–LDSTB Inactive to –AOSTB Active	17	–	ns	

Note 1: As measured from ±0.5 V from worst case static VOH/VOL levels.

FIGURE 6. REGISTER READ TIMING

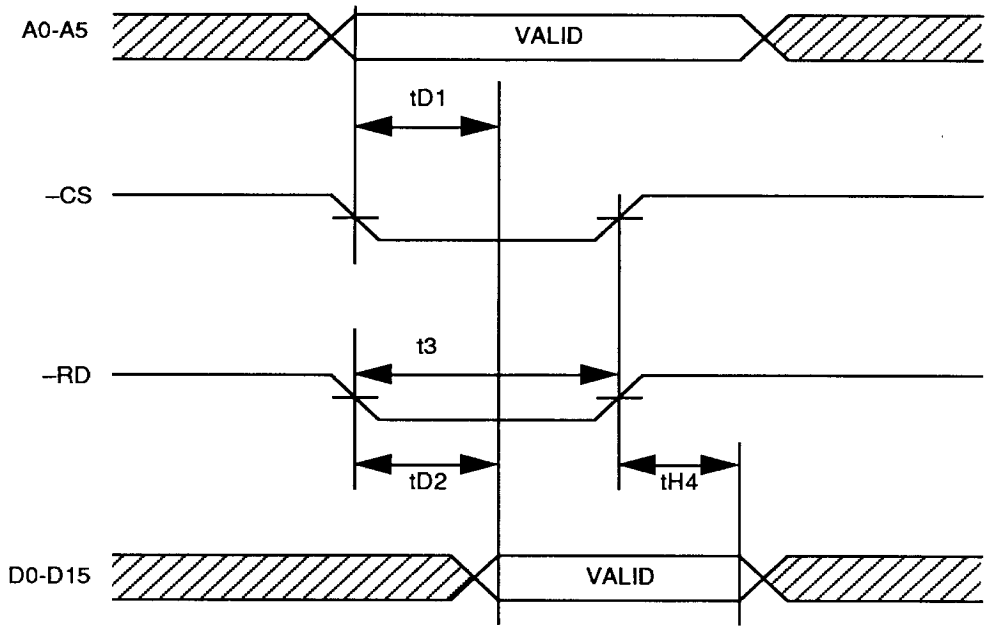


FIGURE 7. REGISTER WRITE TIMING

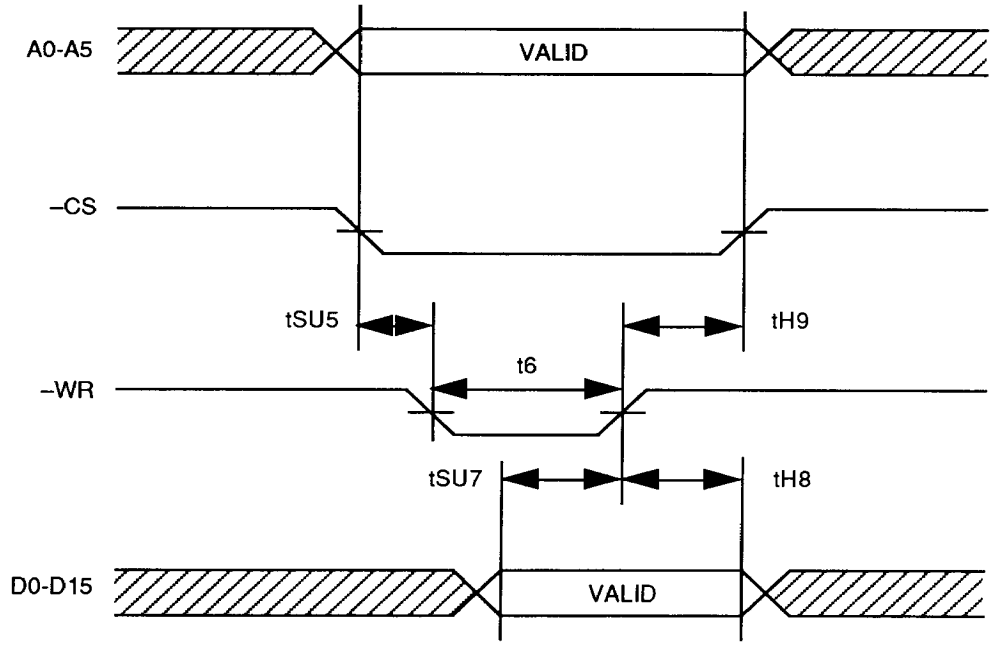
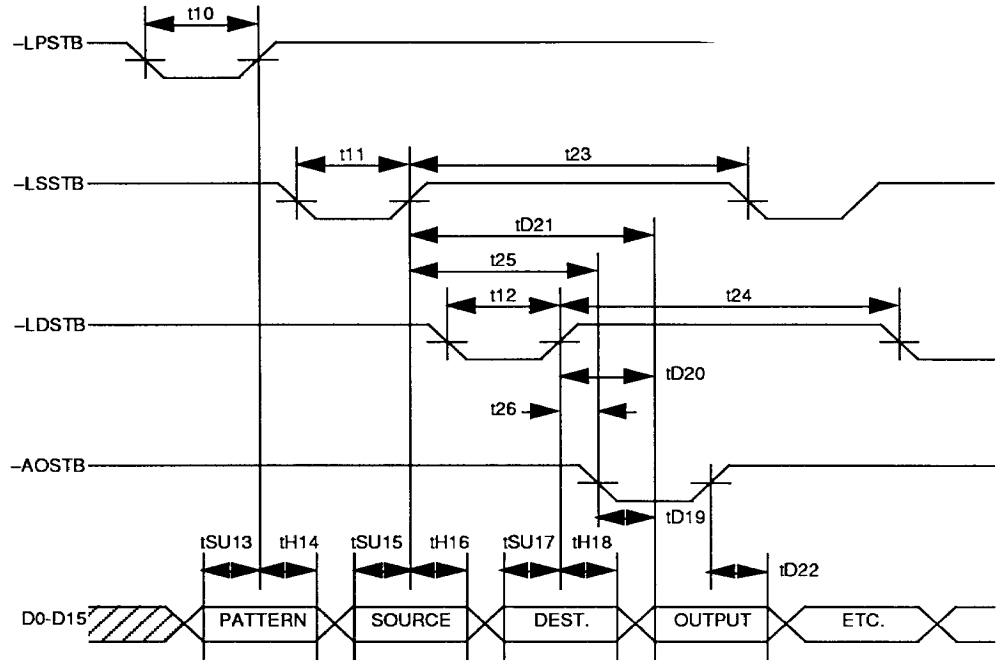


FIGURE 8. DIRECT STROBE CONTROL SIGNAL TIMING



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–40°C to +125°C
Supply Voltage to Ground Potential	–0.5 V to VDD +6.0 V
Applied Input Voltage	–0.5 V to VDD +0.5 V
DC Input Current	±20 mA
Lead Temperature	300°C

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

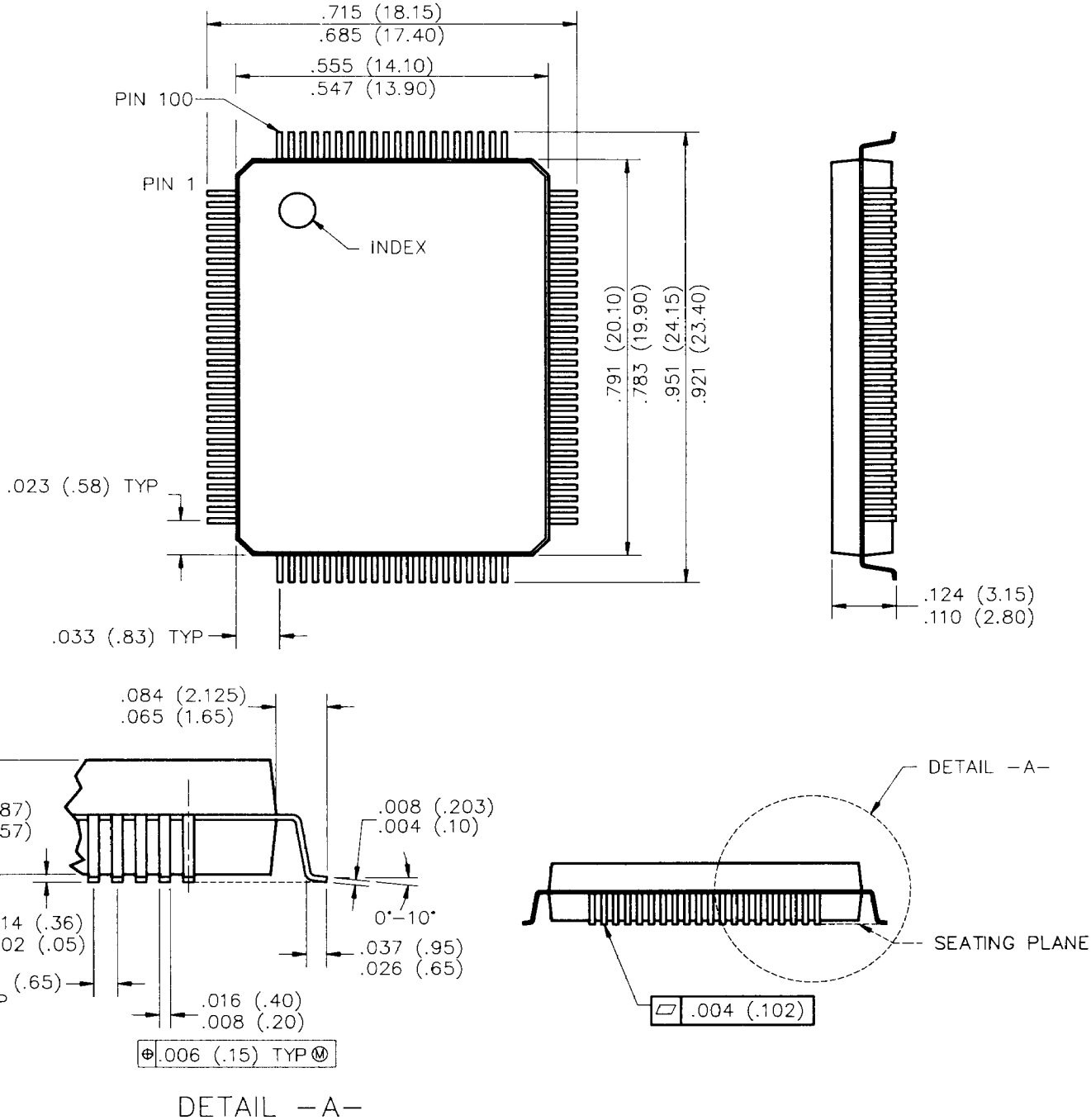
DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ± 5%, VSS = 0 V, Capacitive Load = 50 pF

Symbol	Parameter	Min.	Type	Max.	Units	Condition
VIH	Input High Voltage	2.0	–	VDD	V	VDD = 5.25 V
VIL	Input Low Voltage	–0.5	–	0.8	V	VDD = 5.25 V
VOH	Output High Voltage	2.4	–	–	V	IOH = –8 mA
VOL	Output Low Voltage	–	–	0.4	V	IOL = 8 mA
IIN	Input Leakage Current	–10	–	+10	µA	VIN = VDD/VSS (Note 2)
IIN –TRI	Tri-Input Leakage Current	– –	– –	+10 –300	µA µA	VIN = VDD VIN = VSS
IOZ	High Impedence Output Leakage	–10	–	+10	µA	VOUT = VDD/VSS
IDD	Dynamic Current Drain @ 1.0 MHz	– –	– 9.0	15 –	mA mA/MHz	VDD = 5.25 V

Note 2: Does not apply to pin 16, –TRI input.

PACKAGE OUTLINE

100-LEAD PLASTIC QUAD FLAT PACK



NOTES:

1. CONTROLLING DIMENSION IS MM.

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