3.5.4 Port 3 (P30~P37)

Port 3 is an 8-bit general-purpose I/O port P3 with fixed I/O function. All bits of the output latch are initialized to "1" by resetting, and "High level" is generated to the output port.

In addition to the I/O port function, P30~P34 have the I/O function for the internal serial interface, while P35~P37 have the external memory control function. The additional functions can be selected by the control register P3CR. All bits of the control register are initialized to "0" by resetting, and the port turns to the general-purpose I/O Ports mode.

However, access of an external memory makes P35~P36 automatically function as the memory control pins ($\overline{RD}$ and $\overline{WR}$), and access of an internal memory makes them function as general-purpose I/O ports.

When an external memory is accessed, therefore, the output latch registers P35 ($\overline{RD}$) and P36 ($\overline{WR}$) should be kept at "1" which is the initial value after the reset.

The P3CR <RDE> of the control register is intended for a pseudostatic RAM. When set to "1", it always functions as an $\overline{RD}$ pin. Therefore the $\overline{RD}$ pin outputs "0" (Enable) when it is an internal memory read and internal I/O read cycle.

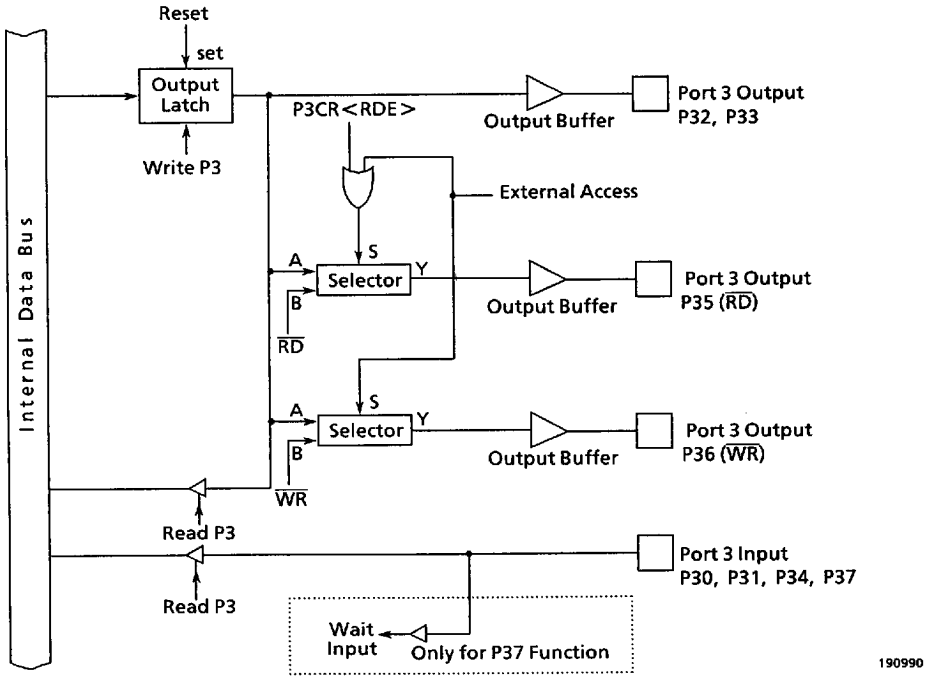

Figure 3.5 (6) Port 3

Port 3 Register

P3 (FFC6H)	7	6	5	4	3	2	1	0
bit Symbol	P37	P36	P35	P34	P33	P32	P31	P30
Read/Write	R	R/W	R/W	R	R/W	R/W	R	R
Resetting Value	Input	1	1	Input	1	1	Input	Input

Port 3 Control Register

P3CR (FFC7H)	7	6	5	4	3	2	1	0
bit Symbol	WAITC1	WAITC0	RDE	ODE	TXDC1	TXDC0	RXDC1	RXDC0
Read/Write	R/W		R/W	R/W	R/W		R/W	
Resetting Value	0	0	0	0	0	0	0	0
Function	Wait Control 00: 2state wait 01: normal wait 10: non wait 11: Not used		RD Control 0: $\overline{RD}$ for only external access 1: Always $\overline{RD}$	P33 Control 0: CMOS Output 1: Open Drain Output	P33 P32 00: Out Out 01: Out TxD 10: TxD Out 11: TxD $\overline{RTS}$/SCLK		P31 P30 00: In In 01: In RxD 10: RxD In 11: Not used	

See "3.8 Serial Channel"

Set port P33 to open drain output

0	CMOS output
1	Open drain output

Set port P35 to fixed $\overline{RD}$ mode

0	General-purpose I/O port
1	Fixed as $\overline{RD}$ Pin

WAIT control

00	2-state wait
01	Normal wait
10	No wait (used as an Input port)
11	Not used

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Figure 3.5 (7) Register for Ports 3

3.5.5 Port 4 (P40~P43)

Port 4 is a 4-bit port P4 intended only for the output. All bits of the output latch are initialized to "0" by resetting, and "0" is generated to the port.

In addition to the output port function, it works as an address bus (A16~A19). The selection of the address bus function is made by the control register P4CR. The output port or address bus function can be selected for each bit. All bits of the control register are initialized to "0" by resetting, and the port turns to the output mode.

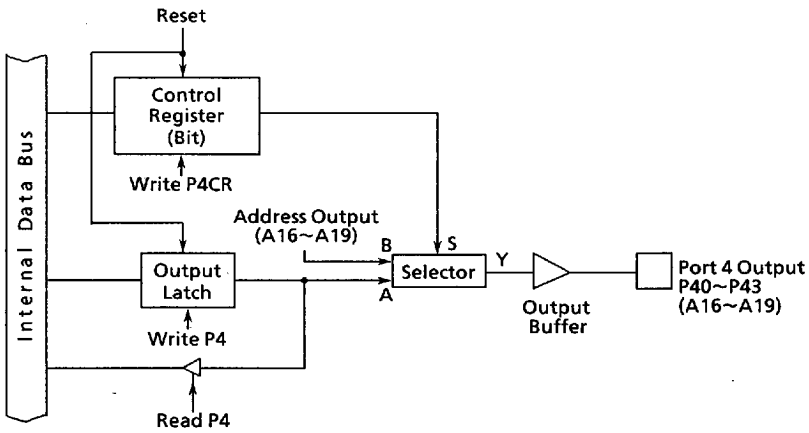

Figure 3.5 (8) Port 4