
HB 56RW872ES Series

8,388,608-Word x 72-Bit(ECC) High Density Dynamic RAM
Module

HITACHI

Preliminary
Rev. 0
Dec. 19, 1995

The HB56RW872ES belongs to 8 Byte DIMM (Dual In-Line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications.

The HB56RW872ES is a 8M x 72 dynamic RAM module, mounted 36 pieces of 16-Mbit DRAM (HM51W16400) sealed in TCP package and 2 pieces of 16-bit BiCMOS line driver (74LVT16244) sealed in TSSOP package.

An outline of the HB56RW872ES is 168-pin socket type package (dual-lead out).

Therefore, the HB56RW872ES makes high density mounting possible without surface mount technology. The HB56RW872ES provides common data inputs and outputs.

Decoupling capacitors are mounted beside each TCP on its module board.

Features

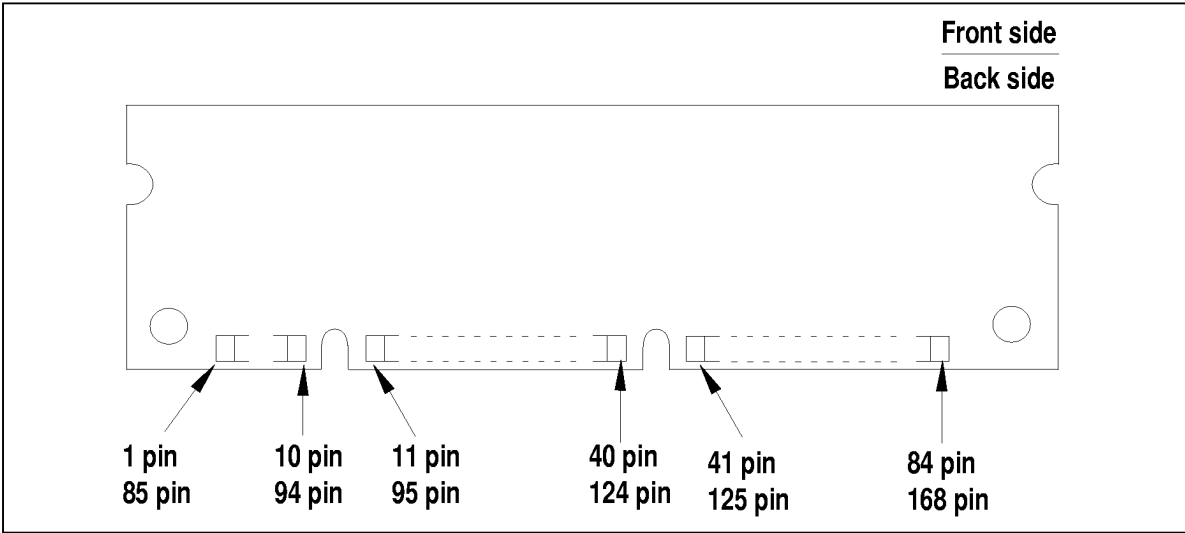
- 168-pin socket type package (Dual lead out)
 - Lead pitch: 1.27 mm
- Single 3.3 V (± 0.3 V) supply
- High speed
 - Access time: $t_{RAC} = 60/70/80$ ns (max.)
 - Access time: $t_{CAC} = 20/23/25$ ns (max.)
- Low power dissipation
 - Active mode: 5.54/4.90/4.57W (max.)
 - Standby mode: 295mW (max.)
- Buffered input except/RAS and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- Fast page mode capability
- 4,096 refresh cycle/64 ms
- 2 variations of refresh
 - /RAS - only refresh
 - /CAS - before - /RAS refresh

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Ordering Information

Type No.	Access time	Package	Contact pad
HB56RW872ES-6B	60ns	168-pin dual lead out socket type	Gold
HB56RW872ES-7B	70ns		
HB56RW872ES-8B	80ns		

Pin Arrangement



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Pin Arrangement

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	/OE2	86	DQ36	128	NC
3	DQ1	45	/RE2	87	DQ37	129	/RE3
4	DQ2	46	/CE4	88	DQ38	130	/CE5
5	DQ3	47	NC	89	DQ39	131	NC
6	Vcc	48	/WE2	90	Vcc	132	/PDE
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE0	69	DQ28	111	NC	153	DQ64
28	/CEO	70	DQ29	112	/CE1	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	/RE0	72	DQ31	114	/RE1	156	DQ67
31	/OE9	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ32	116	VSS	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss

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37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	NC	83	ID0 (Vss)	125	NC	167	ID1
42	NC	84	Vcc	126	B0	168	Vcc

Pin Description

Pin Name	Function
A0 to A11, B0	Address Input Row Address Column Address Refresh Address A0 to A11, B0 A0 to A11, B0 A0 to A9, B0 A0 to A11, B0
DQ to DQ71	Data - in / Data - out
/RE0 to RE3	Row Address Strobe
/CE0, /CE1, /CE4, /CE5	Column Address Strobe
/WE0, /WE2	Read / Write Enable
/OE0, /OE2	Output Enable
Vcc	Power Supply
Vss	Ground
PD1 to PD8	Presence Detect
ID0, ID1	ID bit
/PDE	Presence Detect Enable
NC	Non Connection

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Presence Detect Pin Assignment

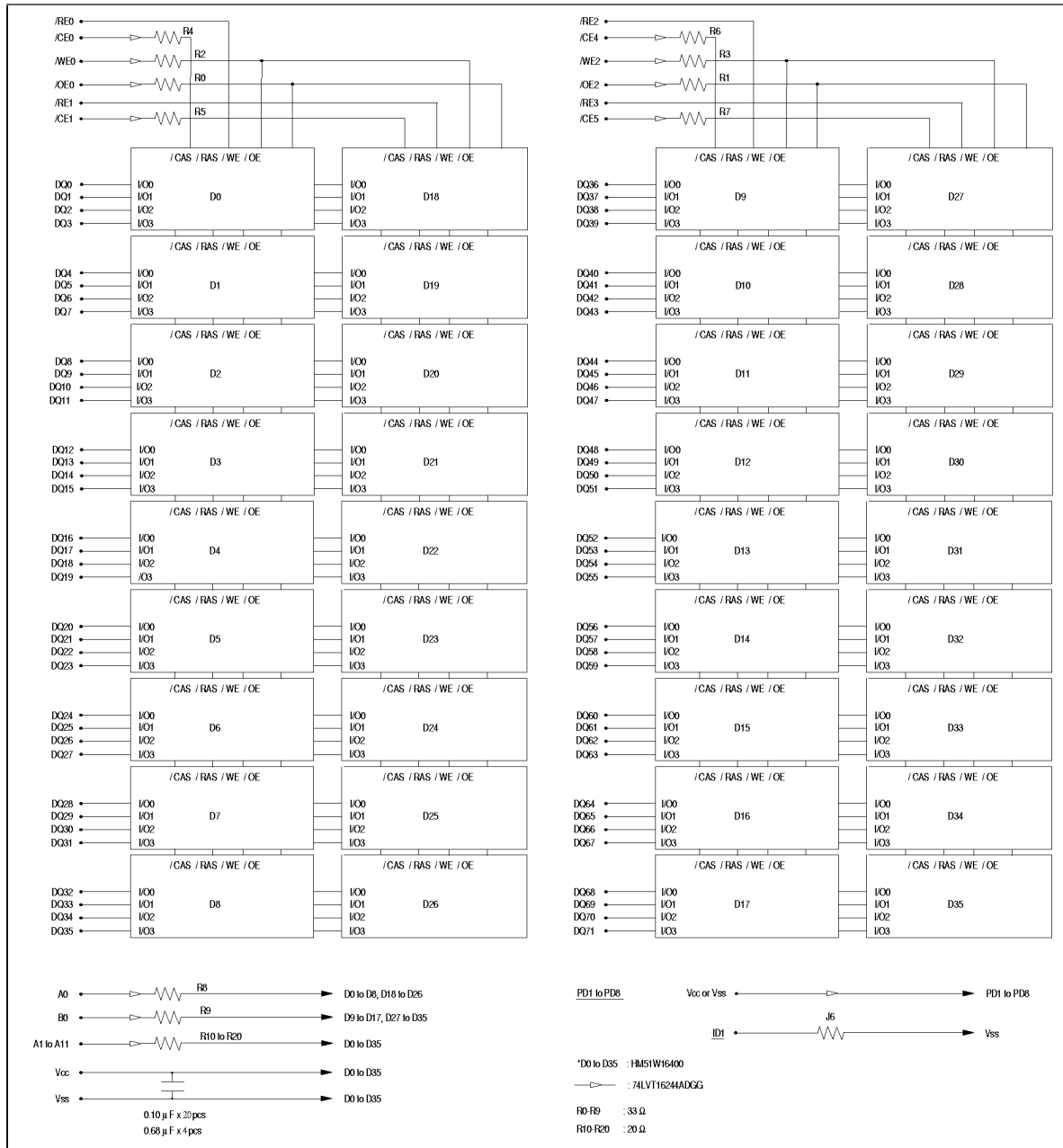
Pin Name	Pin No,	/PDE=Low			/PDE=High	
		-6B	-7B	-8B	All	
PD1	79	0	0	0	High-Z	
PD2	163	0	0	0	High-Z	
PD3	80	1	1	1	High-Z	
PD4	164	1	1	1	High-Z	
PD5	81	0	0	0	High-Z	
PD6	165	1	0	1	High-Z	
PD7	82	1	1	0	High-Z	
PD8	166	0	0	0	High-Z	

1 : High Level (Driver Output)

0 : Low Level (Driver Output)

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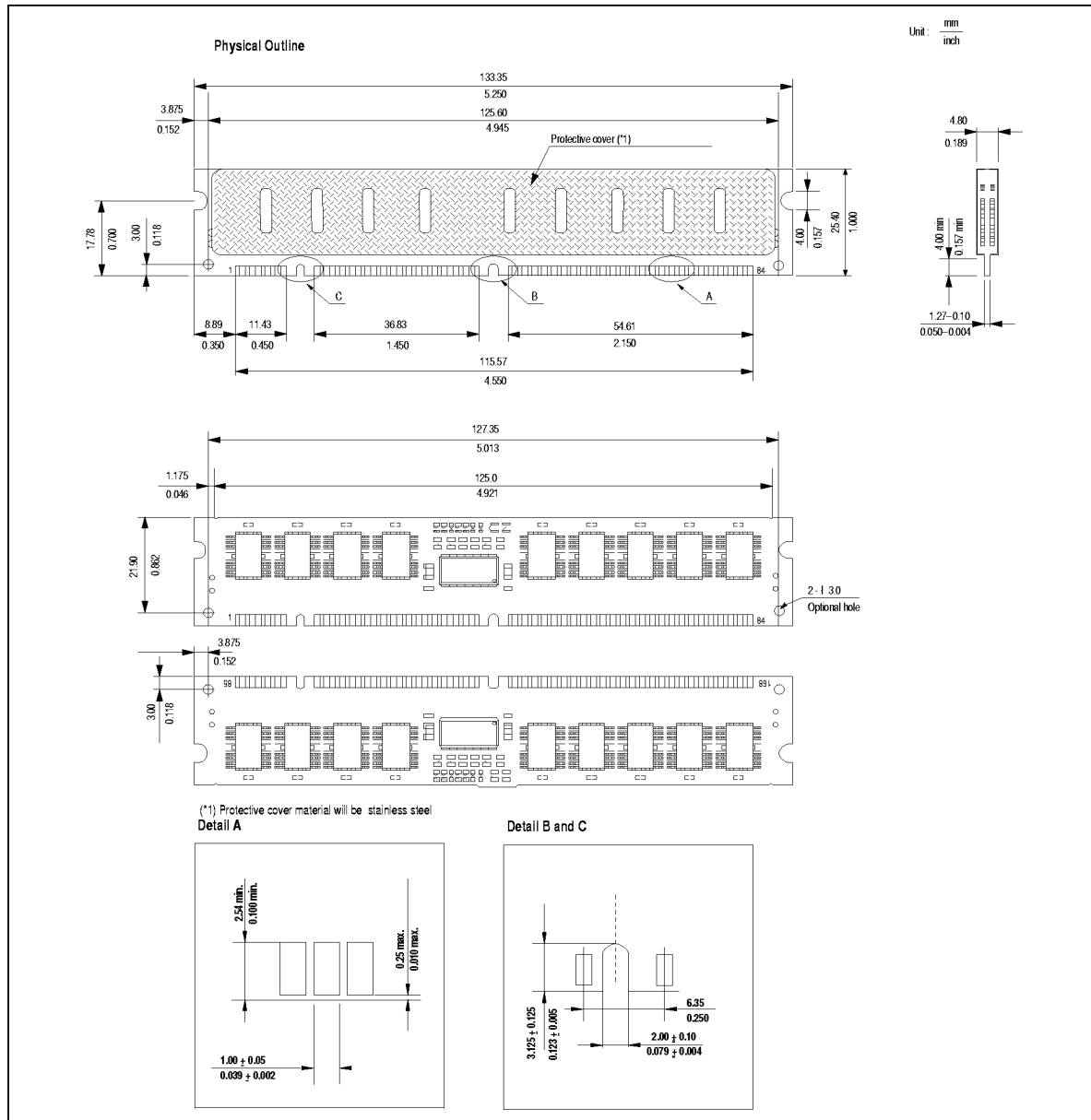
Block Diagram



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Physical Outline

Unit: mm/inch



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss.	VT	-0.5 to +4.6	V
Supply voltage relative to Vss	Vcc	-0.5 to +4.6	V
Short circuit output current	I _{out}	50	mA
Power dissipation	P _t	37	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C

Electrical Characteristics

Recommended DC Operating Condition (T_a = 0 to 70 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	Vss	0	0	0	V	
	Vcc	3.0	3.3	3.6	V	1
Input high voltage	V _{iH}	2.0	-	Vcc+0.3	V	1
Input low voltage	V _{iL}	-0.3	-	0.8	V	1

Note : 1. All voltage referenced to Vss.

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DC Characteristics (Ta=0 to 70°C , Vcc=3.3V±0.3V , Vss=0V)

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Parameter	Symbol	-6B		-7B		-8B		Unit	Test Condition	Note
		Min.	Max.	Min.	Max.	Min.	Max.			
Operating current	Icc1	-	1540	-	1360	-	1270	mA	tRC = min	1.2
Standby current	Icc2	-	82	-	82	-	82	mA	TTL interface /RAS/CAS=ViH Dout=High-Z	
		-	46	-	46	-	46	mA	CMOS interface /RAS/CAS≥VCC-0.2V Dout=High-Z	
/RAS-only refresh current	Icc3	-	1540	-	1360	-	1270	mA	tRC = min.	2
Standby current	Icc5	-	90	-	190	-	190	mA	/RAS=ViH /CAS = ViL Dout=enable	1
/CAS-before-/RAS refresh current	Icc6	-	1540	-	1360	-	1270	mA	tRC = min.	
Fast page mode current	Icc7	-	1360	-	1180	-	1000	mA	tPC = min.	1.3
Input leakage current	ILI	-10	10	-10	10	-10	10	μA	0V≤Vin≤4.6V	
output leakage current	ILO	-10	10	-10	10	-10	10	μA	0V≤Vout≤4.6V Dout=disable	
output high voltage	VoH	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	High Iout= -2mA	
output low voltage	VoL	0	0.4	0	0.4	0	0.4	V	Low Iout = 2mA	

Notes : 1. Icc depends on output load condition when the device is selected, Icc max. is specified at the output open condition.

2. Address can be changed once or less while /RAS = ViL.

3. Address can be changed once or less while /CAS = ViH.

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Capacitance (Ta=25°C, Vcc=3.3V ±0.3V)

Parameter	Symbol	Typ.	Max.	Unit	Notes
Input capacitance (Address)	C11	-	20	pF	1
Input capacitance (/CE,/WE,/OE)	C12	-	20	pF	1
Input capacitance (/RD)	C13	-	78	pF	1
Output capacitance (DQ)	CI/O	-	20	pF	1,2

Notes : 1.Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. /CAS = ViH to disable Dout.

AC Characteristics (Ta=0 to 70°C, Vcc=3.3V±0.3V, Vss=0V) *1, *2, *3, *19

Test Conditions

Input rise and fall times : 5ns

Input timing reference levels: 0.8V, 2.0V

Output timing reference levels:0.8V, 2.0V

Output load: 1 TTL gate +CL (100pF)

(Including scope and jig)

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Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

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Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Random read or write cycle time	tRC	110	-	130	-	150	-	ns	
/RAS precharge time	tRP	40	-	50	-	60	-	ns	
/CAS precharge time	tCP	10	-	10	-	10	-	ns	
/RAS pulse width	tRAS	60	10000	70	10000	80	10000	ns	
/CAS pulse width	tCAS	15	10000	18	10000	20	10000	ns	
Row address setup time	tASR	5	-	5	-	5	-	ns	
Row address hold time	tRAH	10	-	10	-	10	-	ns	
Column address setup time	tASC	0	-	0	-	0	-	ns	
Column address hold time	tCAH	10	-	15	-	15	-	ns	
/RAS to /CAS delay time	tRCD	20	40	20	47	20	55	ns	4
/RAS to column address delay time	tRAD	15	25	15	30	15	35	ns	5
/RAS hold time	tRSH	20	-	23	-	25	-	ns	
/CAS hold time	tCSH	60	-	70	-	80	-	ns	
/CAS to /RAS precharge time	tCRP	10	-	10	-	10	-	ns	
/OE to Din delay time	tOED	20	-	23	-	25	-	ns	6
/OE delay time from Din	tDZO	0	-	0	-	0	-	ns	7
/CAS delay time from Din	tDZC	0	-	0	-	0	-	ns	7
Transition time (fise and fall)	tT	3	50	3	50	3	50	ns	8
Refresh period	tREF	-	64	-	64	-	64	ms	

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Read Cycle

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Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Access time from /RAS	tRAC	-	60	-	70	-	80	ns	9,10
Access time from /CAS	tCAC	-	20	-	23	-	25	ns	10,11,18
Access time from address	tAA	-	35	-	40	-	45	ns	10,11,18
Access time from /OE	tOEA	-	20	-	23	-	25	ns	10
Read command setup time	tRCS	0	-	0	-	0	-	ns	
Read command hold time to /CAS	tRCH	0	-	0	-	0	-	ns	13
Read command hold time to /RAS	tRRH	0	-	0	-	0	-	ns	13
Column address to /RAS lead time	tRAL	35	-	40	-	45	-	ns	
Column address to /CAS lead time	tCAL	30	-	35	-	40	-	ns	
/CAS to output in Low-Z	tCLZ	2	-	2	-	2	-	ns	
Output data hold time	tOH	3	-	3	-	3	-	ns	
Output data hold time from /OE	tOHO	3	-	3	-	3	-	ns	
Output buffer turn-off time	tOFF	-	20	-	20	-	20	ns	14
Output buffer turn-off to /OE	tOEZ	-	20	-	20	-	20	ns	14
/CAS to Din delay time	tCDD	20	-	23	-	25	-	ns	6

Write Cycle

HB56RW872ES									
Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write command setup time	tWCS	0	-	0	-	0	-	ns	15
Write command hold time	tWCH	10	-	15	-	15	-	ns	
Write command pulse width	tWP	10	-	10	-	10	-	ns	
Write command to /RAS lead time	tRWL	20	-	23	-	25	-	ns	
Write command to /CAS lead time	tCWL	15	-	18	-	20	-	ns	
Data-in setup time	tDS	0	-	0	-	0	-	ns	16
Data-in hold time	tDH	15	-	20	-	20	-	ns	16

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Read-Modify-Write Cycle

HB56RW872ES									
Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read-modify-write cycle time	tRWC	155	-	181	-	205	-	ns	
/RAS to /WE delay time	tRWD	90	-	103	-	115	-	ns	15
/CAS to /WE delay time	tCWD	40	-	46	-	50	-	ns	15
Column address to /WE delay time	tAWD	55	-	63	-	70	-	ns	15
/OE hold time from /WE	tOEH	15	-	18	-	20	-	ns	

Refresh Cycle

HB56RW872ES										
Parameter		Symbol	-6B		-7B		-8B		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
/CAS setup time (CBR refresh cycle)		tCSR	10	-	10	-	10	-	ns	
/CAS hold time (CBR refresh cycle)		tCHR	10	-	10	-	10	-	ns	
/WE setup time		tWRP	5	-	5	-	5	-	ns	
/WE hold time		tWRH	10	-	10	-	10	-	ns	
/RAS precharge to /CAS hold time		tRPC	0	-	0	-	0	-	ns	

Fast Page Mode Cycle

HB56RW872ES									
Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast page mode cycle time	tPC	40	-	45	-	50	-	ns	
Fast page mode /RAS pulse width	tRASP	-	100000	-	100000	-	100000	ns	17
Access time from /CAS precharge	tCPA	-	40	-	45	-	50	ns	10.18
/RAS hold time from /CAS precharge	tCPRH	40	-	45	-	50	-	ns	

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Fast Page Mode Read-Modify-Write Cycle

HB56RW872ES									
Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast page mode read-modify-write cycle time	tPRWC	85	-	96	-	105	-	ns	
/WE delay time from /CAS precharge	tCPW	60	-	68	-	75	-	ns	15

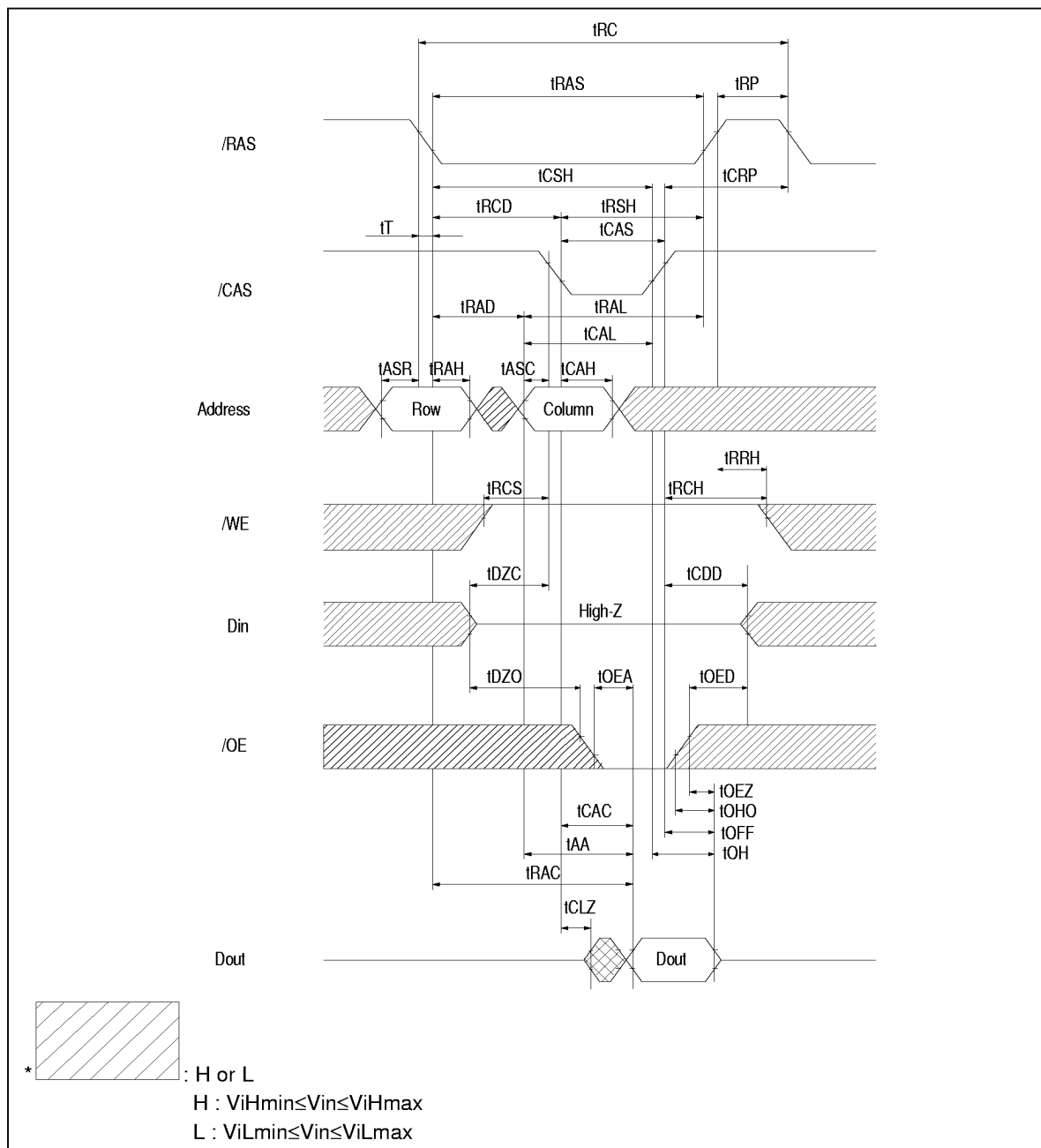
Notes

1. AC measurements assume $t_T = 5\text{ns}$.
2. An initial pause of $200\mu\text{s}$ is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing /RAS-only refresh or /CAS-before-/RAS refresh). If the internal refresh counter is used, a minimum of eight /CAS-before-/RAS refresh cycles are required.
3. Only row address is indispensable on address A10 and A11.
4. Operation with the $t_{\text{RCD}}(\text{max.})$ limit insures that $t_{\text{RAC}}(\text{max.})$ can be met, $t_{\text{RCD}}(\text{max.})$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max.})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Operation with the $t_{\text{RAD}}(\text{max.})$ limit insures that $t_{\text{RAC}}(\text{max.})$ can be met, $t_{\text{RAD}}(\text{max.})$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max.})$ limit, then access time is controlled exclusively by t_{AA} .
6. Either t_{OED} or t_{CDD} must be satisfied.
7. Either t_{DZO} or t_{DZC} must be satisfied.
8. $V_{\text{IH}}(\text{min.})$ and $V_{\text{IL}}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{\text{IH}}(\text{min.})$ and $V_{\text{IL}}(\text{max.})$.
9. Assumes that $t_{\text{RCD}} < t_{\text{RCD}}(\text{max.})$ and $t_{\text{RAD}} < t_{\text{RAD}}(\text{max.})$. if t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
10. Measured with a load circuit equivalent to 1TTL loads and 100pF .
11. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max.})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max.})$.
12. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max.})$ and $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max.})$.
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
14. $t_{\text{OFF}}(\text{max.})$ and $t_{\text{OEZ}}(\text{max.})$ is define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
15. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min.})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min.})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min.})$, $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min.})$, and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min.})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell: if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
16. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in delayed write or read-modify-write cycle.
17. t_{RASP} defines /RAS pulse width in fast page mode cycles.
18. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA} .
19. In delayed write or read-modify-write cycles, /OE must disable output buffer prior to applying data to the device. After /RAS is reset, if $t_{\text{OEH}} \geq t_{\text{CWL}}$, the I/O pins will remain open circuit (high impedance); if $t_{\text{OEH}} \leq t_{\text{CWL}}$, invalid data will be out ay each I/O.

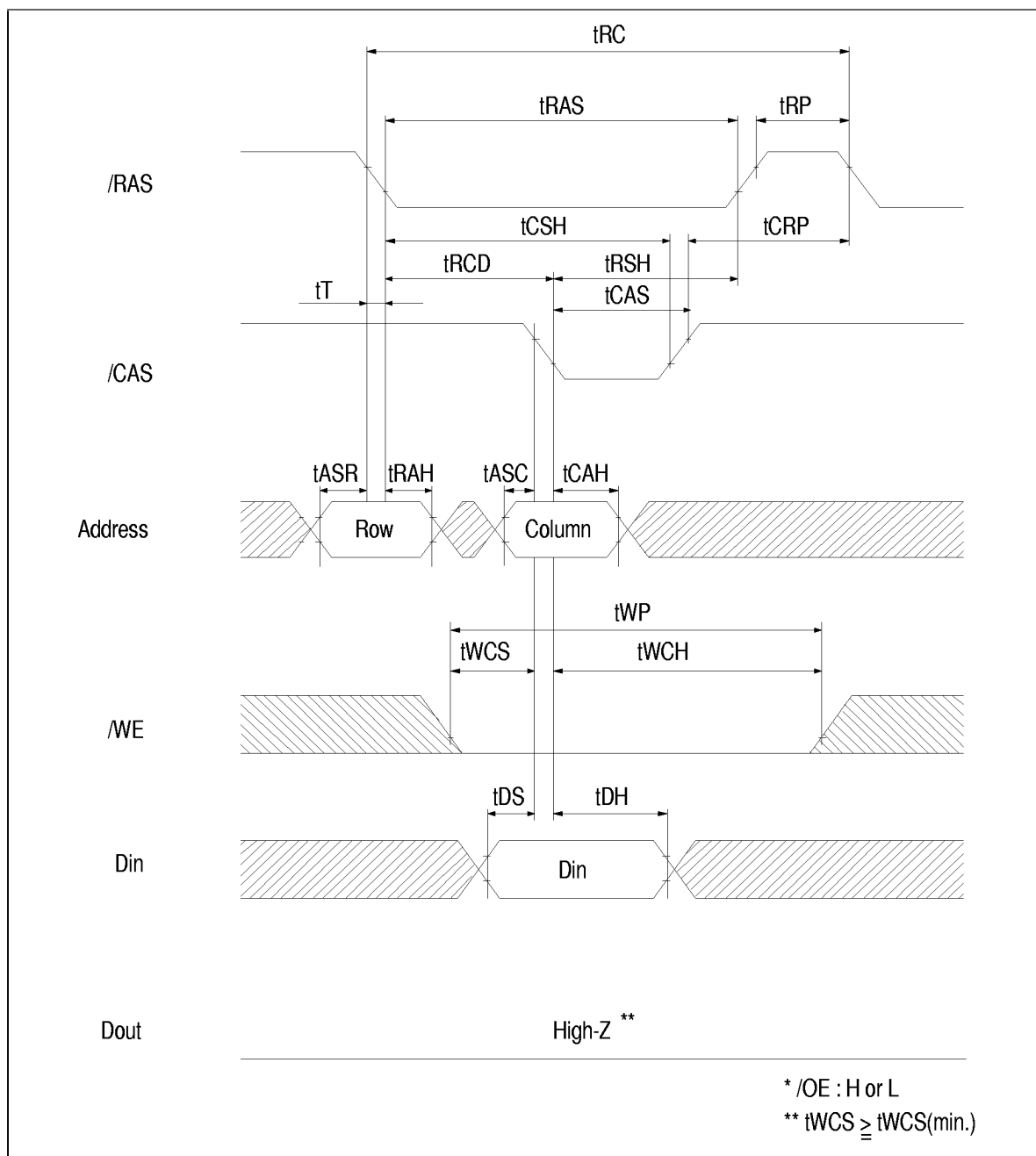
HB 56RW873ES Series

Timing Waveform *

Read Cycle



Early Write Cycle

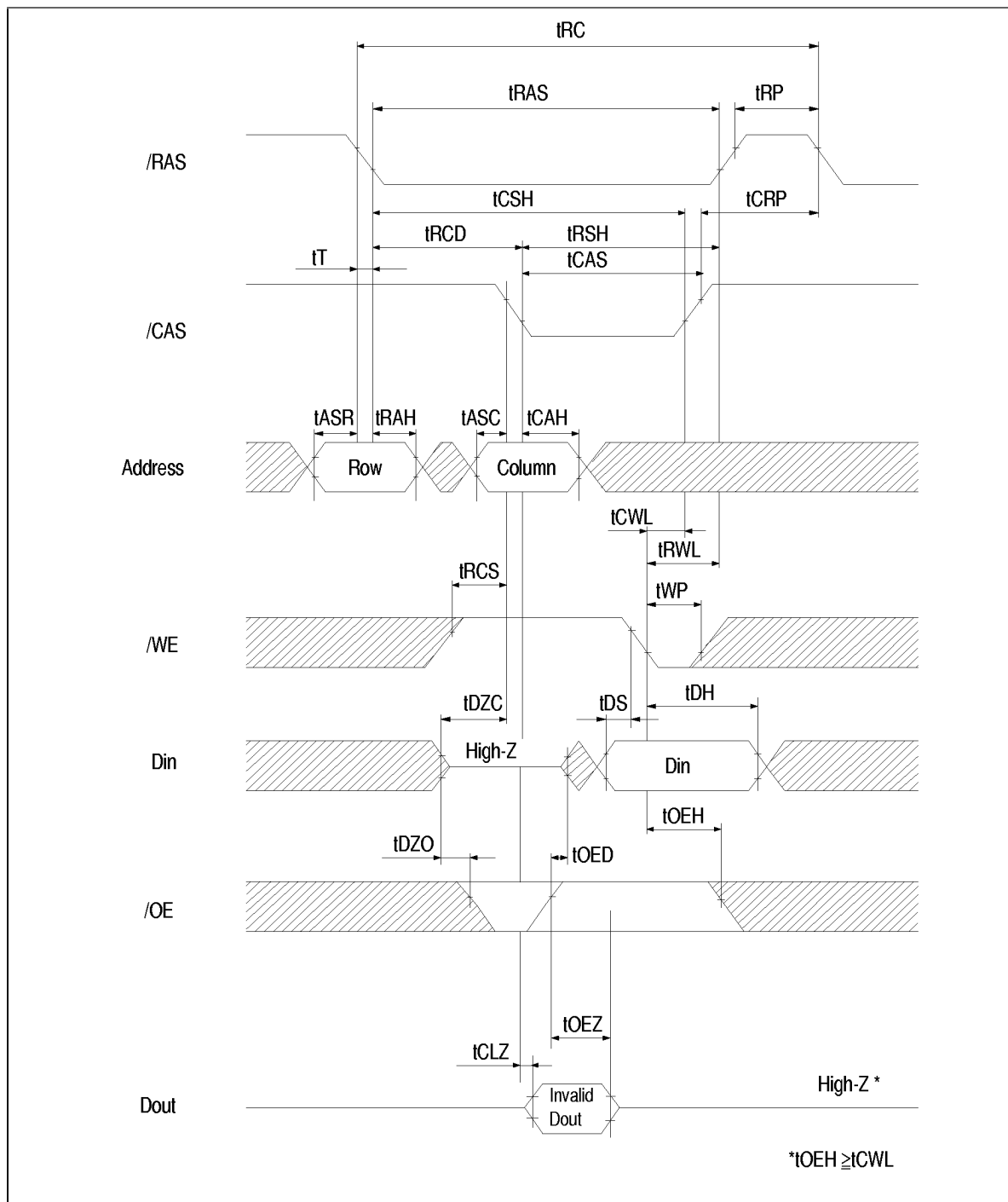


* /OE : H or L

** : $t_{WCS} \geq t_{WCS}(\text{min.})$

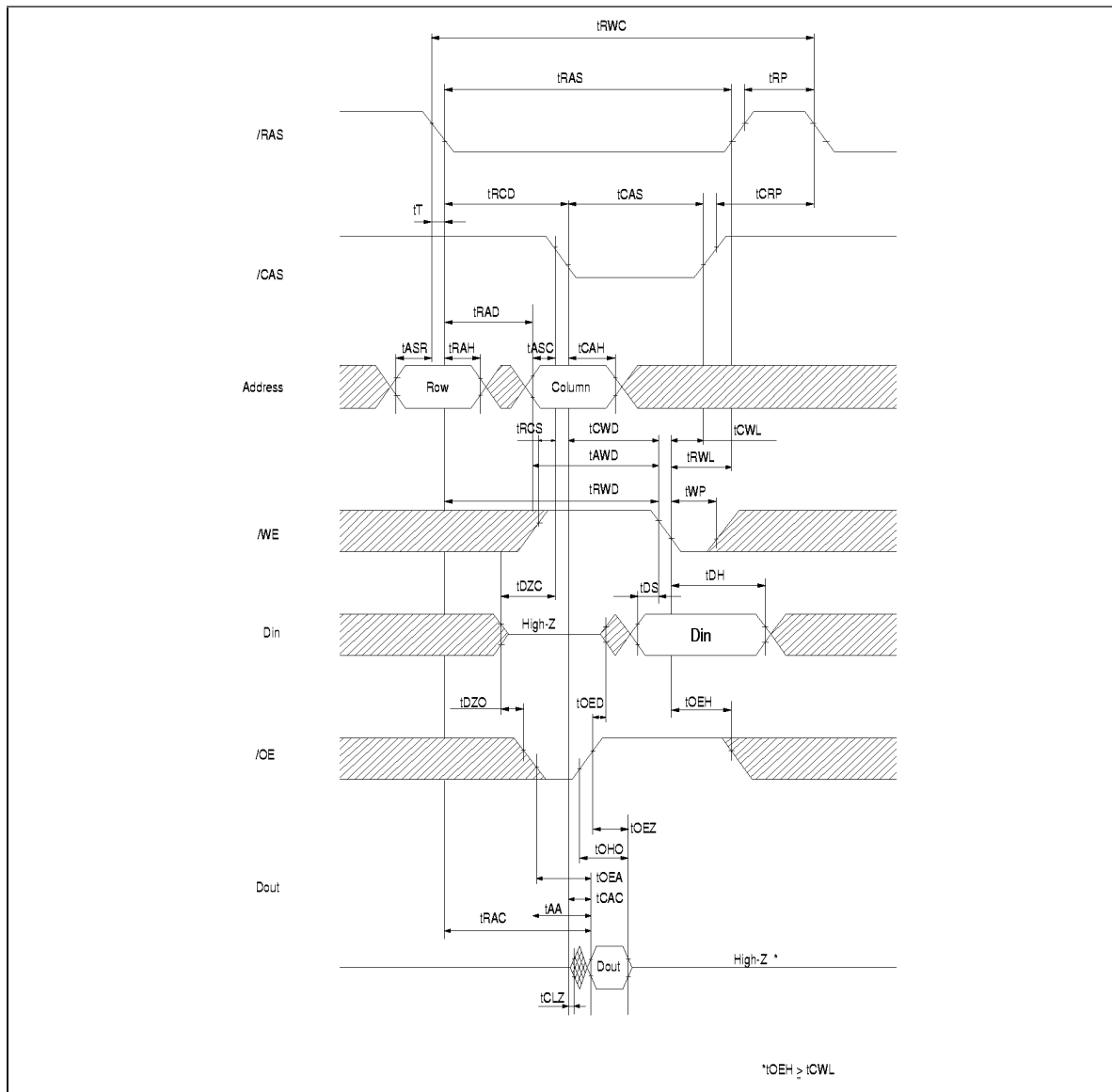
HB 56RW873ES Series

Delayed Write Cycle *19



* : $t_{\text{OEH}} \geq t_{\text{CWL}}$

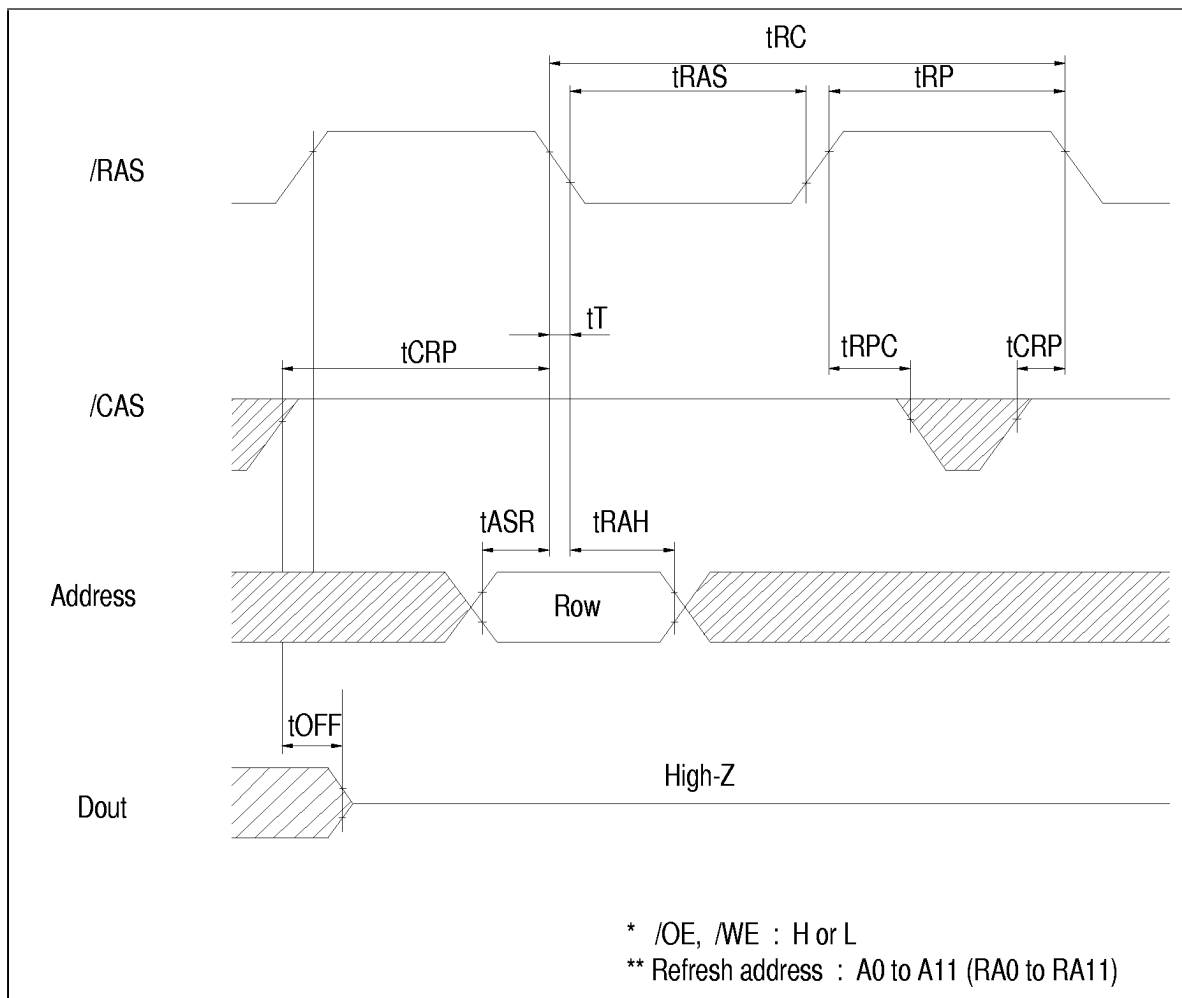
Read - Modify - Write Cycle *19



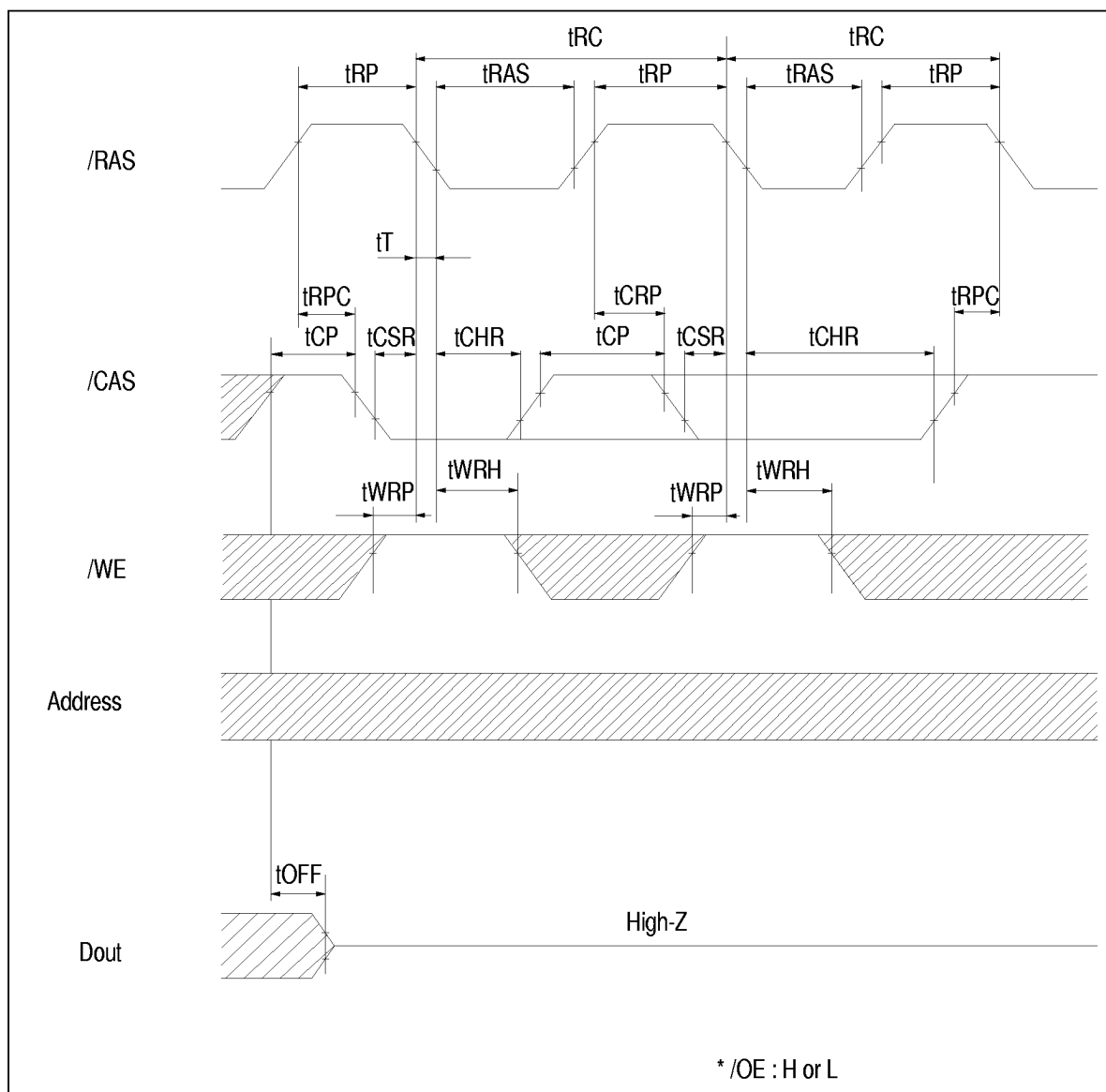
* : $t_{OEZ} \geq t_{CWL}$

HB 56RW873ES Series

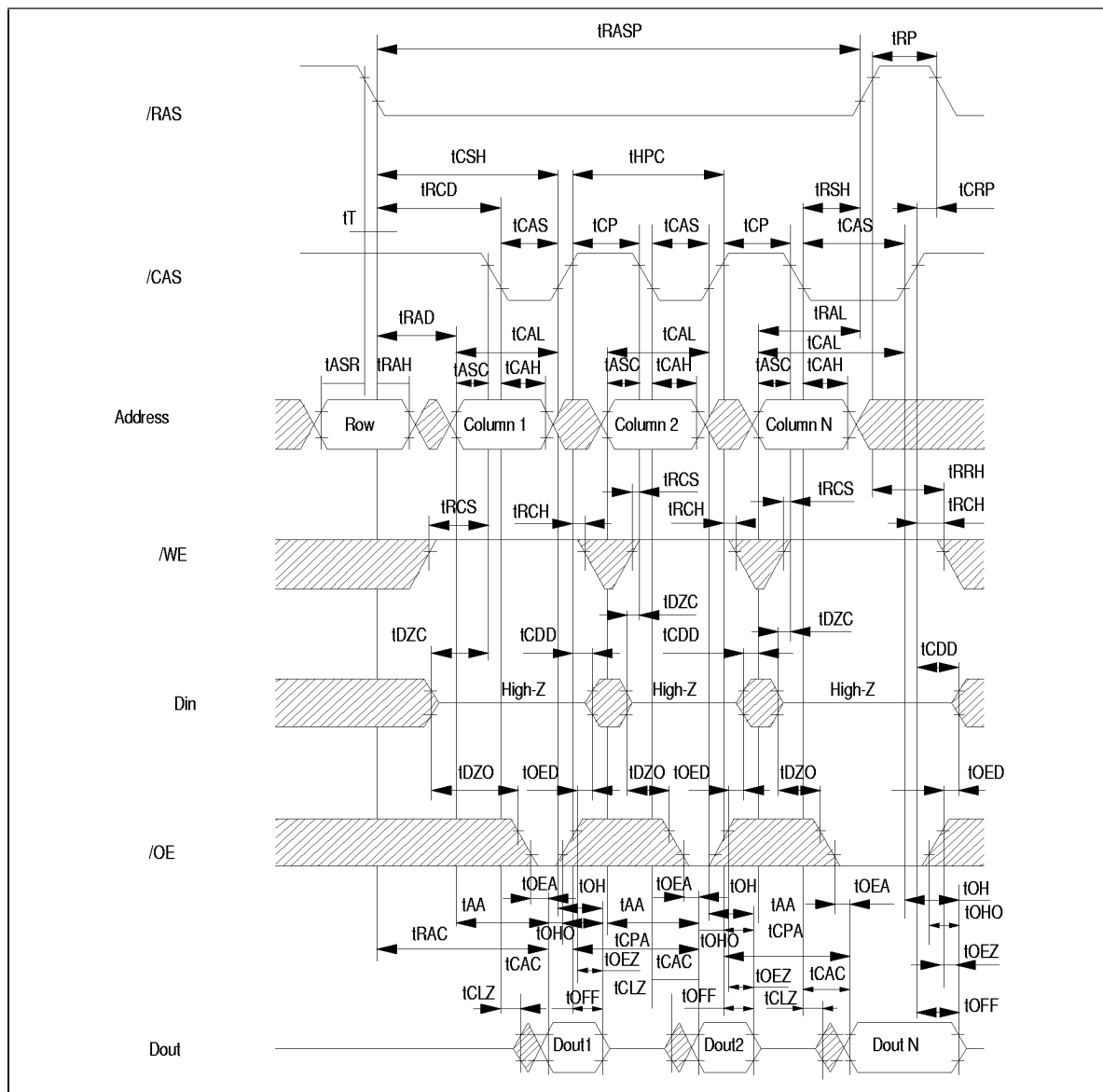
/RAS - Only Refresh Cycle



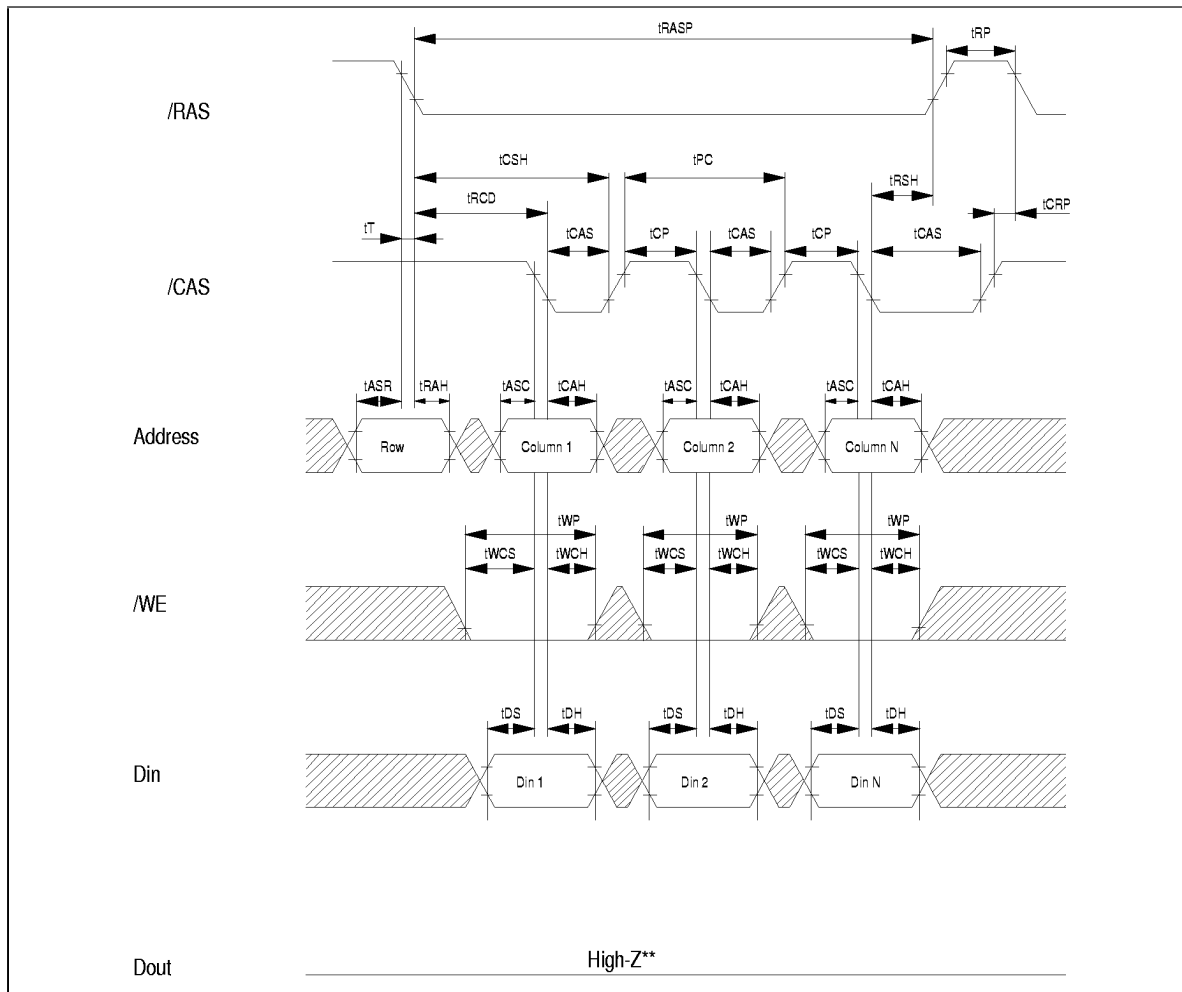
/CAS - Before - /RAS Refresh Cycle



Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle



* /OE : H or L

** : $t_{WCS} \geq t_{WCS}(\text{min.})$

Fast Page Mode Delayed Writed Cycle *19



