64Kx32 Static RAM CMOS, High Speed Module

FEATURES

- 64Kx32 bit CMOS Static
- Random Access Memory
  - Access Times 12 through 25ns
  - Individual Byte Selects
  - Output Enable Function
  - Fully Static, No Clocks
  - TTL Compatible I/O
- High Density Packaging
  - 64 Pin SIMM, No. 30-Straight
  - 64 Pin SIMM, No. 342 Angled
  - 64 Pin ZIP, No. 87
  - JEDEC Standard Pinout
  - Common Data Inputs and Outputs
- Single +5V (±10%) Supply Operation

DESCRIPTION

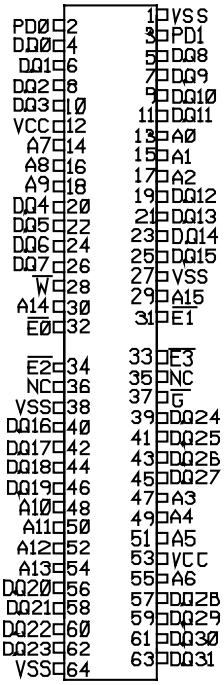
The EDI8F3265C is a high speed 2 megabit Static RAM module organized as 64Kx32. This module is constructed from eight 64Kx4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip Enables ($\overline{E0}$-$\overline{E3}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8F3265C is offered in a both 64 lead SIMM and 64 pin ZIP packages, which enable two megabits of memory to be placed in less than 1.2 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

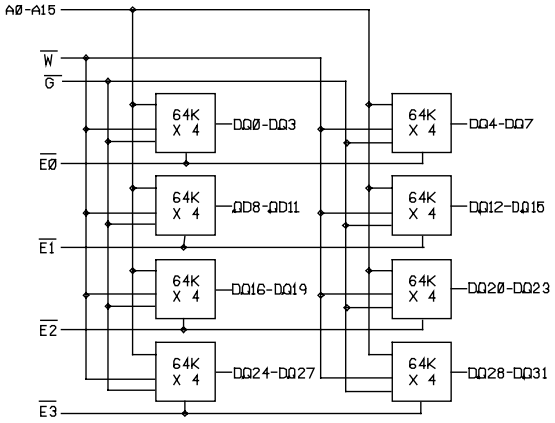
PIN CONFIGURATIONS AND BLOCK DIAGRAM



PD0 = OPEN
PD1 = VSS

PIN NAMES

A0-A15	Address Inputs
$\overline{E0}$-$\overline{E3}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ3	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	
Plastic	-55°C to +125°C
Power Dissipation	8.0 Watt
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL =30pFl

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	ns	Min	Typ*	Max	Units
Operating Power	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA,	12-15ns	–	880	1120	mA
Supply Current		Min Cycle	20-25ns		740	980	mA
Standby (TTL) Power	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL		–	150	280	mA
Supply Current		VIN $\geq$ VIH					
Full Standby Power	ICC3	$\overline{E} \geq$ VCC-0.2V		--	80	160	mA
Supply Current		VIN $\geq$ VCC-0.2V or					
CMOS		VIN $\leq$ 0.2V					
Input Leakage Current	ILI	VIN = 0V to VCC		–	–	±20	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		–	–	±80	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4	–	–	V
Output Low Voltage	VOL	IOL = 8.0mA		–	–	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

TRUTH TABLE

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

CAPACITANCE

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	60	pF
Capacitance (DQ Pins)	CD/Q	20	pF
Input ($\overline{E}$)	CC	20	pF
Input ($\overline{W}$) Line (G)	CW	60	pF

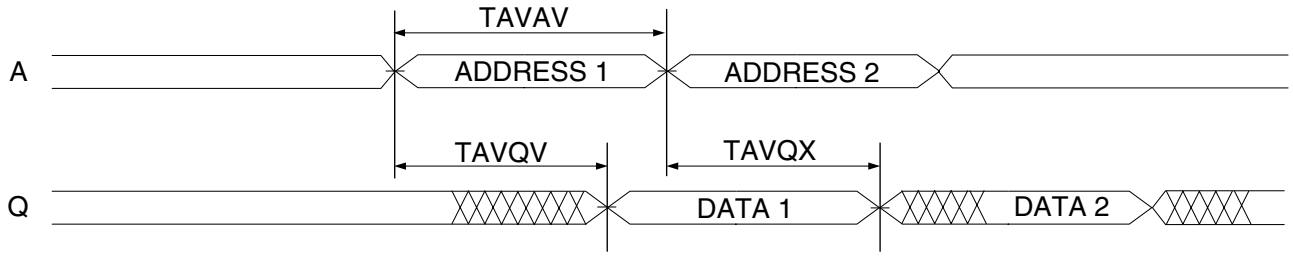
These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

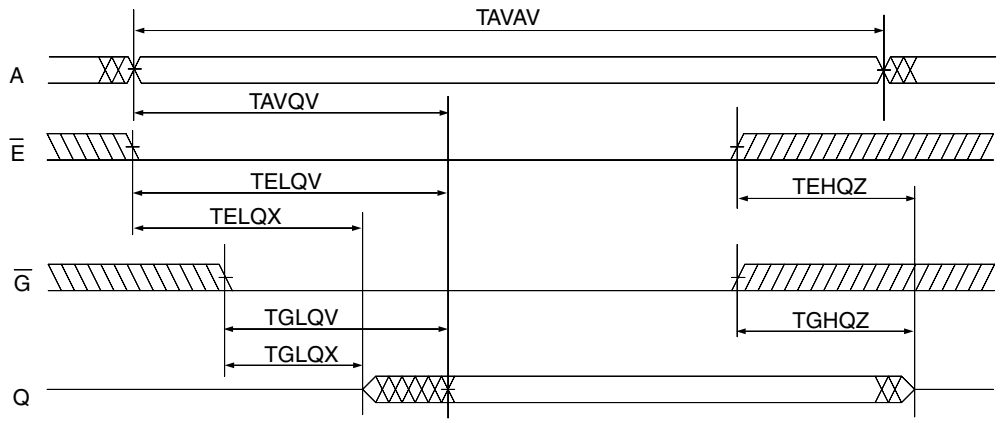
	Symbol		12ns		15ns		20ns		25ns		
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	TAVAV	TRC	12		15		20		25		ns
Address Access Time	TAVQV	TAA		12		15		20		25	ns
Chip Enable Access Time	TELQV	TACS		12		15		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ	0	8	0	8	0	10	0	12	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		8		8		10		15	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	6	0	6	0	8	0	10	ns

Note 1: Parameter guaranteed, but not tested.

READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW



READ CYCLE 2 - $\overline{W}$ HIGH

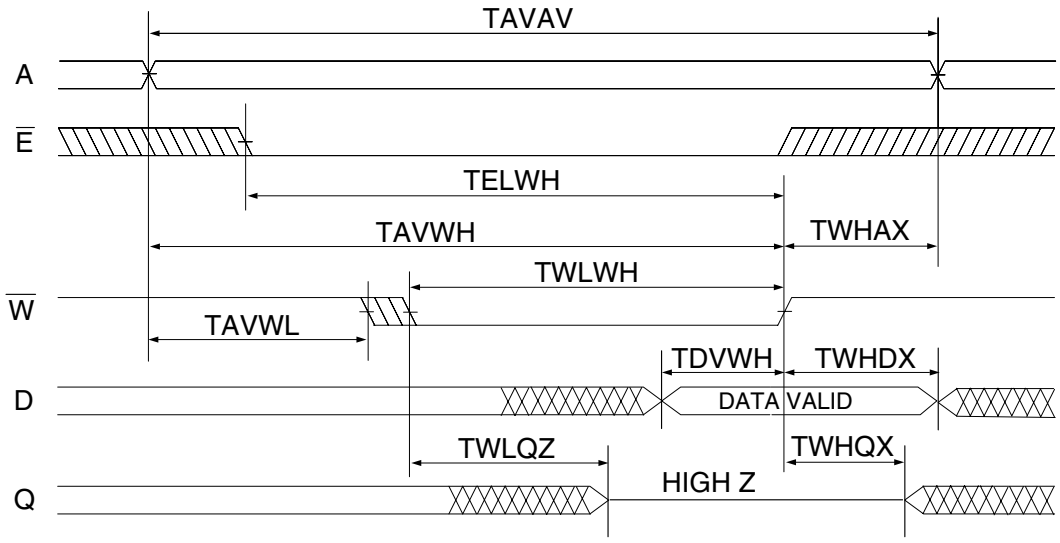


AC CHARACTERISTICS WRITE CYCLE

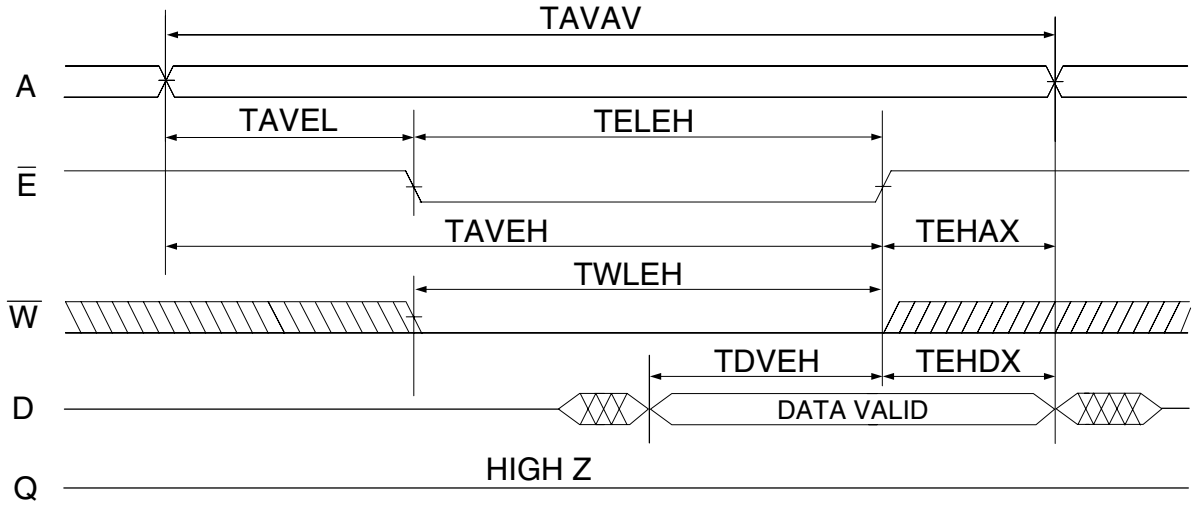
Parameter	Symbol JEDEC	Symbol Alt.	12ns Min	12ns Max	15ns Min	15ns Max	20ns Min	20ns Max	25ns Min	25ns Max	Units
Write Cycle Time	TAVAV	TWC	12		15		20		25		ns
Chip Enable to End of Write	TELWH	TCW	10		10		15		20		ns
	TELEH	TCW	10		10		15		20		ns
Address Setup Time	TAVWL	TAS	0		0		2		2		ns
	TAVEL	TAS	0		0		2		2		ns
Address Valid to End of Write	TAVWH	TAW	12		13		15		20		ns
	TAVEH	TAW	12		13		15		20		ns
Write Pulse Width	TWLWH	TWP	12		13		15		20		ns
	TWLEH	TWP	12		13		15		20		ns
Write Recovery Time	TWHAX	TWR	2		2		2		2		ns
	TEHAX	TWR	2		2		2		2		ns
Data Hold Time	TWHDX	TDH	1		3		1		1		ns
	TEHDX	TDH	1		3		1		1		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	8	0	8	0	10	0	12	ns
Data to Write Time	TDVWH	TDW	10		10		12		15		ns
	TDVEH	TDW	10		10		12		15		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

WRITE CYCLE 1 - $\overline{W}$ CONTROLLED



WRITE CYCLE 2 - $\overline{E}$ CONTROLLED



ORDERING INFORMATION

Part Number	Speed (ns)	Package No.
EDI8F3265C12MZC	12	87
EDI8F3265C15MZC	15	87
EDI8F3265C20MZC	20	87
EDI8F3265C25MZC	25	87

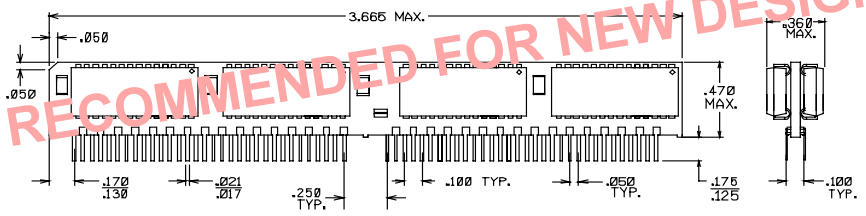
Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I, eg. EDI8F3265C20MZC becomes EDI8F3265C20MZI.

Part Number	Speed (ns)	Package No.
EDI8F3265C12MMC	12	30
EDI8F3265C15MMC	15	30
EDI8F3265C20MMC	20	30
EDI8F3265C25MMC	25	30
EDI8F3265C12MNC	12	342
EDI8F3265C15MNC	15	342
EDI8F3265C20MNC	20	342
EDI8F3265C25MNC	25	342

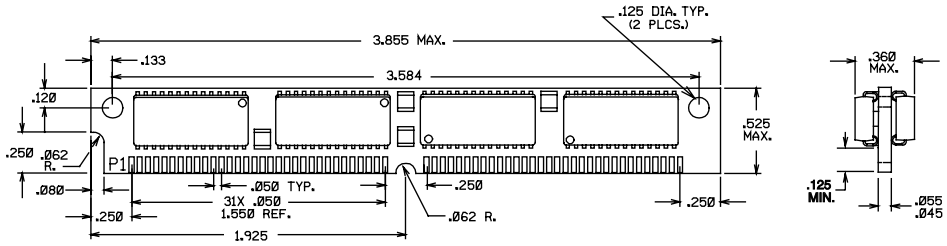
PACKAGE DESCRIPTION

PACKAGE NO. 87: 64 PIN ZIP

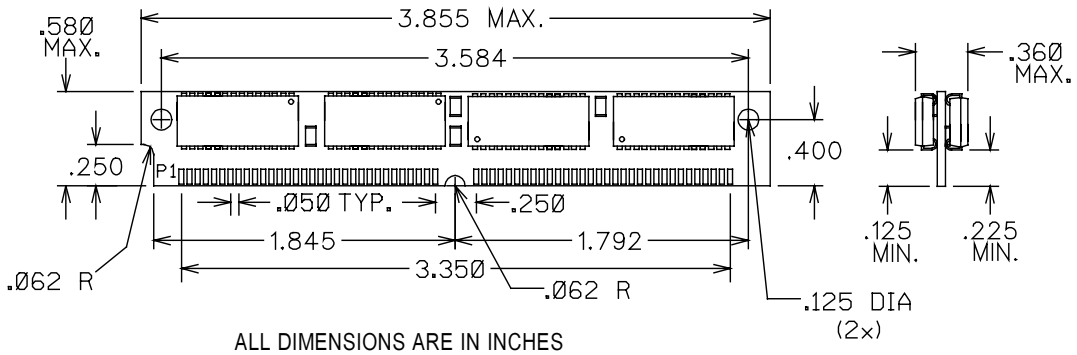
NOT RECOMMENDED FOR NEW DESIGNS



PACKAGE NO. 30: 64 PIN SIMM STRAIGHT



PACKAGE NO. 342: 64 PIN SIMM ANGLED



ALL DIMENSIONS ARE IN INCHES

DATASHEET APPROVALS

ECO# 15655

EDI PART NO. EDI8F3265C NEW REV 9A DATE 10/7/02

APPROVAL:	INITIAL	DATE	CORRECTION ON PAGES
~~JUAN GUZMAN~~ L.K.			
~~MUKESH TRIVEDI~~ M.A.			
PAUL MARIEN			
LARRY WINROTH			
DAVE KELLY			
MARK DOWNEY			
DAVE HARRISON			
TONY LEE			
BOB KHEDERIAN			
LUIS ESTELLA			

	YES	NO
WILL THIS DATASHEET GO ON THE WEB?		
IS THIS A NEW DATASHEET?		
WILL THIS DATASHEET REPLACE AN EXISTING DATASHEET THAT'S ALREADY ON THE WEB?		

LINE:_____
FAMILY:_____
PROD.TYPE:_____
ORG:_____
DENSITY:_____
SPEED:_____
PKG:_____
VOLTAGE:_____

IF YES, WHAT DATASHEET IS IT REPLACING? _____

WHAT SECTION SHOULD THIS DATASHEET BE PLACED IN ON THE WEB? _____

AFTER REVIEWING OR MAKING CORRECTIONS ON THE DATASHEET (S)
PLEASE SIGN-OFF ON THIS SHEET AND ,MAKE YOUR CORRECTIONS –ON **THE ORIGINAL COPY(S).**

AFTER REVIEWING THE DATA SHEET, TEST ENGINEERING WILL COMPLETE THE SECTION BELOW.

TEST PROGRAM CHANGE REQUIRED:
YES:_____NO_____DATE:_____

TEST ENGINEER SIGNATURE_____

IF YES, DO NOT RELEASE DATA SHEET UNTIL TEST PROGRAM CHANGE IS COMPLETED.
TEST PROGRAM CHANGE COMPLETION DATE:_____
TEST PROGRAM NAME AND REVISION_____
TEST ENGINEER SIGNATURE_____