C9811x2

Low EMI Clock Generator for Intel® 810 Chipset Systems

Product Features

- Intel's 810 clock solution
- 3 copies of CPU Clock (CPU[0:1] and CPU_ITP)
- 9 copies of SDRAM Clock (SDRAM[0:7] and DCLK)
- 8 copies of PCI clock
- 2 copies of 3V66 Clock
- 2 copies of APIC Clock, synchronous to PCI Clock
- 1 REF Clock
- 2 USB Clocks (Non SSC)
- Power Down Feature
- Spread Spectrum Support
- SMBUS Support for turning off unused clocks
- 56 Pin SSOP Package

Frequency Table (MHz)

SEL1	SEL0	CPU	SDRAM	PCI
0	0	Tri-state	Tri-state	Tri-state
0	1	Test mode (see table2)		
1	0	66.6	100	33.3
1	1	100	100	33.3

Table 1

Note: The following clocks remain fixed frequencies except in Test Mode.
3V66=66.6MHz, USB/DOT=48MHz, REF=14.318MHz and IOAPIC=16.6 or 33.3MHz depending on power up selection.

Block Diagram

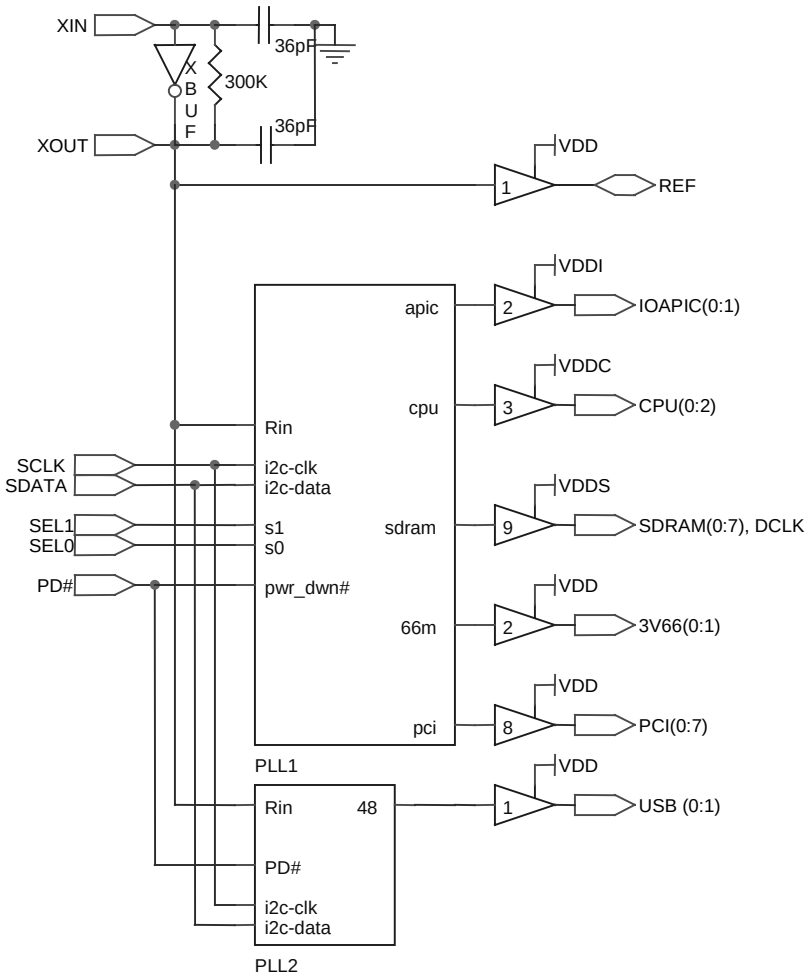
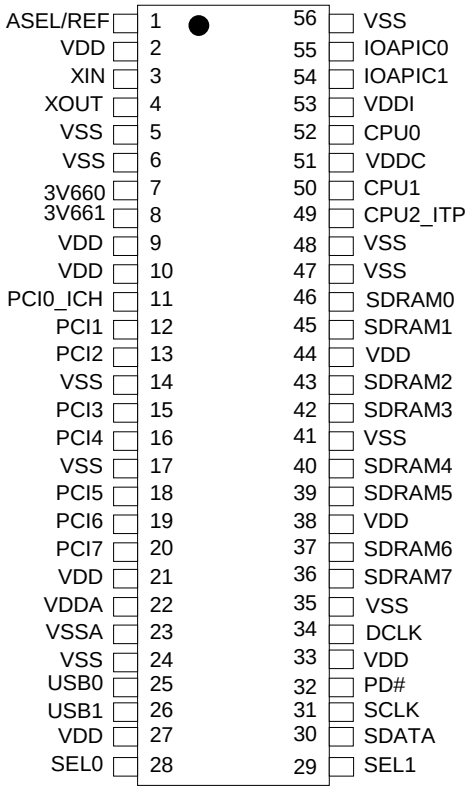


Fig.1

Pin Configuration

C9811X2



Pin Description

PIN No.	Pin Name	PWR	I/O	TYPE	Description
1	**ASEL/REF**	VDD	I/O		3.3V 14.318 MHz clock output. This pin also serves as the select strap for IOAPIC clock frequency. If strapped low during power up, IOAPIC clocks run at PCI/2 (16.6 MHz). If not strapped, it runs at 33 MHz. This pin has a 50K internal pull-up (+/- 20K).
3	**XIN**	VDD	I	OSC1	14.318MHz Crystal input
4	**XOUT**	VDD	O		14.318MHz Crystal output
11, 12, 13, 15, 16, 18, 19, 20	**PCI0/ICH PCI(1..7)**	VDD	O		3.3V PCI clock outputs
7, 8	**3V66(0,1)**	VDD	O		3.3V Fixed 66.6 MHz clock outputs
25, 26	**USB (0:1)**	VDD	O		3.3V Fixed 48 MHz clock outputs
28, 29	**SEL(0,1)**	VDD	I		3.3V LVTTL compatible inputs for logic selection. Has an internal pull-up (Typ. 250KΩ)
30	**SDATA**	VDD	I		I²C compatible SDATA input. Has an internal pull-up (>100KΩ)
31	**SCLK**	VDD	I		I²C compatible SCLK input. Has an internal pull-up (>100KΩ)
32	**PD#**	VDD	I		3.3V LVTTL compatible input. Device enters powerdown mode When held LOW. Has an internal pull-up (>100KΩ)
34	**DCLK**	VDD	O		3.3V output running 100MHz
36, 37, 39, 40, 42, 43, 45, 46	**SDRAM(7..0)**	VDDS	O		3.3V output running 100MHz. All SDRAM outputs can be turned off through SMBUS.
49, 50, 52	**CPU(2)_ITP, CPU(1,0)**	VDDC	O		2.5V Host bus clock outputs. 66 or 100MHz depending on state of SEL0 and SEL1 pins.
54, 55	**IOAPIC(1,0)**	VDDI	O		2.5V clock outputs running rising edge synchronous with the PCI clock frequency. 16.67 MHz or 33.3 MHz dependent on power up strapping of REF (Pin 1).
2, 9, 10, 21, 27	**VDD**	-			3.3V Power Supply
22	**VDDA**	-	P		Analog circuitry 3.3V Power Supply
23	**VSSA**	-	P		Analog circuitry power supply Ground pins.
51, 53	**VDDC, VDDI**	-	P		2.5V Power Supply's
5, 6,14, 17, 24, 35, 41, 47, 48, 56	**VSS**	-	P	-	Common Ground pins.
33, 38, 44	**VDDS**	-	P	-	3.3V power support for SDRAM clock output drivers.

A bypass capacitor (0.1μF) should be placed as close as possible to each positive power pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Test Mode Function

Test Mode Functionality

SEL1	SEL0	CPU	SDRAM	3V66	PCI	48 MHz	REF	IOAPIC
0	1	TCLK÷2	TCLK÷2	TCLK÷3	TCLK÷6	TCLK÷2	TCLK	TCLK÷6

Table 2

Note: TCLK is a test clock over driven on the XIN input during test mode.

Power Management Functions

Power Management on this device is controlled by a single pin, PD# (pin32). When PD# is high (default) the device is in running and all signals are active.

When PD# is asserted (forced) low, the device is in shutdown (or in power down) mode and all power supplies (3.3V and 2.5V except for VDDA/pin 22) may be removed. When in power down, all outputs are synchronously stopped in a low state (see Fig.2 below), all PLL's are shut off, and the crystal oscillator is disabled. When the device is shutdown the I²C function is also disabled.

Power Management Timing

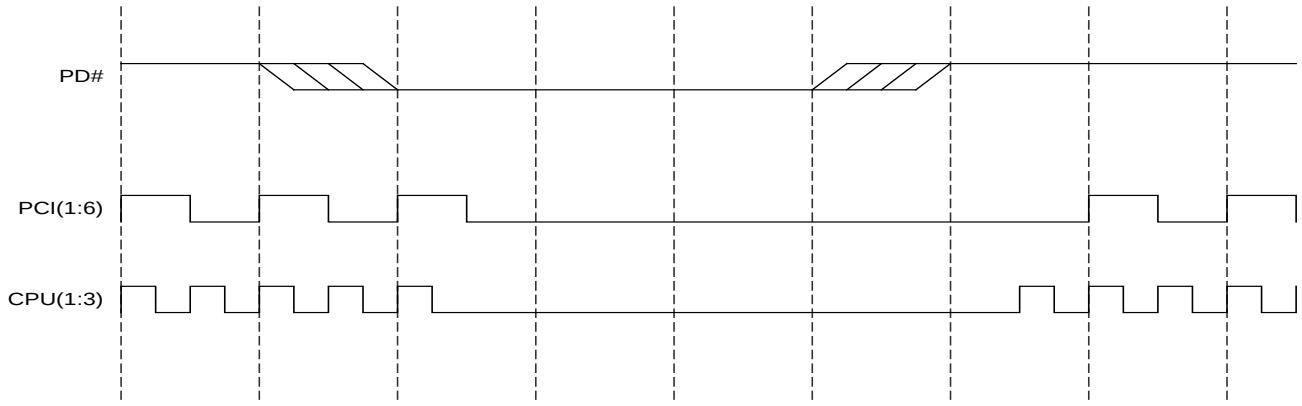


Fig.2

Power Management Current

PD#, **SEL[1..0]** (CPU Clock)	Maximum 2.5 Volt Current Consumption (VDD2.5 =2.625)	Maximum 3.3 Volt Current Consumption (VDD3.3 = 3.465 V)
0XX (Power down)	100 µA	200 µA
110 (66MHz)	70 mA	280 mA
111 (100MHz)	100 mA	280 mA

Table 3

When exiting the power down mode, the designer must supply power to the VDD pins first, a minimum of 200mS before releasing the PD# pin high.

Clock Synchronization and Phase Alignment

This device incorporates IOAPIC clock synchronization. With this feature, the IOAPIC clocks are derived from the CPU clock. The IOAPIC clock lags the CPU clock by the specified 1.5 to 3.5 nSec. Figure 3 shows the relationship between the CPU and IOAPIC clocks.

Device Clock Phase Relationships

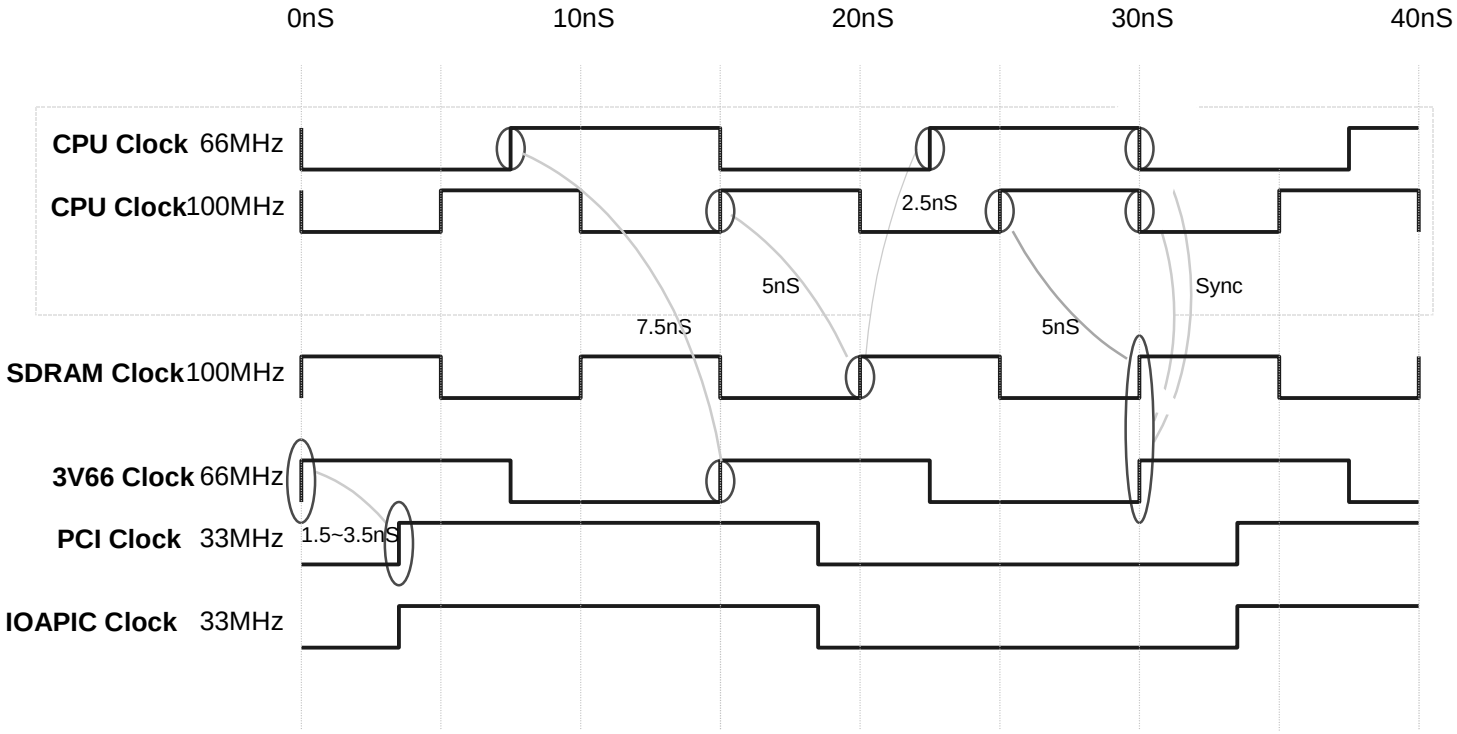


Fig.3

Power on Bi-Directional Pins

Power Up Condition:

Pin1 is a Power up bi-directional pin and is used for selecting the IOAPIC frequency in page 1, table 1. During power-up of the device, this pin is in input mode (see Fig 4, below), therefore; it is considered input select pins internal to the IC. After a settling time, the selection data is latch into the internal control register and this pin becomes a clock output. If strapped low the IOAPIC clock is set to ½ of the PCI frequency (16.6 MHz). If strapped high IOAPIC is 33.3 MHz.

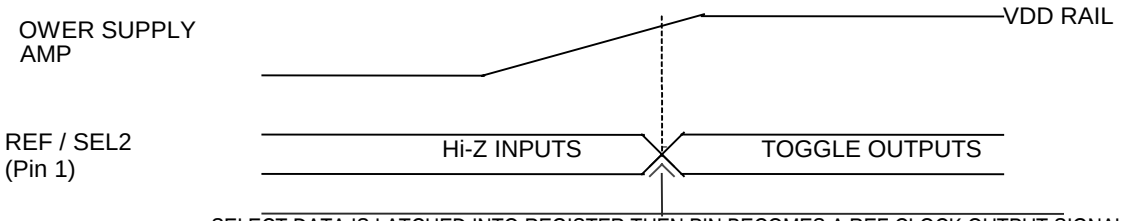


Fig.4

Strapping Resistor Options:

The power up bi-directional pins have a large value pull-up each (250KΩ), therefore, a selection "1" is the default. If the system uses a slow power supply (over 5mS settling time), then **it is recommended** to use an external Pull-up (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see Fig.5A and B.

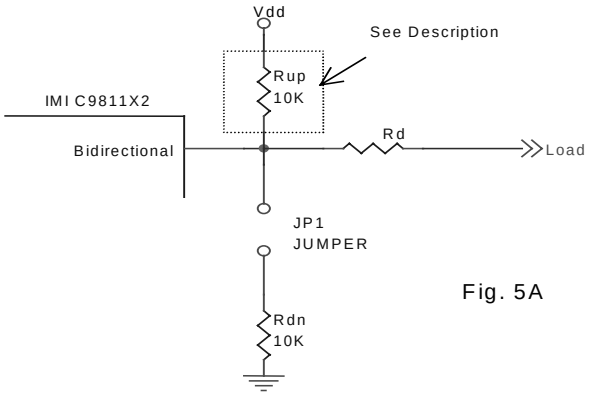


Fig. 5A

Fig. 5A represents an additional pull up resistor 50KΩ connected from the pin to the power line, which allows a faster pull to a high level.
If a selection "0" is desired, then a jumper is placed on JP1 to a 5KΩ resistor as implemented as shown in Fig.5A. Please note the selection resistors (Rup and Rdn) are placed before the Damping resistor (Rd) close to the pin.

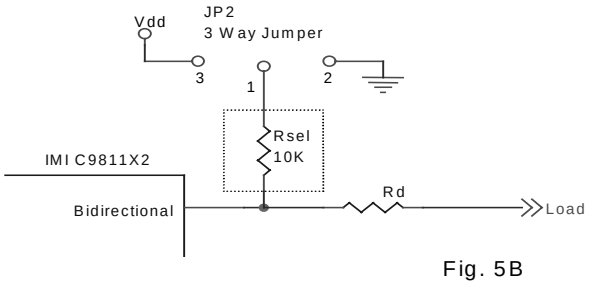


Fig. 5B

Fig. 5B represent a single resistor 10KΩ connected to a 3-way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

2-Wire SMBUS Control Interface

The 2-wire control interface implements a write slave only interface according to SMBus specification. (See Fig. 7 / P. 8). Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is an 8-bit address. W#=0 in write mode.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. Data is transferred MSB first at a max rate of 100kbits/S. The device will not respond to any other control interface conditions, and previously set control registers are retained.

SMBUS Test Circuitry

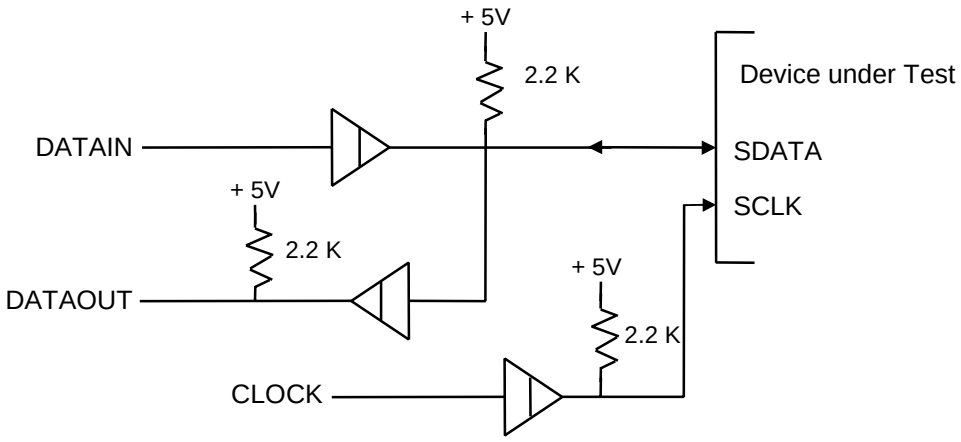


Fig.6

Note: Buffer is 7407 with VCC @ 5.0 V

Serial Control Registers

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte, two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.

Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the sequence described below (Byte 0, Byte 1, and Byte2) will be valid and acknowledged.

Byte 0: CPU Clock Register (1=Enable, 0=Disable, Default=07)

Bit	@Pup	Pin#	Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Spread spectrum mode
2	1	26	USB1
1	1	25	USB0
0	1	49	CPU2_ITP

Byte 1: SDRAM Clock Register (1=Enable, 0=Disable, Default=FF)

Bit	@Pup	Pin#	Description
7	1	36	SDRAM7
6	1	37	SDRAM6
5	1	39	SDRAM5
4	1	40	SDRAM4
3	1	42	SDRAM3
2	1	43	SDRAM2
1	1	45	SDRAM1
0	1	46	SDRAM0

Byte 2: PCI Clock Register (1=Enable, 0=Disable, Default=FE)

Bit	@Pup	Pin#	Description
7	1	20	PCI7
6	1	19	PCI6
5	1	18	PCI5
4	1	16	PCI4
3	1	15	PCI3
2	1	13	PCI2
1	1	12	PCI1
0	0	-	Reserved

Byte 3: Reserved Register (Default=00)

Byte 4: Reserved Register (Default=00)

Byte 5: SSCG Control Register (Default=00)

Bit	@Pup	Pin#	Description
7	0	-	Spread Mode (0=down, 1=center)
6	0	-	Ref. Table 4
5	0	-	Ref. Table 4
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

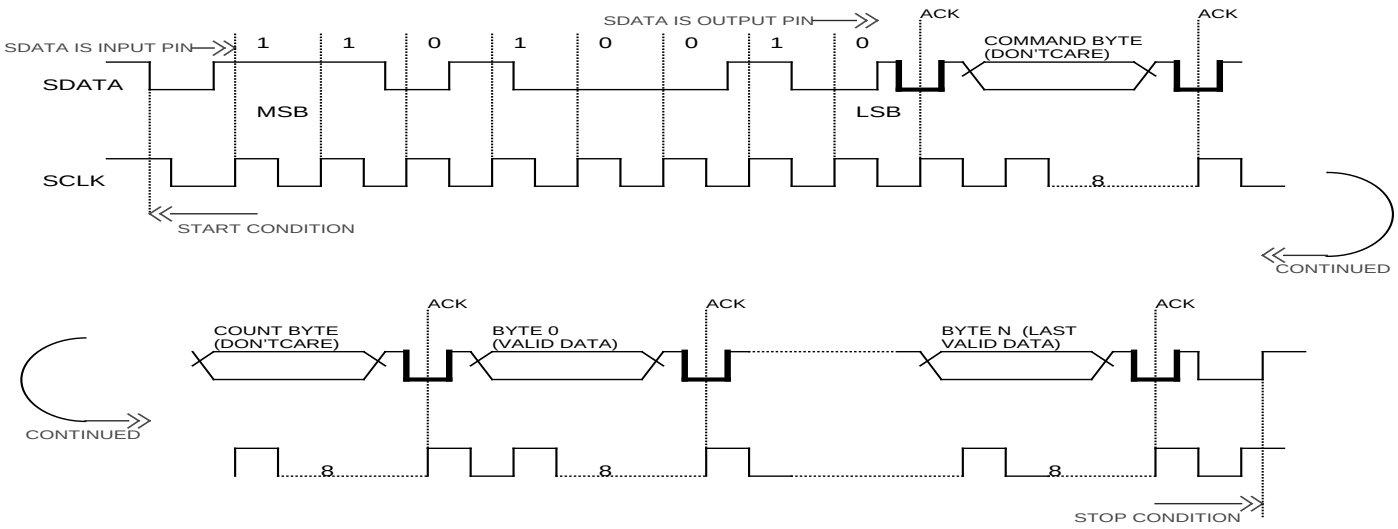


Figure 7
SMBUS Communications Waveforms

Test and Measurement Condition

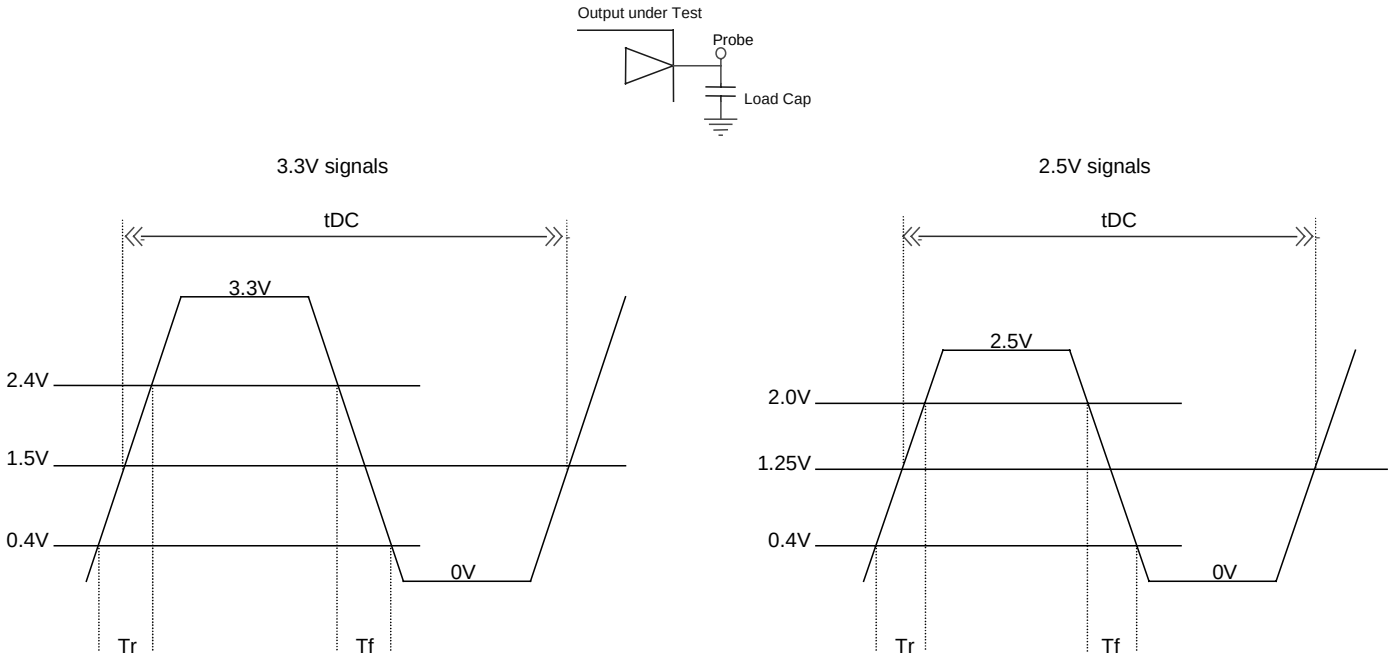


Fig.8

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore spreading the same amount of energy over a spectrum. This technique is achieved by modulating the clock down from (Fig.9A) or around the center (Fig.9B) of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting SMBUS byte0, bit3 = 1. The default of the device at power up keeps the Spread Spectrum disabled, it is therefore, important to have SMBUS accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by SST(0:2) in SMBUS byte 5, bits 5, 6 & 7 following tables 4A, and 4B below.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by ½ of the total spread %. (ex.: assuming the center frequency is 100MHz in non-spread mode; when down spread of –0.5% is enabled, the center frequency shifts to 99.75MHz.).

In Center Spread mode, the Center frequency remains the same as in the non-spread mode.

Down Spread

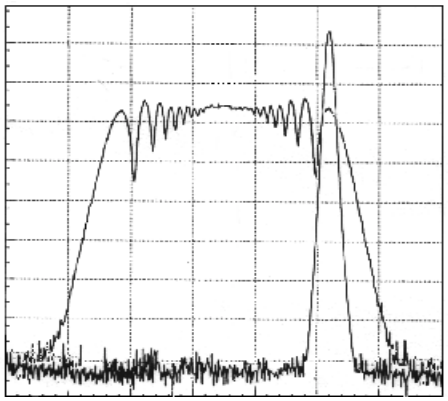


Fig.9A

Center Spread

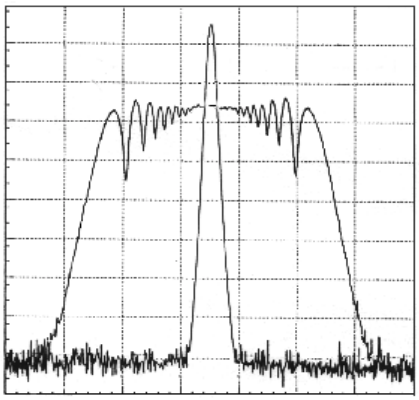


Fig.9B

Spread Spectrum Selection Tables

I²C BYTE5 Bit[7:5]	Center Frequency (MHz)	Spread %
100	66/100	± 0.25
101	66/100	± 0.35
110	66/100	± 0.5
111	66/100	± 0.7

Table 4A

I²C BYTE5 Bit[7:5]	Center Frequency (MHz)	Spread %
000	66/100	- 0.5
001	66/100	- 0.7
010	66/100	- 1.0
011	66/100	- 1.5

Table 4B

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65ºC to + 150ºC
Operating Temperature: 0ºC to +85ºC
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	note 1
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Voltage	VIL2	-	-	1.0	Vdc	note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL =VSS)	IIL	-66		-5	µA	For internal Pull up resistors, note 1 and note 3
Input High Current (@VIL =VDD)	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	280	mA	Sel1 = Sel0 = 1, note 4
Dynamic Supply Current	Idd2.5V	-	-	100	mA	Sel1 = Sel0 = 1, note 4
Static Supply Current	Isdd	-	-	3.2	mA	PD# = 0, Sel1 = Sel0 = x, note 4
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin capacitance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	32	34	38	pF	Measured from Pin to Ground. note 5
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
VDD=VDDS = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0º to +70ºC						

Note1: Applicable to input signals: Sel(0:1), PD#
Note2: Applicable to Sdata, and Sclk.
Note3: Although internal pull-up resistors have a typical value of 250K, this value may vary between 200K and 500K.
Note4: All outputs loaded as per table 3.
Note5: Although the device will reliably interface with crystals of a 17pF – 20pF C_L range, it is optimized to interface with a typical C_L = 18pF crystal specifications.

Clock name	Max Load (in pF)
CPU, IOAPIC, REF, USB (0:1)	20
PCI, SDRAM, 3V66(0,1)	30

Table 5.

AC Parameters

Symbol	Parameter	66 MHz Host		100 MHz Host		Units	Notes
		Min	*Max*	*Min*	*Max*		
TPeriod	Host/CPU CLK period	15.0	15.5	10.0	10.5	nS	2,7
THigh	Host/CPU CLK high time	5.2	-	3.0	-	nS	3
TLow	Host/CPU CLK low time	5.0	-	2.8	-	nS	4
Edge Rate	Rising edge rate	1.0	4.0	1.0	4.0	V/nS	
Edge Rate	Failing edge rate	1.0	4.0	1.0	4.0	V/nS	
T Rise	Host/CPU CLK rise time	0.4	1.6	0.4	1.6	nS	1
T Fall	Host/CPU CLK fall time	0.4	1.6	0.4	1.6	nS	1
Tperiod	IOAPIC 33 MHz CLK period	30.0	-	30.0	-	nS	2,7
THigh	IOAPIC 33 MHz CLK high time	12.0	-	12.0	-	nS	3
TLow	IOAPIC 33 MHz CLK low time	12.0	-	12.0	-	nS	4
Edge Rate	Rising edge rate	1.0	4.0	1.0	4.0	V/nS	
Edge Rate	Failing edge rate	1.0	4.0	1.0	4.0	V/nS	
T Rise	IOAPIC 33 MHz CLK rise time	0.4	1.6	0.4	1.6	nS	1
T Fall	IOAPIC 33 MHz CLK fall time	0.4	1.6	0.4	1.6	nS	1
Tperiod	IOAPIC 16.67 MHz CLK period	60.0	64.0	60.00	64.0	nS	2,7
THigh	IOAPIC 16.67 MHz CLK high time	25.5	-	25.5	-	nS	3
TLow	IOAPIC 16.67 MHz CLK low time	25.3	-	25.3	-	nS	4
Edge Rate	Rising edge rate	1.0	4.0	1.0	4.0	V/nS	
Edge Rate	Failing edge rate	1.0	4.0	1.0	4.0	V/nS	
T Rise	IOAPIC 16.67 MHz CLK rise time	0.4	1.6	0.4	1.6	nS	1
T Fall	IOAPIC 16.67 MHz CLK fall time	0.4	1.6	0.4	1.6	nS	1
Tperiod	3V66 CLK period	15.0	16.0	15.0	16.0	nS	2,7
THigh	3V66 CLK high time	5.25	-	5.25	-	nS	3
TLow	3V66 CLK low time	5.05	-	5.05	-	nS	4
Edge Rate	Rising edge rate	1.0	4.0	1.0	4.0	V/nS	
Edge Rate	Failing edge rate	1.0	4.0	1.0	4.0	V/nS	
T Rise	3V66 CLK rise time	0.5	2.0	0.5	2.0	nS	1
T Fall	3V66 CLK fall time	0.5	2.0	0.5	2.0	nS	1

AC Parameters (Cont.)

Symbol	Parameter	66 MHz Host		100 MHz Host		Units	Notes
		Min	Max	Min	Max		
Tperiod	PCI CLK period (and 33 MHz IOAPIC)	30.00	-	30.0	-	nS	2,7
THigh	PCI CLK high time (& 33 MHz IOAPIC)	12.0	-	12.0	-	nS	3
TLow	PCI CLK low time (& 33 MHz IOAPIC)	12.0	-	12.0	-	nS	4
Edge Rate	Rising edge rate	1.0	4.0	1.0	4.0	V/nS	
Edge Rate	Failing edge rate	1.0	4.0	1.0	4.0	V/nS	
T Rise	PCI CLK rise time (& 33 MHz IOAPIC)	0.5	2.0	0.5	2.0	nS	1
T Fall	PCI CLK fall time (& 33 MHz IOAPIC)	0.5	2.0	0.5	2.0	nS	1
Tperiod	SDRAM CLK period	10.0	10.5	10.0	10.5	nS	2,7
THigh	SDRAM CLK high time	3.0	-	3.0	-	nS	3
TLow	SDRAM CLK low time	2.8	-	2.8	-	nS	4
Edge Rate	Rising edge rate	1.5	4.0	1.5	4.0	V/nS	
Edge Rate	Failing edge rate	1.5	4.0	1.5	4.0	V/nS	
T Rise	SDRAM CLK rise time	0.4	1.6	0.4	1.6	nS	1
T Fall	SDRAM CLK fall time	0.4	1.6	0.4	1.6	nS	1
Tjc-c	48 MHz Clock Cycle to Cycle Jitter	-	500	-	500	pS	2
tpZL,tpZH	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	nS	
tpLZ,tpZH	Output disable delay (all outputs)	1.0	10.0	1.0	10.00	nS	
tstable	All clock Stabilization from power-up		3		3	mS	5

Notes:
1. Output drivers must have monotonic rise/fall times through the specified VOL/VOH levels.
2. Period, jitter, offset and skew measured on rising edge @ 1.25V for 2.5V clocks and @ 1.5V for 3.3V clocks.
3. THigh is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
4. TLow is measured at 0.4V for all outputs.
5. The time specified is measured from when Vddq achieves its nominal operating level (typical condition Vddq = 3.3V) the frequency output is stable and operating within specification.
6. Trise and Tfall are measured as a transition through the threshold region Vol = 0.4V and Voh = 2.0V
7. The average period over any 1 uS period of time must be greater than the minimum specified period.

Output Buffer Characteristics

Buffer Characteristics for CPU

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	13	-	-	mA	Vout =VDDC - 0.5V
Pull-Up Current	IOH_2	25	-	-	mA	Vout = 1.2 V
Pull-Down Current	IOL_1	11	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	25	-	-	mA	Vout = 1.2 V
Dynamic Output Impedance	Z0	13.5		45	Ω	
Rise Time Min Between 0.4 and 2.0 V	Tr	0.4	-	-	nS	20pF Load
Fall Time Max Between 0.4 and 2.0 V	Tf	-	-	1.6	nS	20pF Load

Buffer Characteristics for PCI and 3V66

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	14	-	-	mA	Vout =VDDC – 0.5V
Pull-Up Current	IOH_2	35	-	-	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	13	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	40	-	-	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	12		55	Ω	
Rise Time Min Between 0.4 and 2.4 V	Tr	0.5	-	-	nS	30pF Load
Fall Time Max Between 0.4 and 2.4 V	Tf	-	-	2.0	nS	30pF Load

Buffer Characteristics for USB (0:1) and REF

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	6	-	-	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	15	-	-	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	6	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	22	-	-	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	20		60	Ω	
Rise Time Min Between 0.4 and 2.4 V	Tr	0.4	-	-	nS	20pF Load
Fall Time Max Between 0.4 and 2.4 V	Tf	-	-	4.0	nS	20pF Load

Output Buffer Characteristics (Cont.)

Buffer Characteristics for IOAPIC

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	13	-	-	mA	Vout =VDDI - 0.5V
Pull-Up Current	IOH_2	25	-	-	mA	Vout = 1. 0 V
Pull-Down Current	IOL_1	11	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	25	-	-	mA	Vout = 1.4 V
Dynamic Output Impedance	Z0	13.5		45	Ω	
Rise Time Min Between 0.4 and 2.0 V	Tr	1.0	-	-	nS	20pF Load
Fall Time Max Between 0.4 and 2.0 V	Tf	-	-	1.6	nS	20pF Load

Buffer Characteristics for SDRAM

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	19	-	-	mA	Vout =VDD - 1. 0 V
Pull-Up Current	IOH_2	62	-	-	mA	Vout = 1. 4 V
Pull-Down Current	IOL_1	18	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	59	-	-	mA	Vout = 1.5 V
Dynamic Output Impedance	Z0	10		24	Ω	
Rise Time Min Between 0.4 and 2.4 V	Tr	0.4	-	-	nS	30pF Load
Fall Time Max Between 0.4 and 2.4 V	Tf	-	-	1.33	nS	30pF Load
VDD=VDDS=3.3V ±5%, VDDC=VDDI=2.5±5%, TA=0 to 70ºC						

Suggested Crystal Oscillator Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) Note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) Note 1
Mode	OM	-	-	-		Parallel Resonant, Note 1
Load Capacitance	CL	-	18	-	pF	The crystal's rated load. Note 1
Effective Series resistance (ESR)	R1	-	40	-	Ohms	Note 1
Power Dissipation	DL	-	-	0.10	mW	Note 1
Shunt Capacitance	CO	-	--	8	pF	Crystal's internal package capacitance (total)

Note1: For best performance and accurate Center frequencies of this device, It is recommended but not mandatory that the chosen crystal meets these specifications

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Device pin capacitance: Cxtal = 36pF
In order to meet the specification for CL = 18*p*F following the formula:

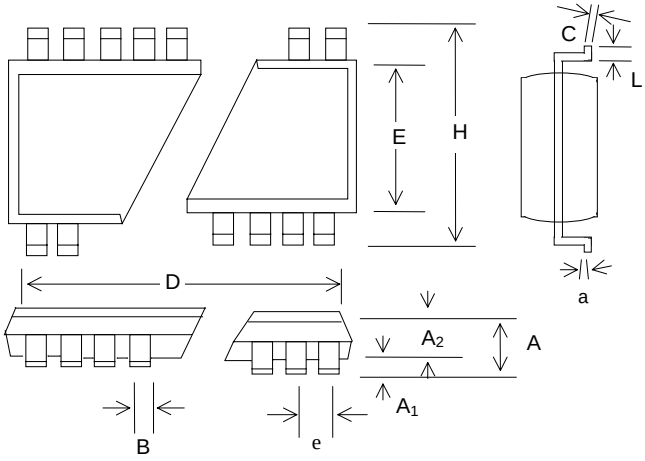
$$C_L = \frac{C_{XIN} x C_{XOUT}}{C_{XIN} + C_{XOUT}}$$

Then the board trace capacitance between Xin and the crystal should be no more than 2pF. (same is applicable to the trace between Xout and the crystal)
In this case the total capacitance from the crystal to Xin will be 36pF. Similarly the total capacitance between the crystal and Xout will be 36pF. Hence using the above formula:

$$C_L = \frac{36\,pFx36\,pF}{36\,pF + 36\,pF} = 18\,pF$$

Low EMI Clock Generator for Intel® 810 Chipset Systems

Package Drawing and Dimensions



56 Pin SSOP Outline Dimensions						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.088	0.090	0.092	2.24	2.29	2.34
B	0.008	0.010	0.0135	0.203	0.254	0.343
C	0.005	-	0.010	0.127	-	0.254
D	.720	.725	.730	18.29	18.42	18.54
E	0.292	0.296	0.299	7.42	7.52	7.59
e	0.025 BSC			0.635 BSC		
H	0.400	0.406	0.410	10.16	10.31	10.41
a	0.10	0.013	0.016	0.25	0.33	0.41
L	0.024	0.032	0.040	0.61	0.81	1.02
a	0º	5º	8º	0º	5º	8º
X	0.085	0.093	0.100	2.16	2.36	2.54

Ordering Information

Part Number	Package Type	Production Flow
C9811X2AYB	56 PIN SSOP	Commercial, 0 to 70ºC

Marking: Example: Cypress
C9811X2
Date Code, Lot #

C9811X2AYB

Flow
B = Commercial, 0 to 70ºC

Package
Y = SSOP

Revision

Device Number

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Document Number: 38-07052

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107060	06/11/01	IKA	Convert from IMI to Cypress