256K (32K x 8) Low Voltage UV Erasable CMOS EPROM

Features

- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C256R
- Low Power 3-Volt CMOS Operation
  - 100 µA max. Standby
  - 26 mW max. Active at 1 MHz for V_{CC} = 3.3 VDC
  - 110 mW max. Active at 5 MHz for V_{CC} = 5.5 VDC
- Read Access Time - 200ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead, 600-mil Cerdip and OTP Plastic DIP, SOIC, or TSOP
  - 32-Pad LCC, 32-Lead JLCC, and OTP PLCC
- High Reliability CMOS Technology
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming - 100 µs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

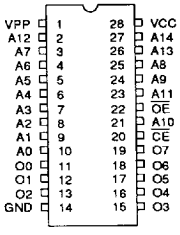
The AT27LV256R chip is a low power, low voltage 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 32K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18 mW at 1 MHz and V_{CC} at 3.3 VDC, the AT27LV256R will draw less than one-fifth the power of a standard 5-volt EPROM. Standby mode supply current is typically less than 10 µA.

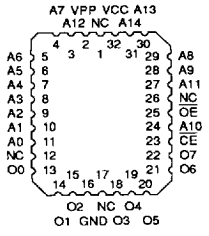
Pin Configurations

Pin Name	Function
A0-A14	Addresses
O0-O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

CDIP, PDIP, SOIC Top View

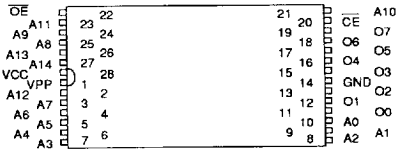


LCC, JLCC, PLCC Top View



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT

TSOP Top View
Type 1



Description (Continued)

The AT27LV256R comes in a choice of industry standard JEDEC-approved through hole and surface mount packages including windowed and one time programmable (OTP) packages, such as the OTP thin small outline package (TSOP). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

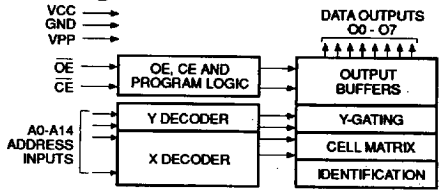
The AT27LV256R operating with V_{CC} at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0 VDC.

Atmel's 27LV256R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV256R programs identically as an AT27C256R.

Erasure Characteristics

The entire memory array of the AT27LV256R is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W-sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X(5)	V_{CC}	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify(2)	X	V_{IL}	Ai	V_{PP}	V_{CC} (2)	D_{OUT}
Optional PGM Verify(2)	V_{IL}	V_{IL}	Ai	V_{CC}	V_{CC} (2)	D_{OUT}
PGM Inhibit(2)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC} (2)	High Z
Product Identification(2),(4)	V_{IL}	V_{IL}	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A14=V_{IL}	V_{CC}	V_{CC} (2)	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics. Programming modes require V_{CC} > 4.5 V.
3. V_H = 12.0 ± 0.5 V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} Current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27LV256R	
		-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		3.0 V to 5.5 V	3.0 V to 5.5 V

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D.C. and Operating Characteristics for Read Operation

(V_{CC} = 3.0V to 5.5V unless otherwise specified)

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = V_{CC}-0.7 V to V_{CC}+0.3 V				10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V				100	µA
		I_{SB2} (TTL), $\overline{CE}$=2.0 to V_{CC}+1.0V				1	mA
I_{CC}	V_{CC} Active Current	I_{CC1}	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 5.5 V	Com.		20	mA
				Ind.		25	mA
		I_{CC2}	f = 1 MHz, I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}, V_{CC} = 3.3 V	Com.		8	mA
				Ind.		10	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA				.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA			V_{CC}-0.3		V
		I_{OH} = -400 µA			2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

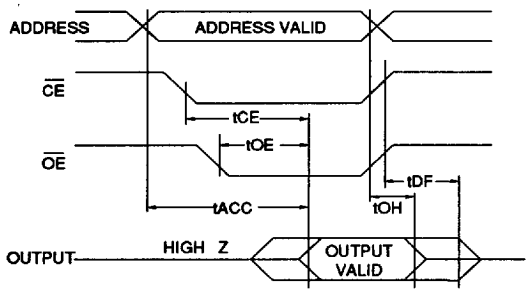
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation (V_{CC} = 3.0 V to 5.5 V)

				AT27LV256R				
				-20		-25		
Symbol	Parameter	Condition		Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		200		250	ns
			Ind.		200		250	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			200		250	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			70		100	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}			50		50	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		ns

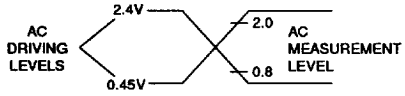
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



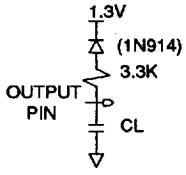
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V. See Input Test Waveforms and Measurement Levels.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



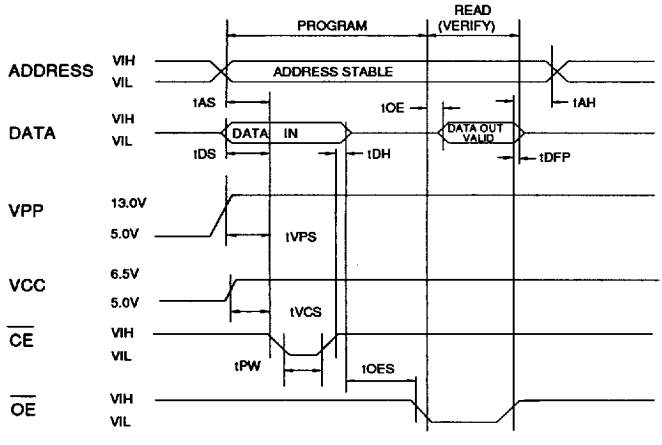
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f= 1 MHz, T=25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Notes: 1. Typical values for 5-V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27LV256R a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25 V, V_{PP} = 13.0 ± 0.25 V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	V_{IN}=V_{IL},V_{IH}		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+1	V
V_{OL}	Output Low Volt.	I_{OL}=2.1 mA		.45	V
V_{OH}	Output High Volt.	I_{OH}=-400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	V_{PP} Current	$\overline{CE}$=V_{IL}		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25 V, V_{PP} = 13.0 ± 0.25 V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$	(Note 2)		150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ±5%.

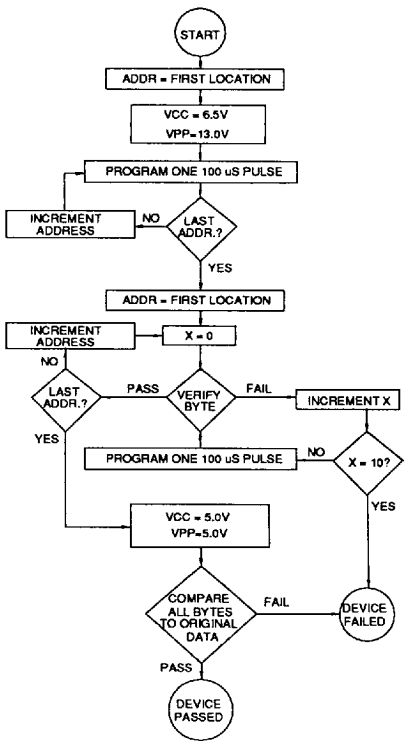
Atmel's 27LV256R Integrated Product Identification Code[1]

Codes	Pins A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Note: 1. The AT27LV256R has the same Product Identification Code as the AT27C256R. Both are programming compatible.

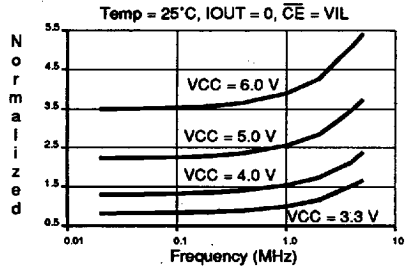
Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All bytes are read again and compared with the original data to determine if the device passes or fails.

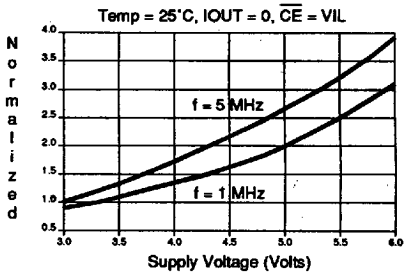


LV EPROM Product Characteristics

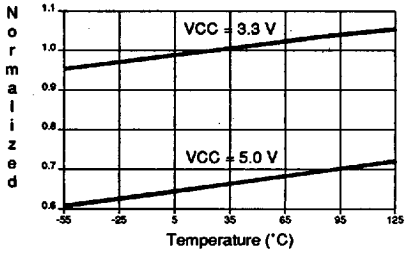
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



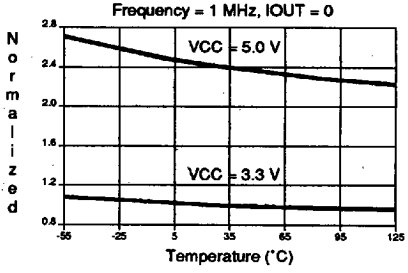
NORMALIZED SUPPLY CURRENT vs. VOLTAGE



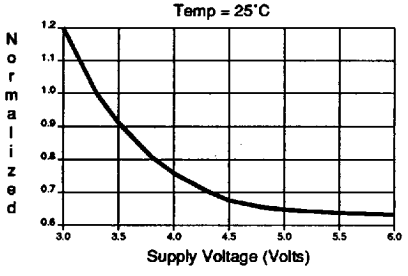
NORMALIZED ACCESS TIME vs. TEMPERATURE



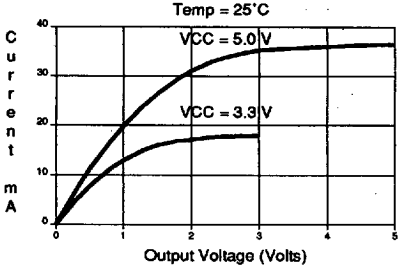
NORMALIZED SUPPLY CURRENT vs. TEMP.



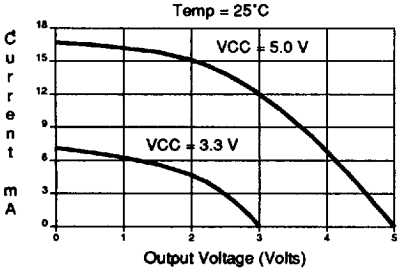
NORMALIZED ACCES TIME vs. SUPPLY VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
200	8	0.1	AT27LV256R-20DC AT27LV256R-20JC AT27LV256R-20KC AT27LV256R-20LC AT27LV256R-20PC AT27LV256R-20RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
200	10	0.1	AT27LV256R-20DI AT27LV256R-20KI AT27LV256R-20LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)
250	8	0.1	AT27LV256R-25DC AT27LV256R-25JC AT27LV256R-25KC AT27LV256R-25LC AT27LV256R-25PC AT27LV256R-25RC	28DW6 32J 32KW 32LW 28P6 28R	Commercial (0°C to 70°C)
250	10	0.1	AT27LV256R-25DI AT27LV256R-25KI AT27LV256R-25LI	28DW6 32KW 32LW	Industrial (-40°C to 85°C)

t_{ACC} (ns)	I_{CC} (mA) V_{CC} = 3.3 V		Ordering Code	Package	Operation Range
	Active	Standby			
200	8	0.1	AT27LV256R-20TC	28T	Commercial (0° to 70°C)
250	8	0.1	AT27LV256R-25TC	28T	Commercial (0° to 70°C)

Package Type	
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32KW	32 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package OTP (TSOP)