T-52-31

>> 32 bit bus transceiver/register, non-inverting or inverting.

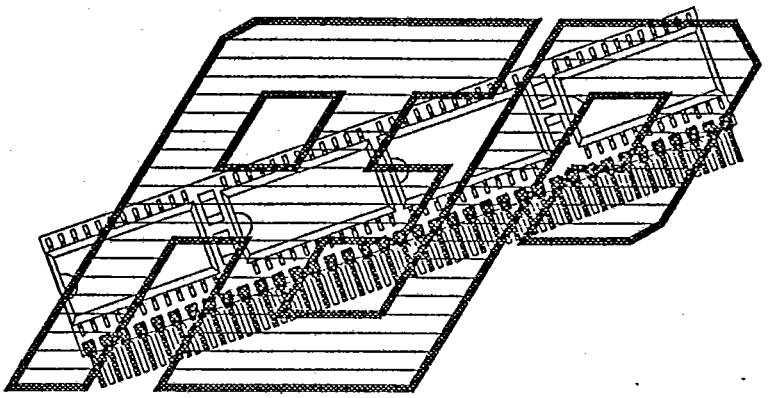
>> High density .070 center spaced ZIP leads for maximum I/O in minimum area.

>> Space saving vertical mounting orientation.

>> Convenient "In one side, out the other" broadside pin-out.

>> TTL compatible

>> Uses single +5V power supply



32 LINE TRANSCEIVER REGISTER MODULE

DESCRIPTION:

The AEPT/RZ32 is a high speed, high density 32-line transceiver/register module ideal for use with 16 or 32-bit wide address/data paths or buses. It combines the advantages of the 646 (non-inverting) or 648 (inverting) type octal transceiver/register ICs with very large data widths and a space saving configuration.

Use of the 646 type ICs provides independent registers for A and B buses, multiplexed real-time and stored data, 3-state outputs, and a choice of true or inverted data paths. The vertical mounting orientation and compact I/O pin footprint of the module make it superb for projects with tight space constraints.

Physically the module consists of an FR4 PC material substrate mounted with four 646 or 648 type transceiver/register ICs, four 0.10 microfarad decoupling capacitors, and 75 I/O pins in a staggered ZIP package format. It can be ordered with any 646 or 648 type register made by any manufacturer producing them in a 24 pin SOP package. The module features all the 646 control lines connected in common to all four ICs except the Output Enable which is split into G-low and G-high controlling 16 lines each. Both G-low and G-high are active LOW.

Performance specifications and electrical characteristics are determined by the IC devices used. These items can vary according to the type and manufacturer of the components. The necessary information is obtained from the IC vendors' data sheets, like those attached, or from their data books.

Mechanical dimensions are 0.505 inch high by 2.66 inches long by 0.22 inch wide. The I/O pins are in two rows which are 0.1 inch apart and offset longitudinally 0.035 inch. In each row the pins are on 0.070 inch center spacing. See included specification drawing.

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PART NUMBERING CHART

T/RZ32 with non-inverting	
74F646 transceiver/register	AEPT/RZ32-F646
74FCT646 transceiver/register	AEPT/RZ32-FCT646
74LS646 transceiver/register	AEPT/RZ32-LS646
T/RZ32 with inverting	
74F648 transceiver/register	AEPT/RZ32-F648
74FCT648 transceiver/register	AEPT/RZ32-FCT648
74LS648 transceiver/register	AEPT/RZ32-LS648

Transceiver/Register notes:
The standard transceiver/register used is the 74FCT646A or 74PCT646A. Please contact AEP if a type that is not listed above is desired. If the pin out configuration is the same as the 74FCT646 or 74FCT648 and the desired type is available in a standard 24 pin SOP, there should be no problem using it on the module.

The "A" at the end of the standard IC number is a "High Performance" speed indicator. AEP may use the "A" version of a device even if it is not explicitly specified unless requested not to. An exact specification (type and manufacturer) of the IC device desired is recommended. Please contact AEP for assistance if needed.

Vendor notes:
The IC device specification information included is typical and does not limit AEP to that vendor. The actual devices used will be equivalent depending on price, availability, and customer requirements. AEP will gladly use or exclude particular manufacturers upon request. However, this might affect module price.

Disclaimers:
The information in this document has been carefully checked and is believed to be reliable. However, Advanced Electronic Packaging Inc. assumes no responsibility for inaccuracies. AEP also reserves the right to change products or specifications without notice.

T-52-31

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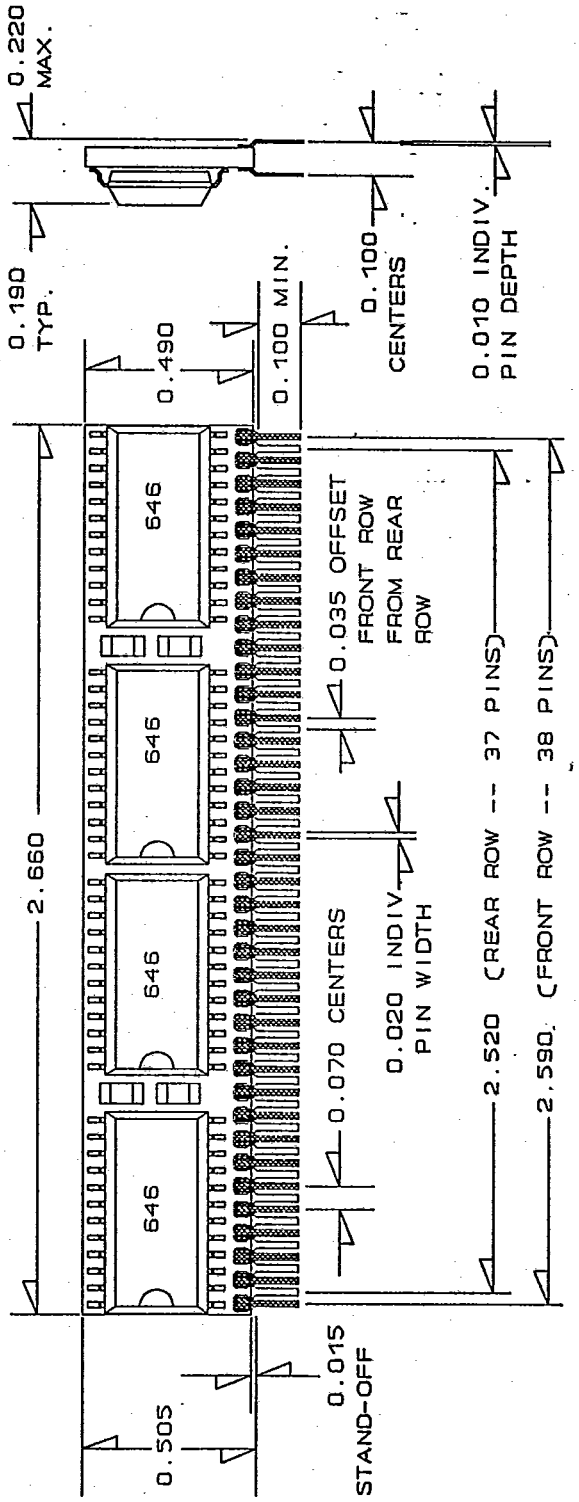
AEPT/RZ32-646
32 LINE TRANSCEIVER/REGISTER

DIMENSIONS IN INCHES. TOLERANCE: +/- 0.010 UNLESS SPECIFIED.



75 PINS TOTAL

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32 LINE TRANSCEIVER/REGISTER MODULE PIN CONFIGURATION (TOP VIEW)

	PIN #s		
A INPUTS /B OUTPUTS	A_1 – 1	2 – B_1	B INPUTS /A OUTPUTS
	A_2 – 3	4 – B_2	
	A_3 – 5	6 – B_3	
	A_4 – 7	8 – B_4	
	A_5 – 9	10 – B_5	
	A_6 – 11	12 – B_6	
	A_7 – 13	14 – B_7	
	A_8 – 15	16 – B_8	
OUTPUT ENABLE$_{LOW}$	G_L – 17	18 – SAB	TRANSMIT/RECEIVE A-B
CLOCK PULSE A-B	CPAB – 19	20 – GND	GROUND
A INPUTS /B OUTPUTS	A_9 – 21	22 – B_9	B INPUTS /A OUTPUTS
	A_{10} – 23	24 – B_{10}	
	A_{11} – 25	26 – B_{11}	
	A_{12} – 27	28 – B_{12}	
	A_{13} – 29	30 – B_{13}	
	A_{14} – 31	32 – B_{14}	
	A_{15} – 33	34 – B_{15}	
	A_{16} – 35	36 – B_{16}	
POWER	Vcc – 37	38 – Vcc	POWER
A INPUTS /B OUTPUTS	A_{17} – 39	40 – B_{17}	B INPUTS /A OUTPUTS
	A_{18} – 41	42 – B_{18}	
	A_{19} – 43	44 – B_{19}	
	A_{20} – 45	46 – B_{20}	
	A_{21} – 47	48 – B_{21}	
	A_{22} – 49	50 – B_{22}	
	A_{23} – 51	52 – B_{23}	
	A_{24} – 53	54 – B_{24}	
GROUND	GND – 55	56 – CPBA	CLOCK PULSE B-A
OUTPUT ENABLE$_{HIGH}$	G_H – 57	58 – SBA	TRANSMIT/RECEIVE B-A
A INPUTS /B OUTPUTS	A_{25} – 59	60 – B_{25}	B INPUTS /A OUTPUTS
	A_{26} – 61	62 – B_{26}	
	A_{27} – 63	64 – B_{27}	
	A_{28} – 65	66 – B_{28}	
	A_{29} – 67	68 – B_{29}	
	A_{30} – 69	70 – B_{30}	
	A_{31} – 71	72 – B_{31}	
	A_{32} – 73	74 – B_{32}	
OUTPUT DIRECTION	DIR – 75		

Note: OUTPUT ENABLEs are active LOW.

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32 LINE TRANSCEIVER/REGISTER MODULE FUNCTIONAL DIAGRAM