ANALOG DEVICES

Very Fast, Complete 12-Bit A/D Converter

AD5240

T-51-10-12

1.1 Scope.

This specification covers the detail requirements for a hybrid high speed 12-bit successive approximation analog-to-digital converter including internal clock, reference and comparator.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD5240BD/883B
−2	AD5240ZBD/883B
−3	AD5240SD/883B
−4	AD5240ZSD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32D.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage	±18V
Logic Supply Voltage	+7V
Analog Inputs (Pins 24, 25)	±25V
Digital Inputs	+5.5V
Junction Temperature	+175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.3.1 Operating Temperature Range.

The operating temperature range of this device is −25°C to +85°C (−1, −2)
−55°C to +125°C (−3, −4).

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 8°C/W
θ_{JA} = 38°C/W

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Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group[2] 2,3	Sub Group 4	Test Condition[1]	Units
Analog Input Voltage Ranges	V_{IN}	–1,3	±2.5, ±5, ±10 0 to 5 0 to 10					V
	V_{IN}	–2,4	±2.5, ±5 0 to 5				$\pm V_{CC}$ = ±12V $+V_{DD}$ = +5V	V
Serial Parallel Code Match Error	SP_{CM}	–1,2,3,4	0	0			Random Codes	±Bits
Input Impedance	R_{IN}	–1,2,3,4	3			3	±5V Input Range	kΩ min
			7			7		kΩ max
Logic Outputs	V_{OL}	–1,2,3,4	0.4			0.4	I_{OL} = 3.2mA	V max
	V_{OH}	–1,2,3,4	2.4			2.4	I_{OH} = –80μA	V min
Buffer Amp Bias Current	I_B	–1,2,3,4	100			100		±nA max
Buffer Amp Offset Error	B_{OS}	–1,2,3,4	10			10		±mV max
Buffer Amp Common-Mode Rejection	B_{CMR}	–1,2,3,4	70			70		dB min
Buffer Amp Settling Time	t_S	–1,2,3,4	2				To 0.01% for 20V Step	μs max
Reference Output Error	V_{REF}	–1,2,3,4	20	20			6.3V Nominal	±mV max
Reference Voltage Drift	V_{REF}	–1,2,3,4	10		10			±ppm/°C max
Unipolar Gain Error[3]	V_{GE}	–1,2,3,4	0.3				0 to +10V Input Range	±% FSR max
Unipolar Offset Error	V_{OSE}	–1,2,3,4	0.1					±% FSR max
Unipolar Offset Drift	V_{OD}	–1,2,3,4	7		7			±ppm/°C max
Bipolar Gain Error[3]	V_{GE}	–1,2,3,4	0.4				+10V Input Range	±% FSR max
Bipolar Gain Drift	V_{GD}	–1,2,3,4	25		25		±5V Range	±ppm/°C max
Bipolar Zero Error	B_{PZ}	–1,2,3,4	0.2				±10V Input Range	±% FSR max
Bipolar Zero Drift	V_{BZD}	–1,2,3,4	7		7		±5V Range	±ppm/°C max
Integral Linearity Error Over Temperature	L_E	–1,2	1/2			1/2	Major Carries & Summations	±LSB max
		–1,2			2			±ppm/°C max
		–3,4			3			
Differential Linearity, Error[4]	D_{LE}	–1,2,3,4	0.75	1	1		Major Carries & Summations	±LSB max
Conversion Speed		–1,2,3,4	5	5			Pin 17 Tied to +5V	μs max
±Power Supply Sensitivity	$PSRR_1$	–1,2,3,4	0.004			0.004	V_{CC} = ±13.5V to ±16.5V	±% FSR/ % V_{CC}
±12V Power Supply Sensitivity	$PSRR_2$	–2,4	0.007				V_{CC} = +11.4V to ±16.5V	±% FSR/ % V_{CC}
+5V Power Supply Sensitivity	$PSRR_3$	–1,2,3,4	0.01			0.01	V_{DD} = +4.75V to +5.25V	±% FSR/ % V_{DD}
+15V Supply Drain	$-I_{CC}$	–1,2,3,4	18			18		mA max
–15V Supply Drain	$-I_{CC}$	–1,2,3,4	38			38		mA max
+5V Supply Drain	$+I_{DD}$	–1,2,3,4	60			60		mA max
Power Dissipation	P_D	–1,2,3,4	1450			1450		mW max

NOTES
[1]T_A = +25°C and $\pm V_S$ = ±15V. V_{DD} = +5V unless otherwise specified.
[2]Subgroup 2 tests performed @ +85°C.
Subgroup 3 tests performed @ –25°C.
[3]Adjustable to zero.
[4]Guaranteed no missing codes –25°C to +85°C; for device –2, V_{CC} = ±12V.

Table 1.

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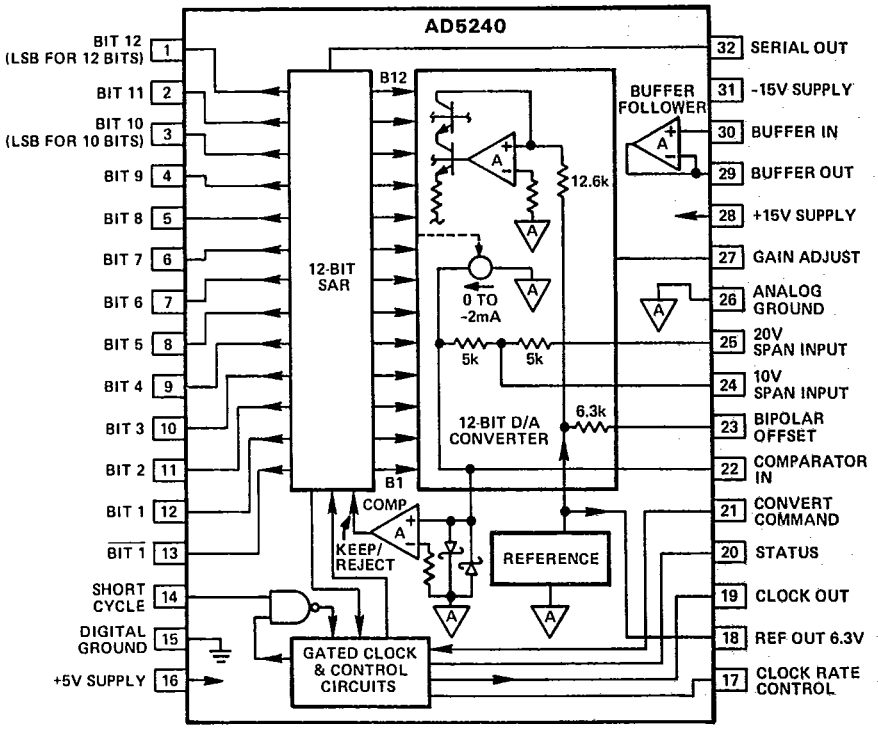
3.2.1 Functional Block Diagram and Terminal Assignments.

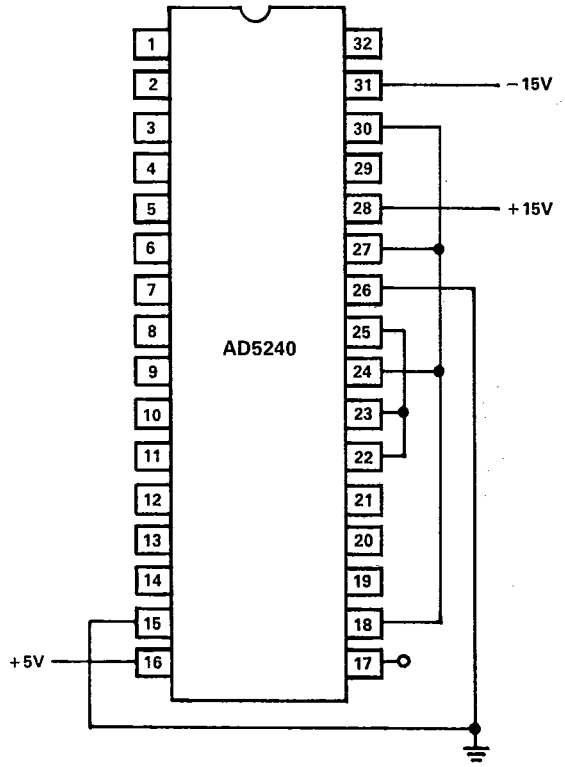


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



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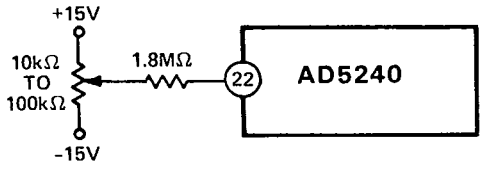


Figure 1. Adjustment Circuit

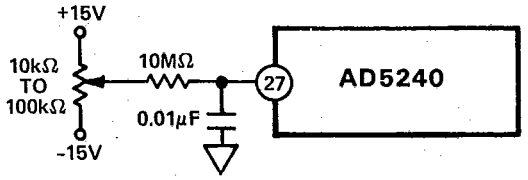


Figure 2. Gain Adjustment Circuit

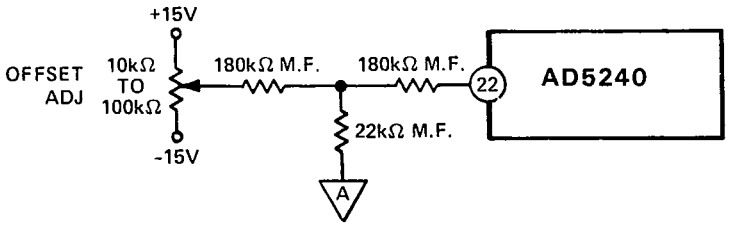


Figure 3. Low Tempco Zero Adjustment Circuit

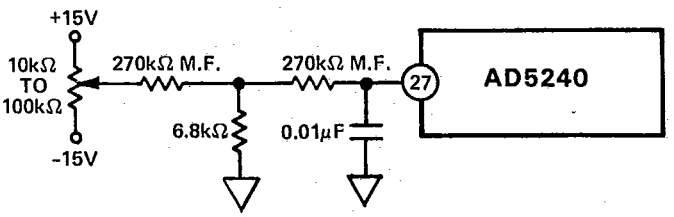
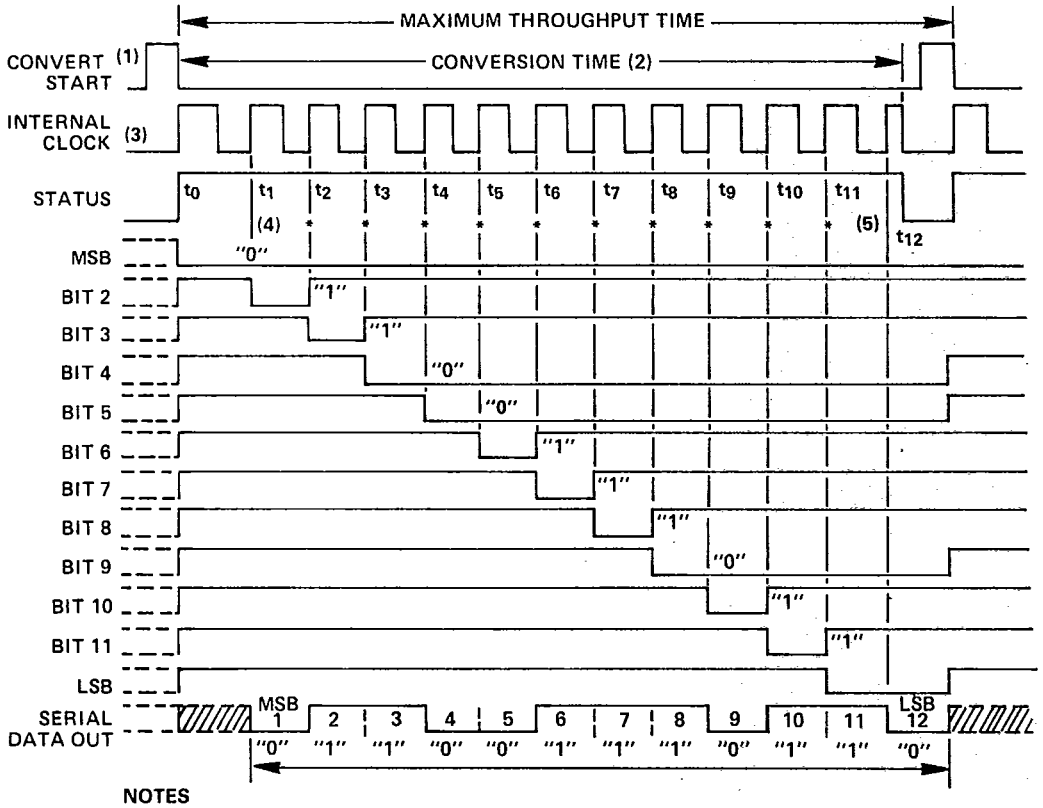


Figure 4. Low Tempco Gain Adjustment Circuit



NOTES
1. THE CONVERT START PULSE WIDTH IS 50ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 5μs FOR 12 BITS AND 4.2μs FOR 10 BITS (MAX – PIN 17 TO +5V).
3. FIRST CLOCK PULSE: 300(ns)H, 300(ns)L. SECOND THROUGH TWELFTH CLOCK PULSE: 100(ns)H, 300(ns)L.
4. MSB DECISION.
5. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW.
*BIT DECISIONS

Figure 5. Timing Diagram (Binary Code 0 1 1 0 0 1 1 1 0 1 1 0)

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6.1 Digital Output Data.

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether Bit 1 (pin 12) or its logical inverse $\overline{\text{Bit 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 50ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 5. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 5. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

The digital output codes corresponding to analog input voltages are shown in Tables 2 and 3.

INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available to pin 13.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table 2. Input Voltages and Code Definition

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
±10V	COB or CTC	22	Input Signal	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

Table 3. AD5240 Input Scaling Connections

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6.1.1 Short Cycle Input.

A Short Cycle input, pin 14, permits the timing cycle shown in Figure 5 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision t_{10} +40ns in timing diagram of Figure 5. Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table 4.

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
16	16	12	0.024	5.0	t_{12} +40ns
2	16	10	0.100	4.1	t_{10} +40ns
4	16	8	0.390	3.3	t_8 +40ns

Table 4. Short Cycle Connections