

REVISIONS

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PMIC N/A				PREPARED BY Gary L. Gross					DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444																					
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Jeff Bowling																										
				APPROVED BY Michael A. Frye																										
				DRAWING APPROVAL DATE 95-02-17																										
				REVISION LEVEL																										
				SIZE A		CAGE CODE 67268			5962-94745																					
				SHEET 1 OF 16																										

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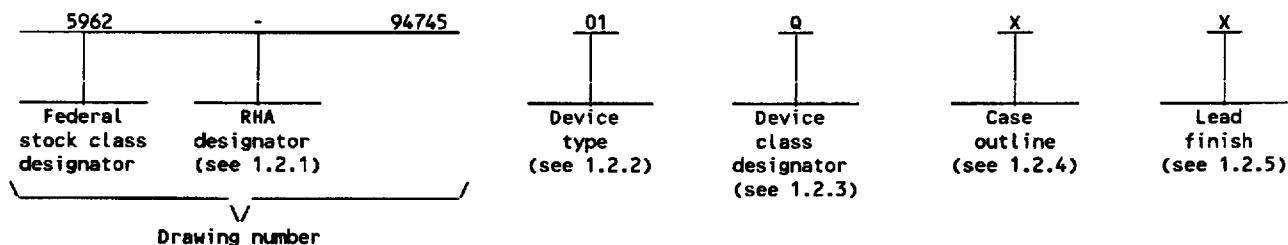
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1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number 1/</u>	<u>Circuit function</u>
01	1213	256K X 1-bit PROM

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.

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1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential (V_{CC}) -2.0 V dc to +7.0 V dc 3/
 DC input voltage -2.0 V dc to +7.0 V dc 3/
 Maximum power dissipation 100 mW
 Lead temperature (soldering, 10 seconds) +260°C
 Thermal resistance, junction-to-case (θ_{JC}) See MIL-STD-1835
 Junction temperature (T_J) +150°C
 Storage temperature range (T_{STG}) -65°C to +150°C
 Temperature under bias -55°C to +125°C
 Data retention 10 years, minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) +4.75 V dc minimum to +5.25 V dc maximum
 Ground voltage (GND) 0 V dc
 Input high voltage (V_{IH}) 2.0 V dc to $V_{CC} + 0.3$ V dc
 Input low voltage (V_{IL}) -3.0 V dc to 0.8 V dc
 Case operating temperature range (T_C) -55°C to +125°C

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
 logic tests (MIL-STD-883, test method 5012) XX percent 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MICROCIRCUIT

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MICROCIRCUIT

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
 MIL-STD-973 - Configuration Management.
 MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MICROCIRCUIT

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

HANDBOOK

MICROCIRCUIT

MIL-HDBK-780 - Standardized Military Drawings.

- 2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
 3/ Minimum dc input is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to +7.0 V for periods shorter than 20 ns under no-load conditions.
 4/ When a Qualified Manufacturers' List (QML) source exists, a value will be provided.

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(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified, the electrical performance characteristics, and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Power supply current (standby)	I_{CC1}		1,2,3		900	μA
Power supply current (active)	I_{CC} 1/	DCLK = 2 MHz	1,2,3		100	mA
Input leakage current	I_{IL}	$V_{IN} = \text{GND or } V_{CC}$	1,2,3		± 10	μA
Tri-state output off-state leakage current	I_{OZ}	$V_{OUT} = \text{GND or } V_{CC}$	1,2,3		± 10	μA
Input low voltage	V_{IL}		1,2,3	-0.3	0.8	V
Input high voltage	V_{IH}		1,2,3	2.0	$V_{CC} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4\text{ mA}$	1,2,3		0.45	V
Output high voltage	V_{OH}	$I_{OH} = -4\text{ mA}$	1,2,3	2.4		V
Output capacitance	C_{OUT} 2/	$f = 1.0\text{ MHz}$, $V_{OUT} = 0\text{ V}$ see 4.4.1c	4		10	pF
Input capacitance	C_{IN} 2/	$f = 1.0\text{ MHz}$, $V_{IN} = 0\text{ V}$ see 4.4.1c	4		10	pF
Functional tests		see 4.4.1d	7, 8A, 8B			
Clock frequency	f_{CK} 1/		9,10,11		6	MHz
Clock period	t_{CK}		9,10,11	160		ns
DCLK low time	t_{CL}		9,10,11	80		ns
DCLK high time	t_{CH}		9,10,11	80		ns
Input rise time	t_R 2/		9,10,11		20	ns
Input fall time	t_F 2/		9,10,11		20	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V \leq V _{CC} \leq 5.5 V -55°C \leq T _C \leq +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
OE high to DATA output enabled	t _{OEZX}		9,10,11		50	ns
nCS low to DATA output enabled	t _{CSZX}		9,10,11		50	ns
nCS high to DATA output enabled	t _{CSXZ} 3/		9,10,11		50	ns
nCS low setup time to first DCLK rising edge	t _{CSS}		9,10,11	100		ns
nCS low hold time after DCLK rising edge	t _{CSH}		9,10,11	0		ns
Data setup time before rising edge on DCLK	t _{DSU}		9,10,11	50		ns
Data hold time after rising edge on DCLK	t _{DH}		9,10,11	0		ns
DCLK to DATA out delay	t _{CO} 4/		9,10,11		75	ns
OE low or nCS high to DATA output disabled	t _{XZ} 3/		9,10,11		50	ns
OE pulse width to guarantee counter reset	t _{OEW}		9,10,11	100		ms
Last DCLK + 1 to nCASC low delay	t _{CASC}		9,10,11		60	ns
Last DCLK + 1 to data tri-state delay	t _{CKXZ} 3/		9,10,11		50	ns
nCS high to nCASC high delay	t _{CEOUT}		9,10,11		100	ns

1/ May not be tested, but shall be guaranteed to the limits specified in table I.

2/ C_{IN}, C_{OUT}, t^R, and t^F are not 100-percent tested but shall be guaranteed to the limits specified in table I.

3/ t_{CSXZ}, t_{XZ}, and t_{CKXZ} are parameters representing the device entering tri-state mode and, although not specifically tested, are guaranteed by characterization.

4/ Eight clock cycles are required after the t_{CSS} setup time has been met to clock out the first eight bits. These bits are all high and are used to synchronize the configuration process. The ninth clock cycle presents the first configuration data bit.

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Device type	01
Case outline	P
Terminal number	Terminal symbol
1	DATA
2	DCLK
3	OE
4	nCS
5	GND
6	nCASC
7	V _{CC}
8	V _{CC}

FIGURE 1. Terminal connections.

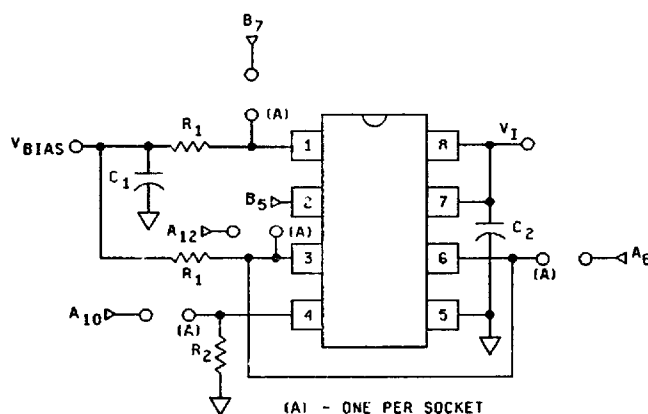
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Mode	DCLK	DATA	OE	nCS	nCASC
Read	V_{IL}/V_{IH}	V_{OL}/V_{OH}	V_{IL}/V_{IH}	V_{IL}/V_{IH}	V_{OL}/V_{OH}
Program	V_{IL}	V_{IL}	V_{IH}	V_{IL}/V_{IH}	V_{OH}
Verify	V_{IL}/V_{IH}	V_{OL}/V_{OH}	V_{IL}	V_{HH}	V_{OH}

FIGURE 2. Truth table.



- NOTES:
1. $R_1 = 625 \text{ ohm}$, 1/4 watt, 5 percent.
 2. $R_2 = 1 \text{ K ohm}$, 1/4 watt, 5 percent.
 3. $C_1 = 1.0 \mu\text{F}$, 50 volt, X7R (1 per socket).
 4. $C_2 = 0.1 \mu\text{F}$, 50 volt, X7R (1 per socket).
 5. $I_{CCA} = 23 \text{ mA}$ per unit (350 units maximum per board).
 6. Pins 1, 3, 4, and 6 must go to an eyelet that can be jumpered to the designated edge connector. The jumpers should not be attached at this time.
 7. Use standard EPLD dynamic burn-in driver configuration.

FIGURE 3. Output load circuit and test conditions.

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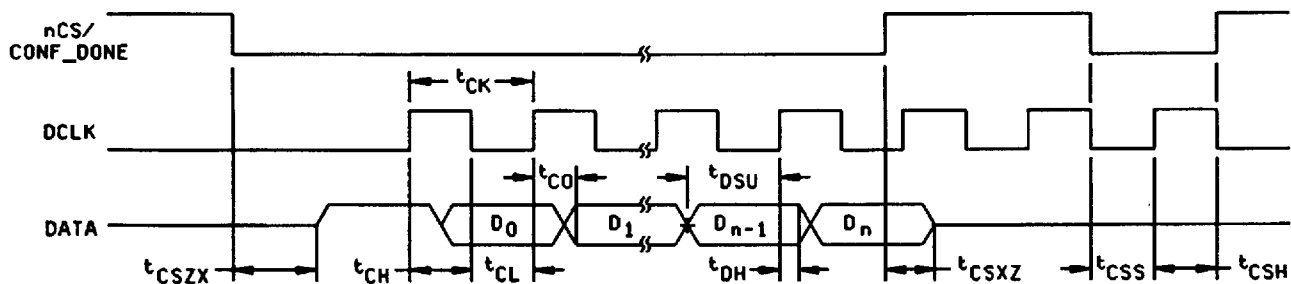


FIGURE 4. A. C. timing waveforms.

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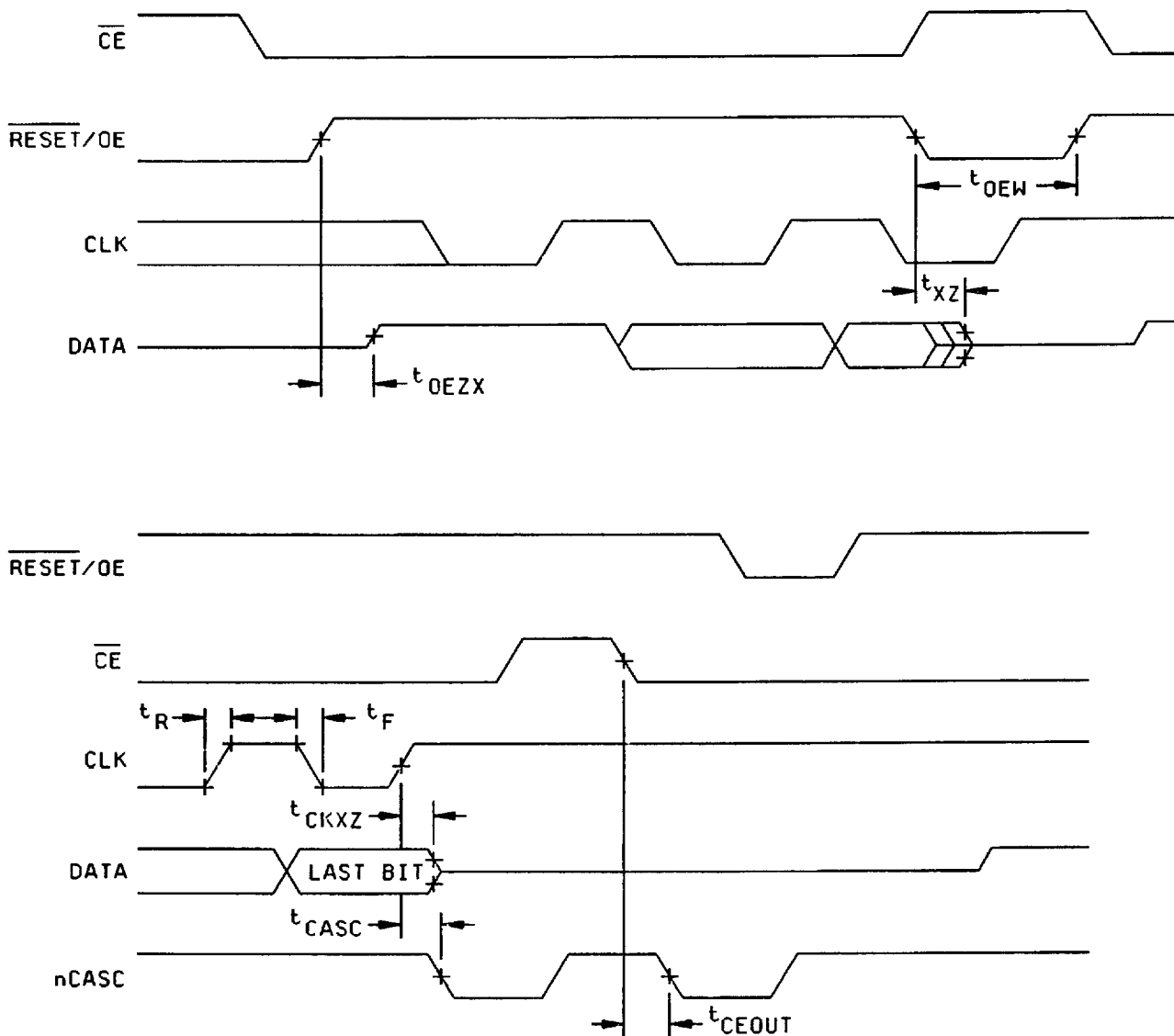


FIGURE 4. A. C. timing waveforms - continued.

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3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-I-38535, appendix A).

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).
- c. Interim and final electrical parameters shall be as specified in table IIA herein.

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4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.
- d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.
- f. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:
 - (1) Testing all devices submitted for test using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

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- (2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 4.5). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

g. Subgroups 7 and 8 shall include verification of the pattern specified in 4.4.1f.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. For group D inspection, end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/

Line no.	Test requirements	Subgroups (per method 5005, table I)	Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9 or 2,8A,10
2	Static burn-in I method 1015	Not required	Not required	Not required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,8A,10	2,8A,10	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	2,8A,10	2,8A,10	2,3,7 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate test are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * Indicates PDA applies to subgroups 1 and 7.

5/ ** See 4.4.1c.

6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see table IIA).

7/ See 4.4.1e.

8/ See 4.6.

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TABLE IIB. Delta limits at +25°C.

Test 1/	All device types
I _{IL}	±10 percent of specified value in table I
I _{OZ}	±10 percent of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions.

C_{IN} Input terminal capacitance.
C_{OUT} Output terminal capacitance.
GND Ground zero voltage potential.
I_{CC} Supply current.
I_{IL} Input current.
I_{OZ} Output current.
T_C Case temperature.
V_{CC} Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

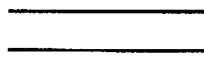



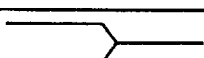
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6.5.2 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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