REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18															

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
94-01-20

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, CMOS, DIGITAL, SCAN PATH LINKERS WITH 4-BIT ID BUS, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-93239
A	67268	

SHEET 1 OF 18

DESC FORM 193
JUL 91

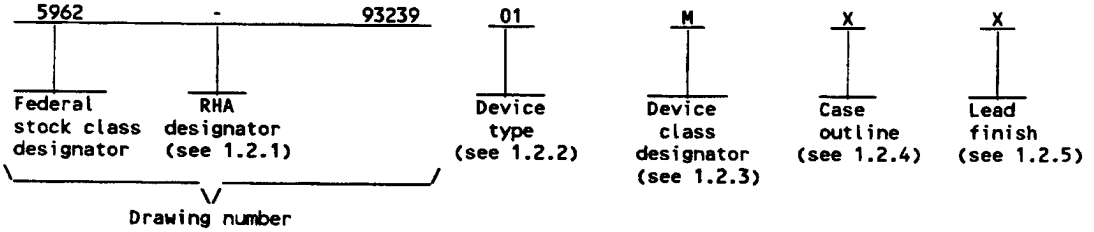
5962-E463-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q, and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT8997	Scan path linkers with 4-bit identification buses

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	Dual-in-line package
3	CQCC1-N28	28	Square chip carrier package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range (V_{IN})	-0.5 V dc to V_{CC} +0.5 V dc
Output voltage range (V_{OUT})	-0.5V dc to V_{CC} +0.5 V dc
Continuous output current (I_{OUT})	±25 mA
Input clamp current (I_{IK})	±20 mA
Output clamp current (I_{OK})	±20 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D): 2/	193 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Input voltage range (V_{IN})	0 to V_{CC}
Output voltage range (V_{OUT})	0 to V_{CC}
High level input voltage (V_{IH})	2 V minimum
Low level input voltage (V_{IL})	0.8 V maximum
High level output current (I_{OH}):	
TDO, DTDO1-4, MCO	-8.5 mA
DTMS1-4, DCO (3-state), DTCK	-13.6 mA
Low level output current (I_{OL}):	
TDO, DTDO1-4, MCO	8.5 mA
DCO, (open drain or 3-state)	13.6 mA
DTMS1-4	20.4 mA
DTCK	40.8 mA
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	3/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Maximum power dissipation is defined as V_{CC} x I_{CC} + V_{OL} X I_{OL} X # of outputs and must withstand the added P_D due to the short circuit output test (e.g., I_{OS}).
3/ Values will be added when they become available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non Government publications. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies shouldbe addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational sevices.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 3.

3.2.5 Boundary Scan Instruction Codes. For device 01 the boundary scan instruction codes shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} = 0.8 V I_{OH} = -7 mA	TDO,DTDO 1-4, MCO	1, 2, 3	3.6		V
	V_{OH}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} = 0.8 V I_{OH} = -11 mA	DTMS1-4, DCO (3-state), DTCK	1, 2, 3	3.6		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} = 0.8 V I_{OL} = 7 mA	TDO, DTDO1-4. MCO	1, 2, 3		0.5	V
	V_{OL}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} = 0.8 V I_{OL} = 11 mA	DCO (open drain or 3-state)	1, 2, 3		0.5	V
	V_{OL}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} = 0.8 V I_{OL} = 16 mA	DTMS1-4	1, 2, 3		0.5	V
	V_{OL}	V_{CC} = 4.5 V V_{IH} = 2.0 V V_{IL} - 0.8 V I_{OL} = 32 mA	DTCK	1, 2, 3		0.5	V
Output leakage current	I_{OZ} 2/	V_{CC} = 5.5 V V_{OUT} = V_{CC} or GND	DTDO1-4, DTMS1-4, DCO, DTCK	1, 2, 3		±10	µA
High level output current	I_{OH}	V_{CC} = 5.5 V V_{OUT} = V_{CC}	DCO (open drain)	1, 2, 3		20	
Input current at maximum input voltage	I_I	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND	MCI, DCI, TCK, 1D1-4	1, 2, 3		±1	µA
	I_I	V_{CC} = 5.5 V V_{IN} = V_{CC}	TDI, DTDI1-4, TMS, TRST	1, 2, 3		±1	µA
		V_{CC} = 5.5 V V_{IN} = GND	TDI, DTDI1-4, TMS, TRST		-0.1	-20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified 1/	Group A subgroups	Limits		Unit
				Min	Max	
Power supply current	I_{CC}	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND I_{OUT} = 0 V	1, 2, 3		100	µA
Quiescent supply current delta	ΔI_{CC}	V_{CC} = 5.5 V One input at V_{IN} = 3.4 V Other inputs at V_{CC} or GND	1, 2, 3		1	mA
Input capacitance	C_{IN}	See 4.4.1c	4		5.5	pF
Functional tests		See 4.4.1b V_{CC} = 4.5 V and 5.5 V	7, 8			
TCK Frequency	f_{max}	V_{CC} = 4.5 V	9, 10, 11	20		MHz
DCI (count mode)				20		
Propagation delay TCK ↓ to DTCK	t_{PLH}	V_{CC} = 4.5 V R_L = 500Ω C_L = 50 pF	9, 10 ,11	2	14	ns
	t_{PHL}		9, 10, 11	2	16	
Propagation delay TCK ↓ to TDO	t_{PLH}		9, 10, 11	7.0	28	ns
	t_{PHL}		9, 10, 11	7.0	26	ns
Propagation delay TCK ↓ to Any DTDO	t_{PLH}		9, 10, 11	7.0	27	ns
	t_{PHL}		9, 10, 11	7.0	26	ns
Propagation delay TCK ↓ to DCO (open drain)	t_{PLH}		9, 10, 11	9.0	33	ns
Propagation delay TCK ↓ DCO (3-state)			9, 10, 11	9.0	32	
Propagation delay TCK ↓ to DCO (open drain)	t_{PHL}		9, 10, 11	9.0	34	
Propagation delay TCK ↓ DCO (3-state)			9, 10, 11	9.0	31	

See footnotes at end of table.

TABLE I. Electrical performance characteristics. continued

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ Unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay TMS to Any DTMS	t_{PLH}	V_{CC} = 4.5 V R_L = 500Ω C_L = 50 pF	9, 10, 11	4.0	21	ns
	t_{PHL}		9, 10, 11	5.0	23	
Propagation delay MCI to MCO	t_{PLH}		9, 10, 11	5.0	23	ns
	t_{PHL}		9, 10, 11	5.0	22	
Propagation delay DCI to DCO (open drain)	t_{PLH}		9, 10, 11	9	30	ns
Propagation delay DCI to DCO (3-state)			9, 10, 11	6	29	
Propagation delay DCI to DCO (open drain)	t_{PHL}		9, 10, 11	7	29	
Propagation delay DCI to DCO (3-state)			9, 10, 11	6	26	
Propagation delay TCK ↓ to Any DTMS	t_{PLH}		9, 10, 11	9	31	
	t_{PHL}		9, 10, 11	9	31	
Output disable time, TCK ↓ to TDO	t_{PHZ}		9, 10, 11	3	17	
	t_{PLZ}		9, 10, 11	3	16	
Output disable time, TCK ↓ to Any DTMS	t_{PHZ}		9, 10, 11	6	23	
	t_{PLZ}		9, 10, 11	6	28	
Output disable time, TCK ↓ to DCO	t_{PHZ}		9, 10, 11	6	23	
	t_{PLZ}		9, 10, 11	6	24	
Output disable time, TCK ↓ to Any DTDO	t_{PHZ}		9, 10, 11	5	19	
	t_{PLZ}		9, 10, 11	5	20	
Output enable time, TCK ↓ to TDO	t_{PZH}		9, 10, 11	8	30	
	t_{PZL}		9, 10, 11	8	31	
Output enable time, TCK ↓ to Any DTDO	t_{PZH}		9, 10, 11	9	31	
	t_{PZL}		9, 10, 11	9	33	

See footnotes at end of table.

TABLE I. Electrical performance characteristics. continued

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ Unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
Output enable time, TCK ↓ Any DTMS	t_{PZH}	V_{CC} = 4.5 V R_L = 500Ω C_L = 50 pF	9, 10, 11	8	31	ns
	t_{PZL}		9, 10, 11	10	35	
Output enable time, TCK ↓ to DCO	t_{PZH}		9, 10, 11	9	37	
	t_{PZL}		9, 10, 11	8	35	
TCK high or low	t_w (Pulse duration)		9, 10, 11	12		
DCI high or low (count mode)			9, 10, 11	7		
$\overline{TRST}$ low			9, 10, 11	7		
TMS before TCK ↑	t_{su} (Setup time)		9, 10, 11	8		ns
TDI before TCK ↑			9, 10, 11	9		
Any DTDI before TCK ↑			9, 10, 11	7		
MCI before TCK ↑			9, 10, 11	3		
DCI before TCK ↑			9, 10, 11	3		
Any ID before TCK ↑			9, 10, 11	2		
TMS after TCK ↑	t_h (Hold time)		9, 10, 11	2		
TDI after TCK ↑			9, 10, 11	2		
Any DTDI after TCK ↑			9, 10, 11	2		
MCI after TCK ↑			9, 10, 11	4		
DCI after TCK ↑			9, 10, 11	4		
Any ID after TCK ↑			9, 10, 11	4		
Delay time, power up to TCK ↑	t_d 3/		9, 10, 11	100		

1/ All test to be performed using worst case condition. Unless otherwise specified.

2/ For I/O pins, the parameter I_{OZ} includes the open drain output leakage current.

3/ Guaranteed, but not tested.

Device type	01	
Case outline	3	X
Terminal number	Terminal symbol	
1	ID4	DCO
2	ID3	MCO
3	ID2	DTDO1
4	$\overline{ID1}$	DTDO2
5	TRST	DTDO3
6	MCI	DTDO4
7	DCI	GND
8	DCO	DTMS1
9	MCO	DTMS2
10	DTDO1	DTMS3
11	DTDO2	DTMS4
12	DTDO3	DTK
13	DTDO4	TDO
14	GND	TMS
15	DTMS1	TCK
16	DTMS2	TDI
17	DTMS3	DTDI4
18	DTMS4	DTDI3
19	DTCK	DTDI2
20	TDO	DTDI1
21	TMS	V_{CC}
22	TCK	ID4
23	TDI	ID3
24	DTDI4	ID2
25	DTDI3	$\overline{ID1}$
26	DTDI2	TRST
27	DTDI1	MCI
28	V_{CC}	DCI

FIGURE 1. Terminal connections.

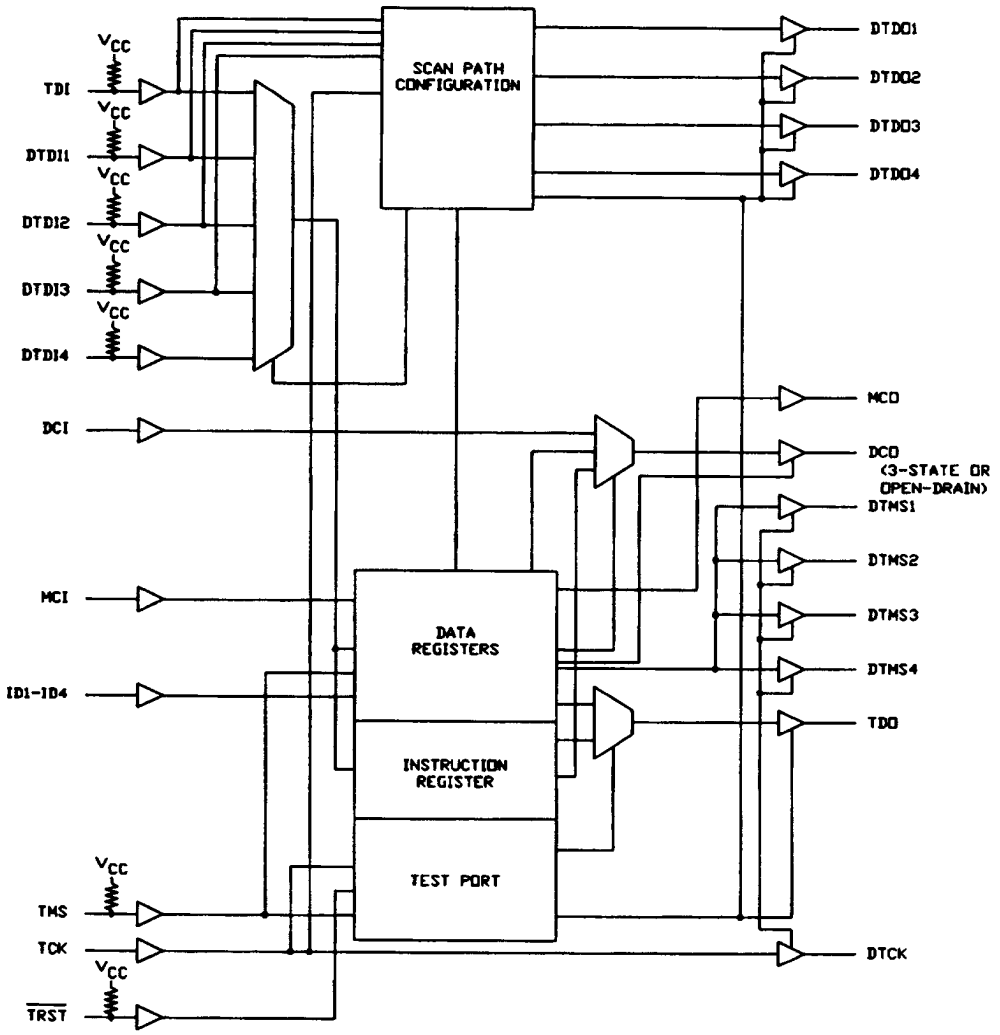
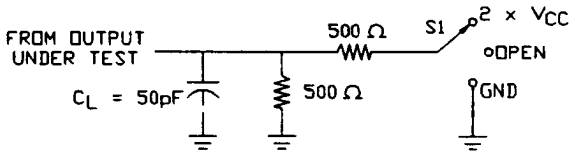
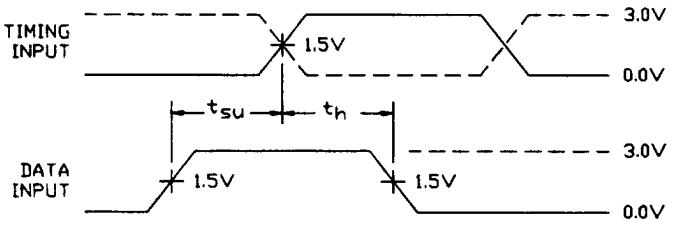


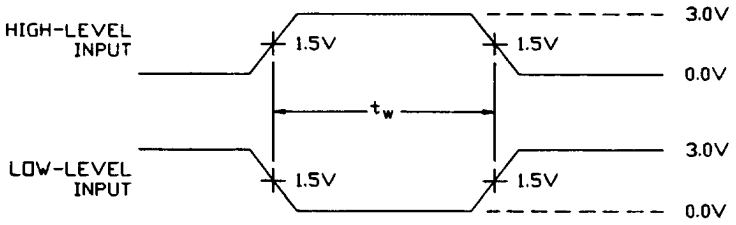
FIGURE 2. Logic diagram.



LOAD CIRCUIT FOR 3-STATE OUTPUTS



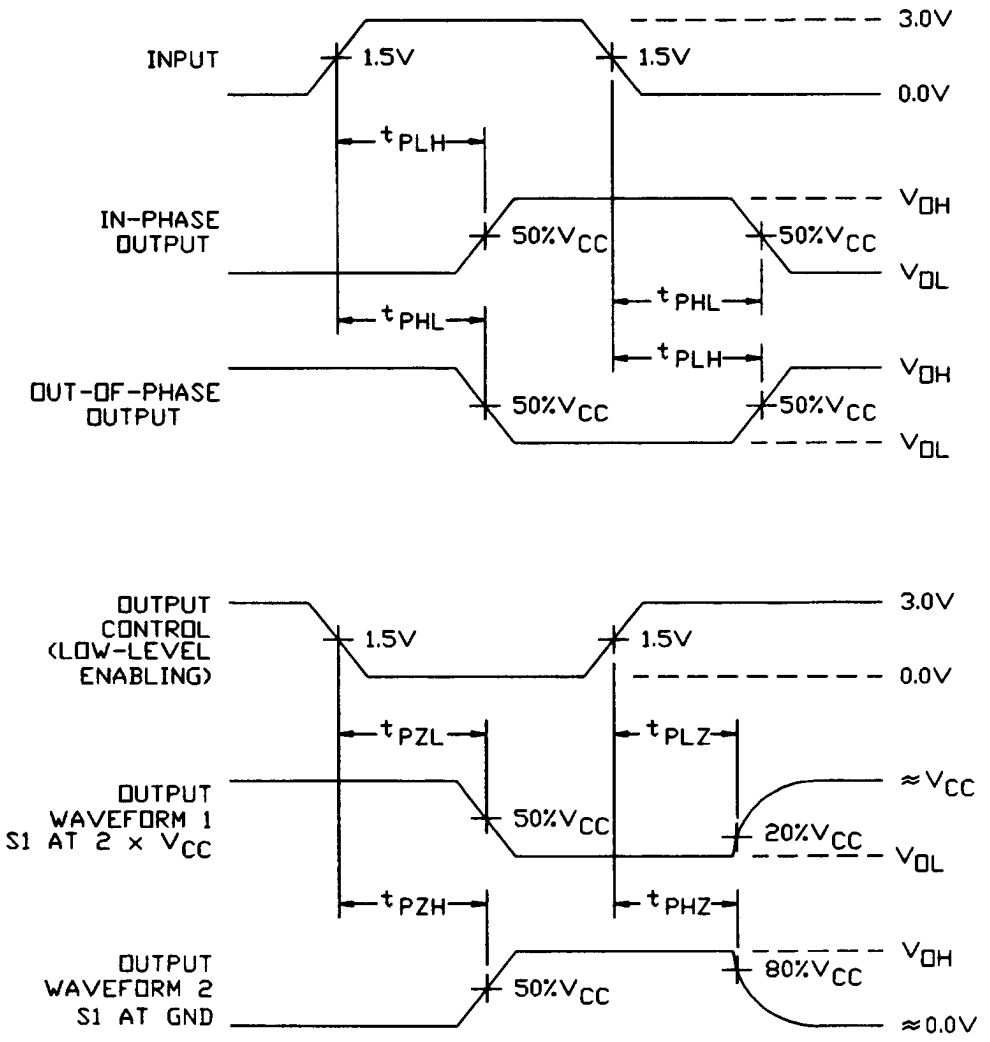
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 X V_{CC}
t_{PHZ}/t_{PZH}	GND

FIGURE 3. Test circuit and switching waveforms.



NOTES:
1. Pulse generator characteristics:
   PRR = ≤ 10 MHz, Z_{OUT} = 50Ω, t_r = t_f = 3.0 ns duty cycle = 50 percent.
2. C_L = 50 pF.
3. R_L = 500Ω.
4. C_L includes probe and jig capacitance.

FIGURE 3. Test circuit and switching waveforms - Continued.

BINARY CODE BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER
00000000	EXTEST	Boundary scan	Boundary scan
10000001	BYPASS 1/	Bypass scan	Bypass
10000010	SAMPLE/RELOAD	Sample boundary	Boundary scan
00000011	INTEST	Boundary scan	Boundary scan
10000100	BYPASS 1/	Bypass scan	Bypass
00000101	BYPASS 1/	Bypass scan	Bypass
00000110	BYPASS 1/	Bypass scan	Bypass
10000111	BYPASS 1/	Bypass scan	Bypass
10001000	COUNT	Count	Counter
00001001	COUNT	Count	Counter
00001010	BYPASS 1/	Bypass scan	Bypass
10001011	BYPASS 1/	Bypass scan	Bypass
00001100	BYPASS 1/	Bypass scan	Bypass
10001101	BYPASS	Bypass scan	Bypass
10001110	SCANCN	Control register scan	Control
00001111	SCANCT	Control register scan	Control
11111010	SCANCNT	Counter scan	Counter
01111011	READCNT	Counter read	Counter
11111100	SCANIDB	ID bus register scan	ID bus
01111101	READIDB	ID bus register read	ID bus
01111110	SCANSEL	Select register scan	Select
All others	BYPASS	Bypass scan	Bypass

1/ A SCOPE opcode exists but is not supported by the 01 device.

FIGURE 4. Boundary scan instruction codes.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

3.11 IEEE 1149.1 compliance. Device type 01 shall be compliant with IEEE 1149.1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except that interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.
b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero reject shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,7 8,9,10,11 1/	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7, 8,9,10,11	1,2,3,4,7 8,9,10,11	1,2,3,4,7, 8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,	1,2,3,	1,2,3,
Group D end-point electrical parameters (see 4.4)	1,2,3,	1,2,3,	1,2,3,
Group E end-point electrical parameters (see 4.4)		1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-8525.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and table III.

6.5.1 Table III. Pin descriptions.

TDI-TEST DATA IN. One of the four pins required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or data registers. TDI is typically driven by the TDO pin of the primary bus controller (PBC). An internal pullup forces TDI to a high level if it is left unconnected.

TDO-TEST DATA OUT. One of the four pins required by IEEE Standard 1149.1. TDO is the serial output for shifting information out of the instruction register or data registers. TDO is typically connected to the TDI pin of the next testable device in the primary scan path.

TCK-TEST CLOCK. One of the four pins required by IEEE Standard 1149.1. All operations of the ACT8997, except for the count function, are synchronous to TCK. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.

TMS-TEST MODE SELECT. One of the four pins required by IEEE Standard 1149.1. The level of TMS at the rising edge of TCK directs the ACT8997 through its states. An internal pullup forces TMS to a high level if it is left unconnected.

$\overline{\text{TRST}}$-TEST RESET. This active-low pin implements the optional reset function of IEEE Standard 1149.1. When asserted, TRST causes the ACT8997 to go to the Test Logic Reset state and configure the instruction register and data registers to their power-up values. An internal pullup forces $\overline{\text{TRST}}$ to a high level if it is left unconnected.

DTMS1-DTMS4-DEVICE TEST MODE SELECT 1-4. Any combination of these four pins can be selected to follow the TMS pin to direct the secondary scan path(s) through the states in figure 1. The unselected DTMS pins can be independently set to a high or low logic level. The TMS circuit monitors input from the control register to determine the configuration of the DTMS pins.

MCI-MASTER CONDITION INPUT. This pin receives interrupt and protocol signals from a PBC. The level on MCI is buffered and output on MCO.

MCO-MASTER CONDITION OUTPUT. This pin transmits interrupt and protocol signals to the secondary scan path(s).

DCI-DEVICE CONDITION INPUT. This pin receives interrupt and protocol signals from the secondary scan path(s). When the counter register is instructed to count up or down, the DCI is configured as the counter clock.

DCO-DEVICE CONDITION OUTPUT. DCO is configured by the control register to output protocol and interrupt signals and may be configured by the control register to output an error signal if the instruction register is loaded with an invalid value. DCO is further configured by the control register as:

1. Active high or low (reset condition = active low).

2. Open drain or 3-state (reset condition = open drain).

DTDI1-DTDI4-DEVICE TEST DATA IN 1-4. These pins receive the serial test data outputs of the selected secondary scan path(s). An internal pullup forces DTDI1-DTDI4 to a high logic level if it is left unconnected.

DTDO1-DTDO4-DEVICE TEST DATA OUT 1-4. These pins output serial test data to the TDI input(s) of the secondary scan path(s).

DTCK-DEVICE TEST CLOCK. This outputs the buffered test clock TCK to the secondary scan path(s).

ID1-ID4-IDENTIFICATION 1-4. This 4-bit data bus can be hardwired to provide identification of the subsystem under test. The value present on the bus can be scanned out through the boundary scan or ID bus registers.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.