MOTOROLA

Military 54F112

MPO

Advance Information

Dual J-K Negative Edge-Triggered Flip-Flop

ELECTRICALLY TESTED PER:
MIL-M-38510/34103

The 54F112 consists of two high-speed, completely independent JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the Clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S_D}$ or $\overline{C_D}$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S_D}$ and $\overline{C_D}$ force both Q and $\overline{Q}$ HIGH.

Asynchronous Inputs:
LOW Input to $\overline{S_D}$ sets Q to HIGH level
LOW Input to $\overline{C_D}$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C_D}$ and $\overline{S_D}$ makes both Q and $\overline{Q}$ HIGH

AVAILABLE AS:

1) JAN: *
2) SMD: *
3) 883C: 54F112/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2
*Call Factory for latest update

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{CP1}$	1	1	2	V_{CC}
K1	2	2	3	V_{CC}
J1	3	3	4	V_{CC}
$\overline{SD1}$	4	4	5	GND
Q1	5	5	7	OPEN
$\overline{Q1}$	6	6	8	OPEN
$\overline{Q2}$	7	7	9	OPEN
GND	8	8	10	GND
Q2	9	9	12	OPEN
$\overline{SD2}$	10	10	13	GND
J2	11	11	14	V_{CC}
K2	12	12	15	V_{CC}
$\overline{CP2}$	13	13	17	V_{CC}
$\overline{CD2}$	14	14	18	GND
$\overline{CD1}$	15	15	19	GND
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

AC TEST CIRCUIT

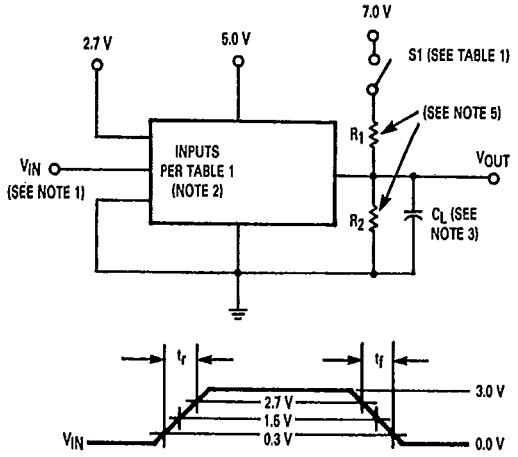

Table 1

Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

NOTES:
1. V_{IN} = Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz.
2. Terminal conditions (pins not designated may be high $\geq$ 2.0 V, low $\leq$ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = R_2$ = 499 Ω ± 5.0%.
6. When testing f_{MAX}, the output frequency shall be 1/2 the input frequency.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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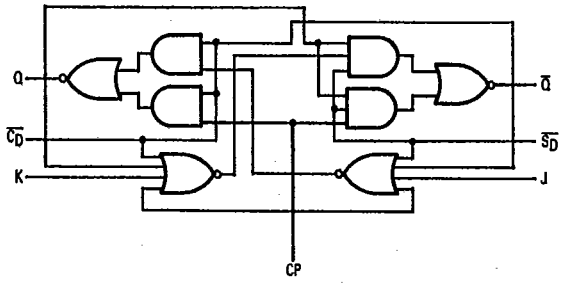
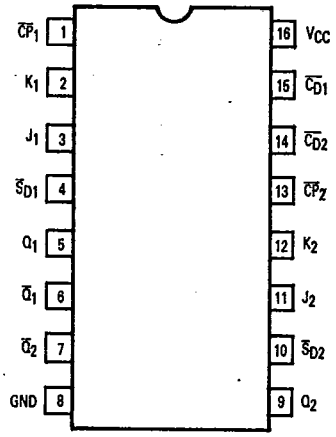
LOGIC DIAGRAM
(one half show)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

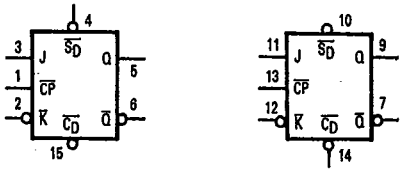
CONNECTION DIAGRAM



TRUTH TABLE		
Inputs		Outputs
@ t_n		@ t_n+1
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	Qn

t_n = Bit time before clock pulse
t_n+1 = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



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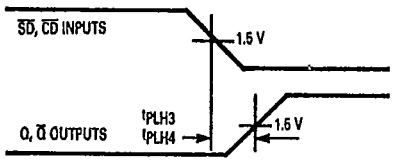
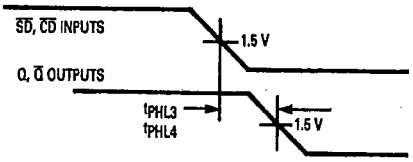
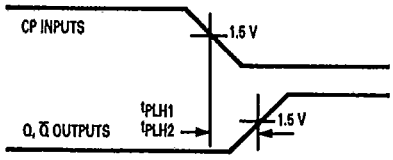
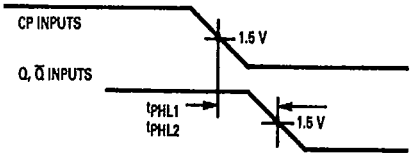
WAVEFORMS









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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IN} = 2.0 V, other inputs = 0.8 V, CP = (See Note 1).
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V, other inputs = 4.5 V or 2.0 V, CP = (See Note 1).
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, J = 4.5 V, other inputs = GND, 4.5 V, (2.7 V) or (See Note 1).
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, J = 4.5 V, other inputs = GND, 4.5 V, (7.0 V) or (See Note 1).
I_{IL}	Logical "0" Input Current K and J	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, other inputs = 4.5 V, SD1 & CD1 = 4.5 V or (See Note 1).
I_{IL}	Logical "0" Input Current $\overline{CD}$1 and 2, $\overline{SD}$1 and 2	−0.09	−1.8	−0.09	−1.8	−0.09	−1.8	mA	V_{CC} = 5.5 V, $V_{IN(CP)}$ = 0.5 V, other inputs = 4.5 V, CDn = (See Note 1).
I_{IL}	Logical "0" Input Current $\overline{CP}$1 and 2	−0.12	−2.4	−0.12	−2.4	−0.12	−2.4	mA	V_{CC} = 5.5 V, $\overline{CD}$ = 0.5 V, $\overline{SD}$ = 0 V, other inputs = 4.5 V.
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 4.5 V, V_{IN} = 5.5 V, $\overline{SD}$ = 0 V or 5.5 V, V_{OUT} = 2.5 V.
I_{OS}	Short Circuit Output Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, $\overline{SD}$ = GND, V_{OUT} = 0 V.
I_{CC}	Power Supply Current		19		19		19	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, $\overline{SD}$ = GND or 4.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (Repeat at) V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

NOTE:
1. Apply all voltages, then apply 3.0 V, 0 V, 3.0 V to $\overline{CDX}$, or $\overline{SDX}$ (as required) then make measurement.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output CP to Q	3.3	7.7	2.5	9.5	2.5	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 5.0%.
t_{PLH1}	Propagation Delay /Data-Output CP to Q	3.3	7.7	2.5	9.5	2.5	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 5.0%.
t_{PHL2}	Propagation Delay /Data-Output CP to $\overline{Q}$	3.3	7.7	2.5	9.5	2.5	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 5.0%.
t_{PLH2}	Propagation Delay /Data-Output CP to $\overline{Q}$	3.3	7.7	2.5	9.5	2.5	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 5.0%.
t_{PHL3}	Propagation Delay /Data-Output $\overline{CD}$ or $\overline{SD}$ to Q or $\overline{Q}$	3.3	7.7	2.0	9.5	2.0	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 5.0%.
t_{PLH3}	Propagation Delay /Data-Output $\overline{CD}$ or $\overline{SD}$ to Q or $\overline{Q}$	3.0	7.0	2.0	9.0	2.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 5.0%.
t_{PHL4}	Propagation Delay /Data-Output $\overline{CD}$ or $\overline{SD}$ to Q or $\overline{Q}$	3.3	7.7	2.5	9.5	2.5	9.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 5.0%.
t_{PLH4}	Propagation Delay /Data-Output $\overline{CD}$ or $\overline{SD}$ to Q or $\overline{Q}$	3.0	7.0	2.0	9.0	2.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 5.0%.
f_{MAX}	Maximum Clock Frequency	90		90		90		MHz	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω ± 5.0%.

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