National Semiconductor

September 1991

54ACT/74ACT2725
512 x 9 First-In, First-Out Memory (FIFO)

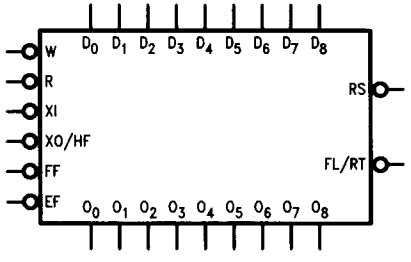
General Description

The 512 x 9 FIFO is a first-in, first-out dual port memory capable of asynchronous, simultaneous read and write. Other important features are: expansion capability in both the word depth and bit width, half-full flag capability in the single device mode, empty and full warning flags, ring pointers for fall-through time; it is suited for high-speed applications.

Features

- First-in, first-out dual port memory
- 512 x 9 organization
- Low power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by word depth and/or bit width
- Half-full flag capability in single device mode
- Empty and full warning flags
- Auto retransmit capability
- Outputs source/sink 8 mA
- 'ACT2725 has TTL-compatible inputs
- Pin and functionality compatible with IDT7201A

Logic Symbol



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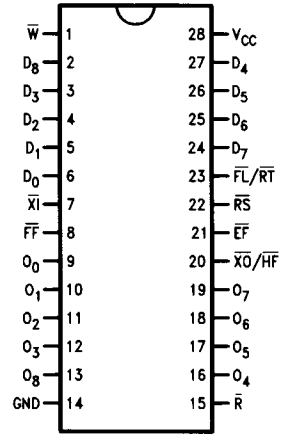
Connection Diagram

Pin Assignment for DIP, Flatpak and SOIC



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Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{XI}$	Expansion In
$\overline{XO}/\overline{HF}$	Expansion Out, Half-Full Flag
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag
$\overline{RS}$	Reset
$\overline{FL}/\overline{RT}$	First Load/Retransmit

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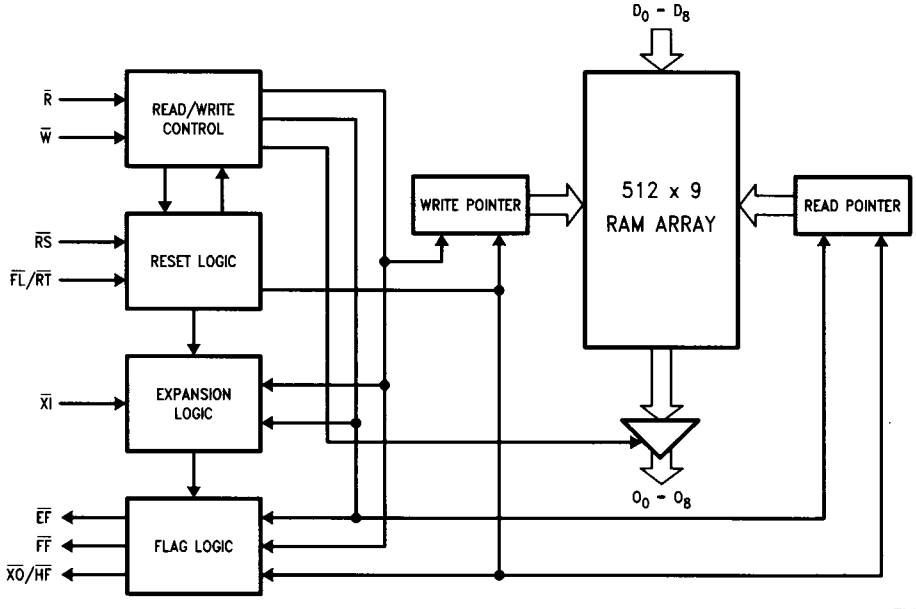
Logic Diagram

'ACT2725 Block Diagram



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Functional Description

INPUTS

Data Inputs (D0–D8)

Data Inputs for 9-bit wide data are TTL-compatible. Word width can be reduced by tying unused inputs to ground and leaving corresponding outputs open.

Reset ($\overline{RS}$)

The device is reset whenever the Reset ($\overline{RS}$) input is taken LOW. During reset, both the internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. During Reset, the Write Enable ($\overline{W}$) and Read Enable ($\overline{R}$) can be in any state. However, the Reset Recovery Time (t_{RSR}) must be met before the first write as shown in *Figure 1*. The Half-Full and Flags ($\overline{HF}$ and $\overline{FF}$) will be set to HIGH after reset. Empty Flag ($\overline{EF}$) will go LOW after reset.

Write Enable ($\overline{W}$)

The write cycle is initiated on the falling edge of the ($\overline{W}$) input provided the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is written to the FIFO by the write enable, independent of any ongoing read operation. After half of the memory is filled and on the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will go LOW and will remain LOW until the difference between the write pointer and the read pointer is less than or equal to one half the total memory of the device. The Half-Full Flag ($\overline{HF}$) then goes HIGH on the rising edge of the next read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations when the FIFO is full. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF} *(Figure 3)* allowing another valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in the Write Enable ($\overline{W}$) will not affect the FIFO during this state.

Read Enable ($\overline{R}$)

The read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. This signal reads the data available at the read pointer. When ($\overline{R}$) is LOW, data appears at the output and when ($\overline{R}$) is HIGH, the outputs are TRI-STATED. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the final read cycle but inhibiting further read operations. The data outputs will remain TRI-STATED. Upon the completion of a valid write operation, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} *(Figure 4)* allowing a valid read to begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in the Read Enable will not affect the FIFO in this state.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

The $\overline{FL}/\overline{RT}$ is a dual purpose input. In the Single Device Mode (SDM), the $\overline{FL}/\overline{RT}$ pin acts as a re-transmit input. Pulsing this input LOW in SDM resets the read pointer to the first data location and data can be re-read without affecting the write pointer. This feature is useful if less than 512 writes have been performed between resets. Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be HIGH during re-transmit. In Multiple Device Mode (MDM), the $\overline{FL}/\overline{RT}$ input is grounded to indicate that this is the first device in the FIFO chain, and is tied to V_{CC} for all other devices. *(Figure 11.)*

Expansion In ($\overline{XI}$)

The Expansion In pin acts as a dual purpose input. XI is grounded to indicate operation in SDM *(Figure 10)*. In MDM, XI is connected to Expansion Out ($\overline{XO}$) pin of the preceding device *(Figure 11)*.

OUTPUTS

Full Flag ($\overline{FF}$)

After the falling edge of the last write operation, the Full Flag will be set (LOW) indicating that all locations of the FIFO are full. If the Read Enable $\overline{R}$ is held HIGH from reset, the Full Flag ($\overline{FF}$) will go LOW on the falling edge of the 512th write. When the $\overline{FF}$ is LOW, all further writes are disabled. After the rising edge of the first read operation, the $\overline{FF}$ goes HIGH enabling further writes.

Empty Flag ($\overline{EF}$)

After the falling edge of the last read operation, the Empty Flag goes LOW disabling further reads and indicating that the device is empty. The Empty Flag goes HIGH after the rising edge of the first write operation. Assuming a full FIFO and holding write enable ($\overline{W}$) HIGH, the falling edge of the 512th Read will cause $\overline{EF}$ to go LOW. On Reset, the Empty Flag is forced LOW indicating that the FIFO is empty.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

The $\overline{XO}/\overline{HF}$ pin is a dual purpose output. In SDM, this pin acts as the Half-Full Flag ($\overline{HF}$). On Reset, this pin is HIGH. After half the memory is filled and on the falling edge of the next write operation, the output will go LOW and remain LOW until the difference between the write pointer and the read pointer is less than or equal to one half the total memory of the device. The Half-Full Flag goes HIGH after the rising edge of the next read.

In Multiple Device Expansion Mode, Expansion Out ($\overline{XO}$) is connected to Expansion In ($\overline{XI}$) input of the next device in the FIFO chain. When the last physical memory location is reached by either the read pointer or the write pointer, the $\overline{XO}$ provides a pulse to the Expansion In of the next device.

Data Outputs (O0–O8)

Data output bus is 9 bits wide. When $\overline{R}$ is LOW, the data outputs are enabled. When $\overline{R}$ is HIGH, the data outputs are TRI-STATED.

Functional Description (Continued)

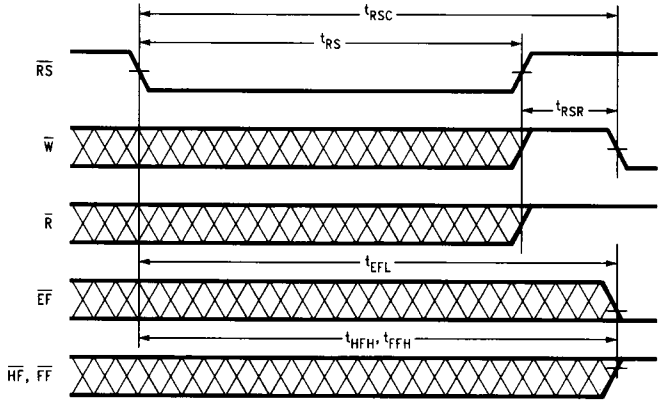

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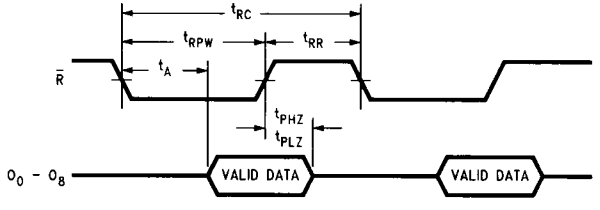
FIGURE 1. Reset



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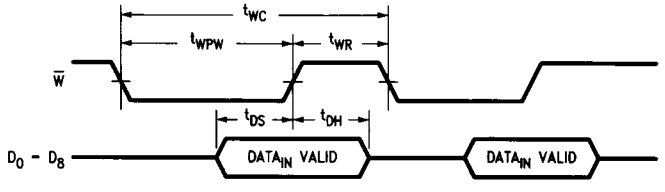

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FIGURE 2. Asynchronous Write and Read Operation

Functional Description (Continued)

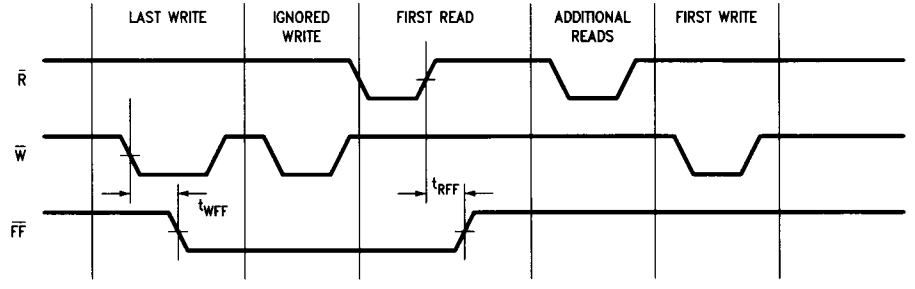

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FIGURE 3. Full Flag From Last Write to First Read

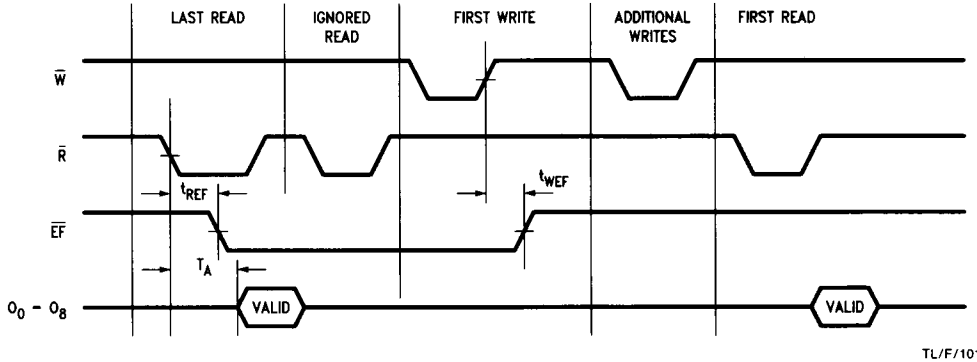

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FIGURE 4. Empty Flag From Last Read to First Write

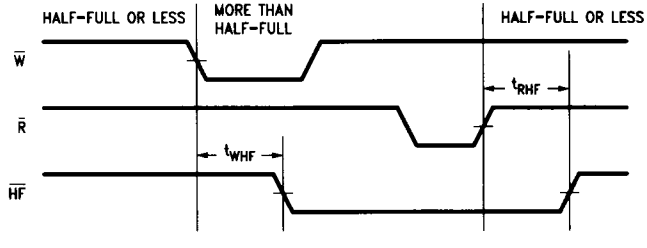

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FIGURE 5. Half-Full Flag Timing

Functional Description (Continued)

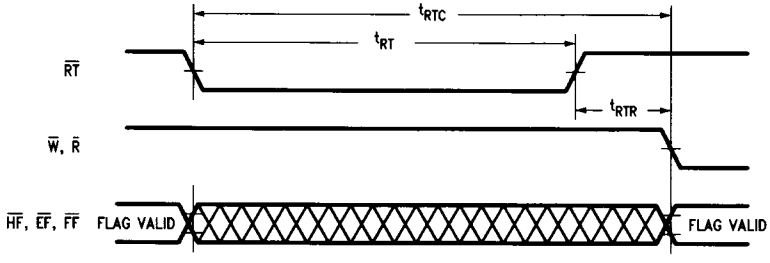

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FIGURE 6. Retransmit

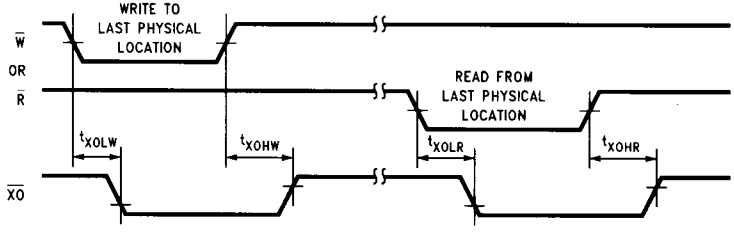

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FIGURE 7. Expansion Out

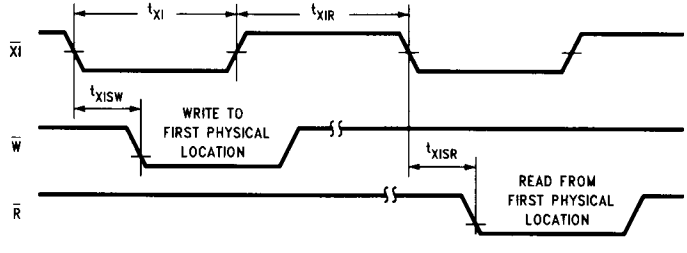

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FIGURE 8. Expansion In

Modes of Operation

Single Device Mode (SDM):

The 'ACT2725 may be used in a single device configuration when the application requires 512 words or less. In SDM, the Expansion In (XI) input is grounded *(Figure 9).*

Word Width Expansion

Word Width of the 'ACT2725 can be increased by connecting the corresponding control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{HF}$, and $\overline{FF}$) can be detected from any one device *(Figure 10).*

Multiple Device Mode (MDM):

Depth Expansion Mode

In applications requiring greater than 512 words, the 'ACT2725 may be expanded vertically as demonstrated in *Figure 11.* The '2725 operates in Depth Expansion Mode when the following conditions are met:

1. The first device in the FIFO chain must be identified by grounding the First Load ($\overline{FL}$) control input.
2. All other devices in the chain must hold $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

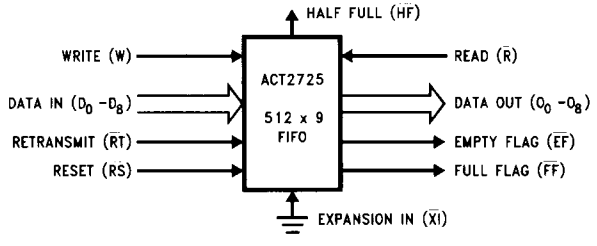

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FIGURE 9. Block Diagram of Single—512 x 9 FIFO

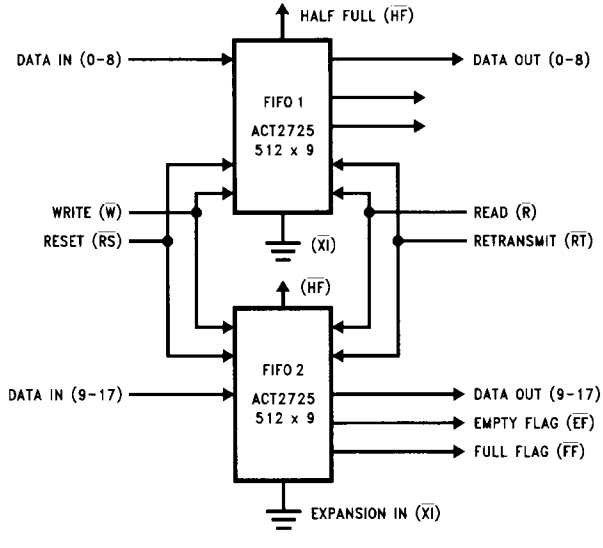

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FIGURE 10. Word Width Expansion—512 x 18 FIFO

Modes of Operation (Continued)

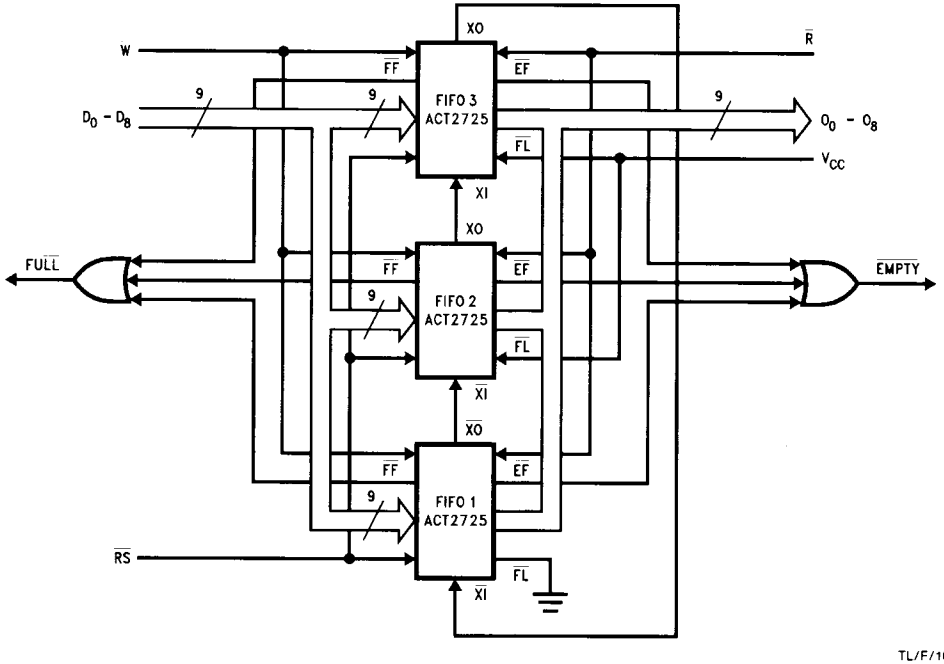

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FIGURE 11. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)

TABLE I

$\overline{FL}/\overline{RT}$	$\overline{XI}$	Operating Mode
0	0	SDM, Retransmit
0	1	MDM, First Device
1	0	SDM, Normal
1	1	MDM, Not First Device

SDM—Single Device Mode
MDM—Multiple Device Mode

Modes of Operation (Continued)

Compound Word Width and Depth Expansion Mode

The 'ACT2725 can be expanded in both horizontal Word Width and Vertical Depth directions to achieve large FIFO arrays. *(Figure 12).*

Data Flow-Through Mode

Two types of flow-through modes are permitted: a read flow-through mode and a write flow-through mode. Read flow-through mode permits the reading of a single word after writing one word of data into an empty FIFO. During the read flow-through mode, Read ($\overline{R}$) is brought LOW in anticipation of a data word being written in. The rising edge of the Write signal completes the write, and the Empty Flag ($\overline{EF}$) is temporarily set HIGH for a brief interval t_{REF}. Valid data is available on the bus t_{WZL}, t_{WZH} ns after the rising edge of the write signal ($\overline{W}$).

The $\overline{R}$ signal has to be held LOW for a time of t_{RPW} as referenced to the rising edge of $\overline{EF}$. The guarantees that the internal Read signals for reading the data and advancing the read pointer are generated correctly *(Figure 13).* During one cycle of read flow-through operation the Write ($\overline{W}$) line should be asserted only once as shown in *Figure 13.*

In the write flow-through mode, the 'ACT2725 permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The rising edge of the read ($\overline{R}$) line causes the Full Flag ($\overline{FF}$) to go HIGH but the write ($\overline{W}$), being LOW causes the $\overline{FF}$ to go LOW in anticipation of a new data word. On the rising edge of the write, the new word is loaded into the FIFO. The ($\overline{W}$) signal has to be low for a time of T_{WPW} after the rising edge of $\overline{FF}$. This guarantees that the internal write signals for writing data and advancing the write pointer are generated correctly *(Figure 14).* During one cycle of write flow-through operation the read ($\overline{R}$) line should be asserted once as shown in *Figure 14.*

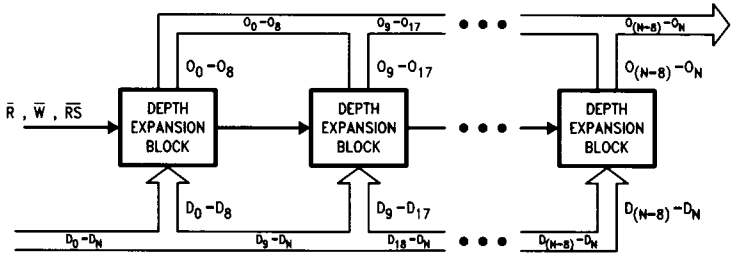

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FIGURE 12. Compound FIFO Expansion

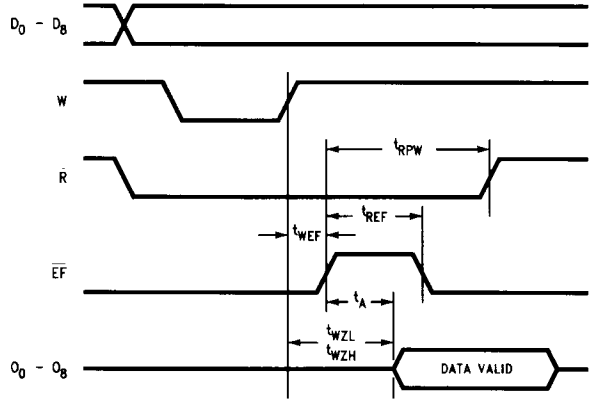

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FIGURE 13. One Cycle of Read Data Flow-Through Mode Operation

Modes of Operation (Continued)

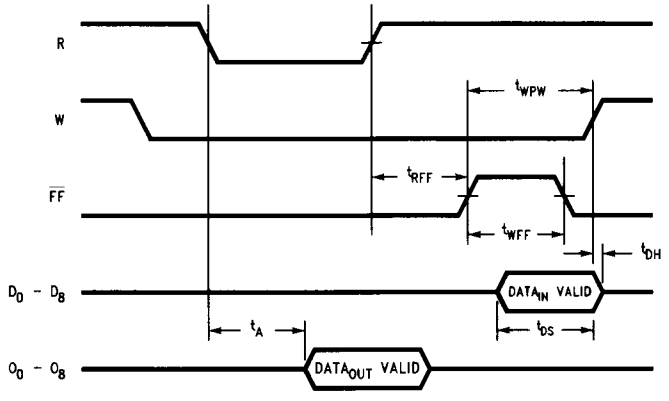

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FIGURE 14. One Cycle of Write Data Flow Through Mode Operation

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±32 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±32 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC}) (Unless Otherwise Specified)	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	0°C to +70°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics For 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = 0°C to +70°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −8 mA −8 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 8 mA 8 mA
I_{IN}	Maximum Input	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6	1.0	1.6	1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			32	32	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−32	−32	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

Note 1: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = 0°C$ to $+70°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PZH}	Data Access Time (TA)	5.0	9.5	20.0	24.0			8.5	26.5	ns	2, 4, 13, 14
t_{PZL}	Data Access Time (TA)	5.0	9.5	17.5	21.0			8.5	23.0	ns	2, 4, 13, 14
t_{PLZ}	Read Pulse High to Data Bus Disable	5.0	3.5	8.5	10.5			3.0	11.0	ns	2
t_{PHZ}	Read Pulse High to Data Bus Disable	5.0	4.0	10.0	12.0			3.5	13.0	ns	2
t_{WZL}	Write Pulse High to Data Low (Note 1)	5.0	16.5	32.0	37.5			15.5	42.0	ns	13
t_{WZH}	Write Pulse High to Data High (Note 1)	5.0	17.5	35.0	41.0			16.5	46.0	ns	13
t_{EFL}	Reset to Empty Flag Low	5.0	4.0	8.5	9.5			3.5	10.5	ns	1
t_{FFH}	Reset to Full Flag High	5.0	5.0	10.5	12.0			4.5	13.0	ns	1
t_{HFH}	Reset to Half Flag High	5.0	4.5	9.0	10.0			4.0	11.0	ns	1
t_{REF}	Read Low to Empty Flag Low	5.0	9.0	17.0	20.0			8.0	22.0	ns	4, 13
t_{RFF}	Read High to Full Flag High	5.0	6.5	11.5	13.5			5.5	15.0	ns	3, 14
t_{RHF}	Read High to Half Flag High	5.0	7.0	12.5	14.5			6.0	16.0	ns	5
t_{WEF}	Write High to Empty Flag High	5.0	8.0	14.0	19.5			7.0	22.0	ns	4, 13
t_{WFF}	Write Low to Full Flag Low	5.0	6.0	11.5	13.5			5.5	15.0	ns	3, 14
t_{WHF}	Write Low to Half Flag Low	5.0	7.0	13.0	14.5			6.0	16.0	ns	5
t_{XOLW}	Write Low to $\overline{XO}$ Low	5.0	6.0	12.5	14.0			5.5	15.5	ns	7
t_{XOHW}	Write High to $\overline{XO}$ High	5.0	7.5	13.5	15.5			6.5	17.5	ns	7
t_{XOLR}	Read Low to $\overline{XO}$ Low	5.0	6.0	12.5	14.0			5.5	15.5	ns	7
t_{XOHR}	Read High to $\overline{XO}$ High	5.0	7.5	13.5	15.5			6.5	17.5	ns	7

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Read flow through mode only.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = 0°C$ to $+70°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_{RC}	Read Cycle Time*1	5.0	20.0	22.0		25.0	ns	2
t_{RR}	Read Pulse Width High	5.0	5.0	6.0		7.0	ns	2
t_{RPW}	Read Pulse Width Low	5.0	15.0	16.0		18.0	ns	2, 13
t_{WC}	Write Cycle Time *2	5.0	20.0	22.0		25.0	ns	2
t_{WR}	Write Pulse Width High	5.0	5.0	6.0		7.0	ns	2
t_{WPW}	Write Pulse Width Low	5.0	15.0	16.0		18.0	ns	2, 14

*Voltage Range 5.0 is 5.0V ±0.5V

*1 = This parameter not measured, guaranteed by design = $T_{RPW} + T_{RR}$

*2 = This parameter not measured, guaranteed by design = $T_{WPW} + T_{WR}$

AC Operating Requirements (Continued)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = 0°C$ to $+70°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_{DS}	Data Set-Up Time	5.0	2.5	5.5		6.0	ns	2, 14
t_{DH}	Data Hold Time HIGH	5.0	0.0	0.0		0.0	ns	2, 14
t_{RSC}	Reset Cycle Time *3	5.0	4.0	5.0		5.5	ns	1
t_{RS}	Reset Pulse Width Low	5.0	3.0	4.0		4.5	ns	1
t_{RSR}	Reset Recovery Time	5.0	1.0	1.0		1.0	ns	1
t_{RTC}	Retransmit Cycle Time *4	5.0	4.0	5.0		5.5	ns	6
t_{RT}	Retransmit Pulse Width	5.0	3.0	4.0		4.5	ns	6
t_{RTR}	Retransmit Recovery Time	5.0	1.0	1.0		1.0	ns	6
t_{XI}	$\overline{XI}$ Pulse Width (Note 2)	5.0	15.0	16.0		18.0	ns	8
t_{XIR}	$\overline{XI}$ Recovery Time (Note 2)	5.0	3.0	4.0		4.5	ns	8
t_{XISW}	$\overline{XI}$ to Write Set-Up Time (Note 2)	5.0	7.0	9.0		10.0	ns	8
t_{XISR}	$\overline{XI}$ to Read Set-Up Time (Note 2)	5.0	7.0	9.0		10.0	ns	8

*Voltage Range 5.0 is 5.0V ±0.5V

*3 = This parameter not measured, guaranteed by design = $T_{RS} + T_{RSR}$

*4 = This parameter not measured, guaranteed by design = $T_{RT} + T_{RTR}$.

Note 2: Valid in expansion mode only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

74ACT 2725 P C QR

Temperature Range Family
- 74ACT = Commercial TTL-Compatible
- 54ACT = Military TTL-Compatible

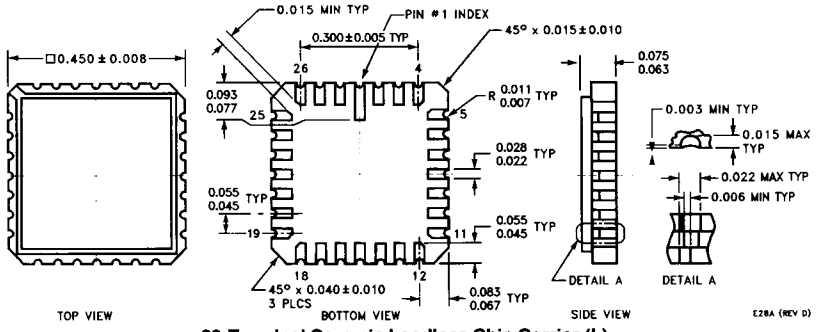
Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- L = Leadless Ceramic Chip Carrier (LCC)
- S = Small Outline (SOIC)
- Q = Plastic Chip Carrier (PCC)

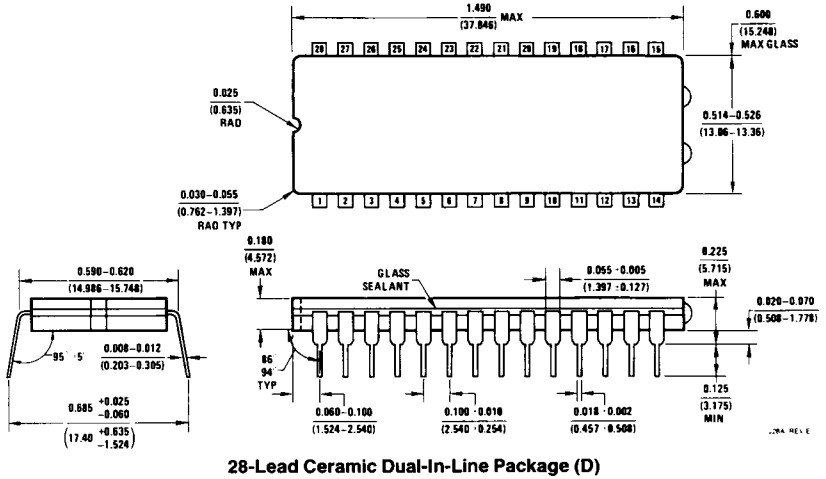
Temperature Range
- C = Commercial (−40°C to +85°C)
- M = Military (−55°C to +125°C)

Special Variations
- QR = Commercial grade device with burn-in
- QB = Military grade device with environmental and burn-in processing shipped in tubes

Physical Dimensions inches (millimeters)



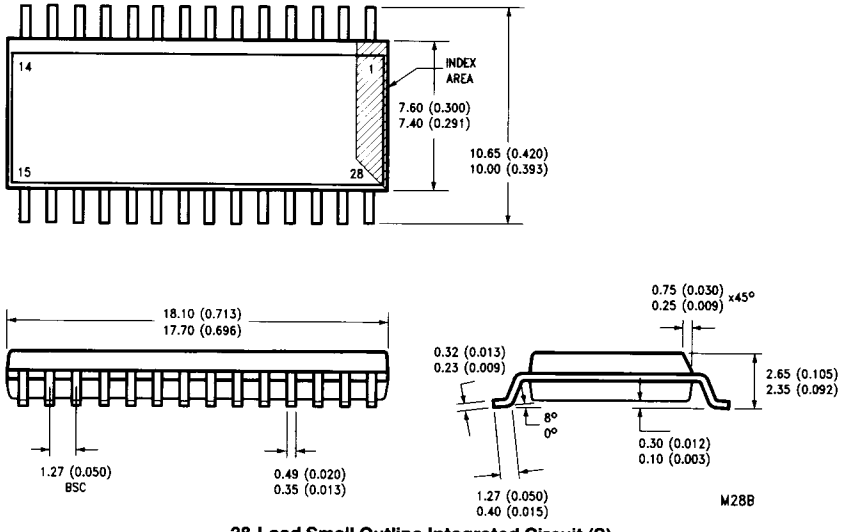
28-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



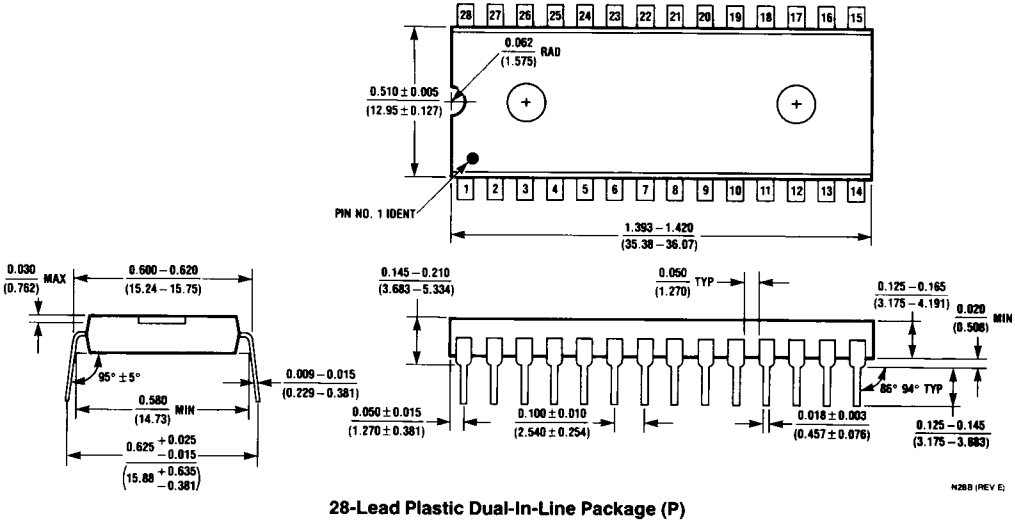
28-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J28A

Note: FACT Product Shipped WITHOUT Protective Silicon "Bumpers"

Physical Dimensions inches (millimeters) (Continued)

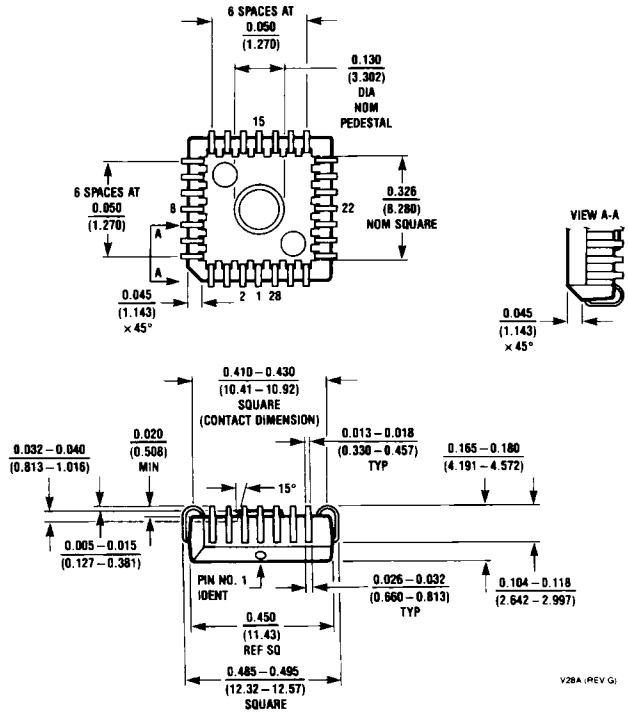


28-Lead Small Outline Integrated Circuit (S)
NS Package Number M28B



28-Lead Plastic Dual-In-Line Package (P)
NS Package Number N28B

Physical Dimensions inches (millimeters) (Continued)



28-Lead Plastic Chip Carrier (Q)
NS Package Number V28A

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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