SONET STS-1 Framer MegaCore Function (STS1FRM)

June 2001; ver. 1.01 Data Sheet

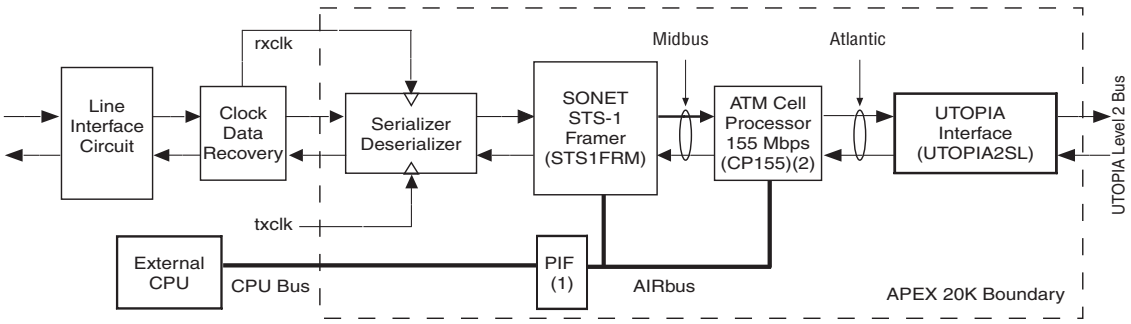
Features

- Performs synchronous optical network (SONET) framing and transmission convergence (TC)
- Processes transport overhead (TOH) and path overhead (POH)
- Supports a data rate of up to 51.84 Megabits per second (Mbps)
- Easy-to-use MegaWizard® Plug-In generates MegaCore® variants
- Quartus® II software and OpenCore® feature allow place-and-route, and static timing analysis of designs prior to licensing
- Secure register transfer level (RTL) simulation models allow simulation with user design in third-party simulators
- Optimized for the Altera® APEX™ 20KE device architecture

Typical Applications

Figure 1 shows the STS1FRM interfacing with two other Altera MegaCore variants to achieve ATM transport over SONET.

Figure 1. Typical Application



Notes:
(1) PIF—Processor interface block
(2) The CP155 runs at 51.84 MHz.

Other possible applications include:

- ATM switches
- Digital cross-connection (DCC) systems
- Routers
- Multiplexers

The STS1FRM complies with all applicable standards, including:

- American National Standards Institute (ANSI), *Synchronous Optical Network (SONET) –Basic Description including Multiplex Structure, Rates, and Formats, ANSI T1-105*–1995.
- American National Standards Institute (ANSI), *Synchronous Optical Network (SONET) –Payload Mappings, ANSI T1-105.02*–1995.
- Telcordia, *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria, GR-253-CORE,* Issue 3, September 2000.
- Telcordia, *Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria Issue List Report, GR-253-ILR,* Issue 3A, October 2000.

Functional Description

The STS1FRM operates in full-duplex mode, and comprises four blocks, as illustrated in Figure 2.

The following list of functions is based on a full-feature STS1FRM. See Table 2 for all possible options.

- Transport overhead receiver (RXTOH)
  - Inputs raw SONET data
  - Descrambles the data
  - Performs frame alignment
  - Performs error checking
  - Maintains counters and buffers
  - Captures the TOH bytes for processing by software, and parameterized hardware extraction
- Path overhead receiver (RXPOH_0)
  - Processes the pointer
  - Performs error checking
  - Maintains counters and buffers
  - Captures the POH bytes for processing by software, and parameterized hardware extraction
  - Outputs payload data
- Transport overhead transmitter (TXTOH)
  - Generates the pointer (normal, positive stuff, negative stuff, or new data flag (NDF) selected by software)
  - Allows the flexible insertion of the TOH by software, or by parameterized hardware
  - Generates parity bytes
  - Maintains counters and buffers
  - Scrambles the data
  - Outputs raw SONET data

- Path overhead transmitter (TXPOH_0)
  - Inputs payload data
  - Allows the flexible insertion of the POH by software, or by parameterized hardware
  - Generates parity bytes
  - Maintains counters and buffers

Interfaces & Protocols

Two interfaces support the STS1FRM: the middle interface (Midbus), and the access to internal registers (AIRbus) interface.

Midbus

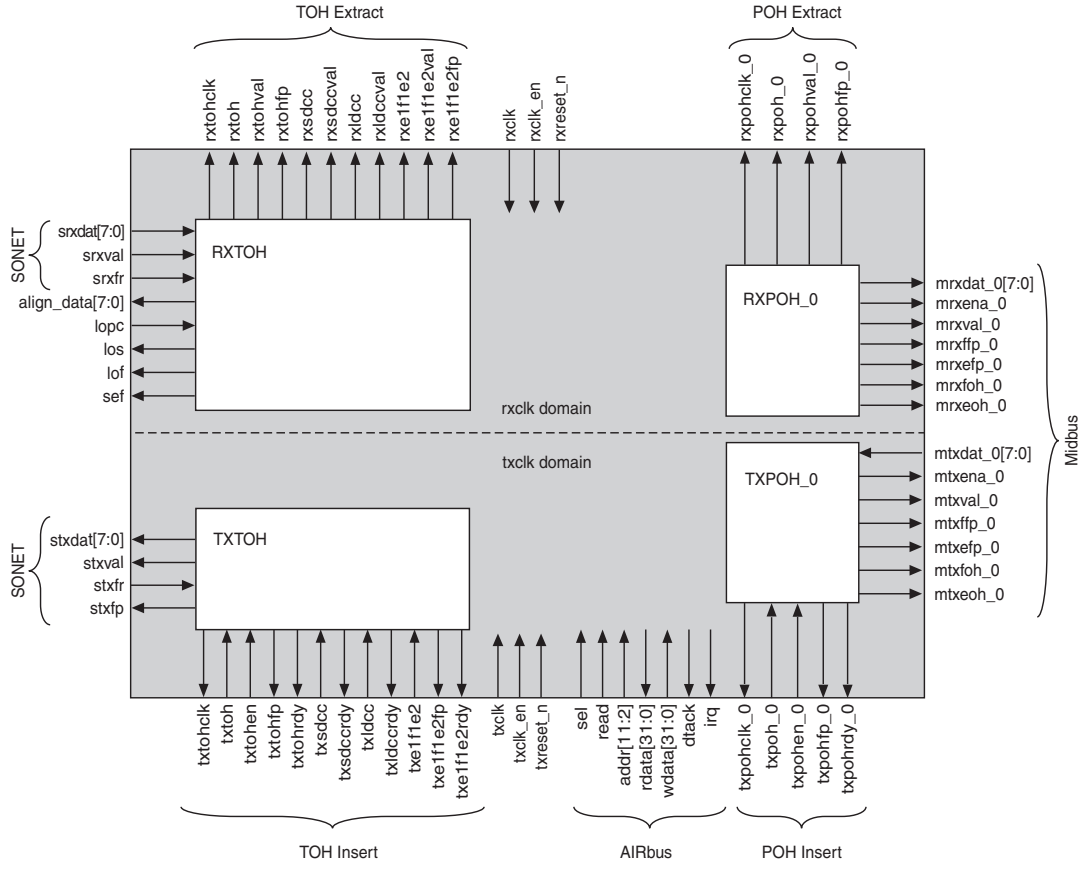
The Midbus interface is a simple synchronous full-duplex data path bus. The STS1FRM Midbus runs at 6.48 MHz over a single byte lane in each direction. In the receive (RX) direction, data is transferred from the Midbus master (RXPOH_0) to the slave. In the transmit (TX) direction, data is transferred from the slave to the master (TXPOH_0). In each direction, RX and TX, the Midbus can carry eight bits per clock cycle. It includes Midbus receive data (`mrxdat_0[7:0]`) and Midbus receive enable (`mrxena_0`) lines to indicate valid data transfers in the RX direction, and Midbus transmit data (`mtxdat_0[7:0]`) and Midbus data enable (`mtxena_0`) lines to indicate valid data requests in the TX direction.

AIRbus

The AIRbus interface provides access to internal registers using a simple synchronous internal bus protocol. This consists of separate read data (`rdata[31:0]`) and write data (`wdata[31:0]`) buses, a data transfer acknowledge (`dtack`) signal, and a block select (`sel`) signal. An address (`addr[11:2]`) bus and read (`read`) signal indicate the location and type of access within the block. The `rdata` buses and `dtack` signals can be merged from multiple blocks using a simple OR function. The `dtack` signal is sustained until the block `sel` is removed (four-way handshaking), meaning the AIRbus can cross clock domain boundaries. In the STS1FRM the AIRbus has a data width of 32 bits.

More detailed information on the Midbus, and AIRbus is available from the Altera web site at http://www.altera.com/IPmegastore.

Figure 2. Block Diagram



I/O Signals

The following is a port list for the STS1FRM. The signal direction is indicated by (I) for input, or (O) for output.

RX Clock Domain Signals: `rxclk` (I), `rxclk_en` (I), `rxreset_n` (I); **SONET Signals:** `srxdat[7:0]` (I), `srxval` (I), `srxfr` (I); **Maintenance Signals:** `align_data[7:0]` (O), `lopc` (I), `los` (O), `lof` (O), `sef` (O); **Hardware Serial TOH Extract Signals:** `rxtohclk` (O), `rxtoh` (O), `rxtohval` (O), `rxtohfp` (O), `rxsdcc` (O), `rxsdccval` (O), `rxldcc` (O), `rxldccval` (O), `rxe1f1e2` (O), `rxe1f1e2val` (O), `rxe1f1e2fp` (O); **Hardware Serial POH Extract Signals:** `rxpohclk_0` (O), `rxpoh_0` (O), `rxpohval_0` (O), `rxpohfp_0` (O); **Midbus Signals:** `mrxdat_0[7:0]` (O), `mrxena_0` (O), `mrxval_0` (O), `mrxffp_0` (O), `mrxefp_0` (O), `mrxfoh_0` (O), `mrxeoh_0` (O).

AIRbus Signals: `sel` (I), `read` (I), `addr[11:2]` (I), `rdata[31:0]` (O), `wdata[31:0]` (I), `dtack` (O), `irq` (O).

TX Clock Domain Signals: txclk (I), txclk_en (I), txreset_n (I); **SONET Signals:** stxdat[7:0] (O), stxval (O), stxfr (I), stxfp (O); **Hardware Serial TOH Insert Signals:** txtohclk (O), txtoh (I), txtohen (I), txtohfp (O), txtohrdy (O), txsdcc (I), txsdccrdy (O), txldcc (I), txldccrdy (O), txe1f1e2 (I), txe1f1e2fp (O), txe1f1e2rdy (O); **Hardware Serial POH Insert Signals:** txpohclk_0 (O), txpoh_0 (I), txpohen_0 (I), txpohfp_0 (O), txpohrdy_0 (O); **Midbus Signals:** mtxdat_0[7:0] (I), mtxena_0 (O), mtxval_0 (O) mtxffp_0 (O), mtxefp_0 (O), mtxfoh_0 (O), mtxeoh_0 (O).

Performance

Table 1 shows the required speed and estimated gate count of the STS1FRM in an APEX 20KE device.

Table 1. Performance *Note (1)*

LEs	ESBs	Frequency (MHz)
4,169 – 6,843	1 – 11	6.48 required to support 51.84 Mbps

Note:
(1) The numbers for the logic elements (LEs) and embedded system blocks (ESBs) are approximate as of May 25, 2001. They reflect the range from the basic to the full feature variant.

Generating Variants

Table 2 shows the optional features available to generate all variants.

Table 2. Optional Features *Note (1)*

Options	Parameters	Choices	LEs	ESBs
Basic Configuration	–	–	**4,169**	**1**
Serial insertion/extraction of TOH and POH bytes	SOH	Y/N	619	0
64-byte insert, extract, and expect buffers Automatic monitoring of extracted section trace J0 (transport overhead)	J0B	Y/N	305	3
64-byte insert, extract, and expect buffers Automatic monitoring of extracted path trace J1 (path overhead)	J1B	Y/N	284	3
Bit error rate monitoring with one second window	BM1S	Y/N	1,495	4

Note:
(1) The numbers for the LEs and ESBs are approximate as of May 25, 2001. Users are strongly advised to run the MegaWizard Plug-In and the Quartus II software to see exact numbers for each STS1FRM variant.

Licensing

A license is not required to perform the following trial operations using your own custom logic:

- Instantiation
- Place-and-route
- Static timing analysis
- Simulation on a third-party simulator

Only when you are ready to generate programming files, do you need to obtain licenses through your local Altera sales representative.

All current variants use a single license with ordering code: PLSM-STS1FRM.

Deliverables

The following elements are provided with the STS1FRM package:

- Data sheet
- User guide
- Midbus and AIRbus interface functional specifications
- MegaWizard Plug-In
  - Encrypted gate level netlist
  - Place-and-route constraints (where necessary)
  - Secure RTL simulation model
- Demo testbench
- Access to problem reporting system

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