FEATURES

- 20 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY016/TMC216, Cypress CY7C516, IDT 7216L, and AMD Am29516
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- DECC SMD No. 5962-86873
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Ceramic PGA
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC

DESCRIPTION

The **LMU16** and **LMU216** are high-speed, low power 16-bit parallel multipliers. The LMU16 and LMU216 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU16 and LMU216 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control bit are similarly loaded by CLK B. The TCA and TCB controls specify the A and B operands as two's complement when HIGH, or unsigned magnitude when LOW.
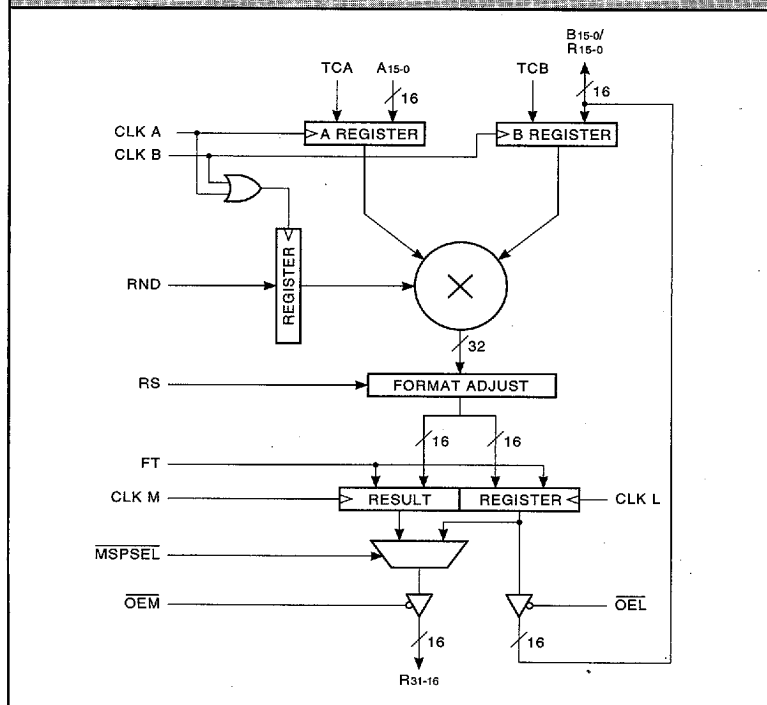
RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS HIGH gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output, these registers may be made transparent by setting the feed through control (FT) HIGH.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. MSPSEL LOW causes the MSP outputs to be driven by the most significant half of the result. MSPSEL HIGH routes the least significant half of the result to the MSP outputs. In addition, the LSP is available via the B port through a separate three-state buffer.

The output multiplexer control MSPSEL uses a pin which is a supply ground in the TRW MPY016H/TMC216H. When this control is LOW (GND), the function is that of the MPY016H/TMC216H, thus allowing full compatibility.

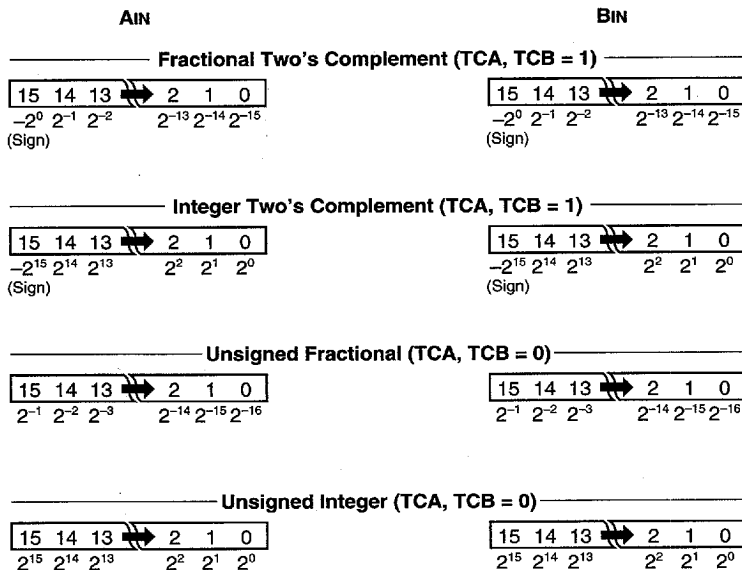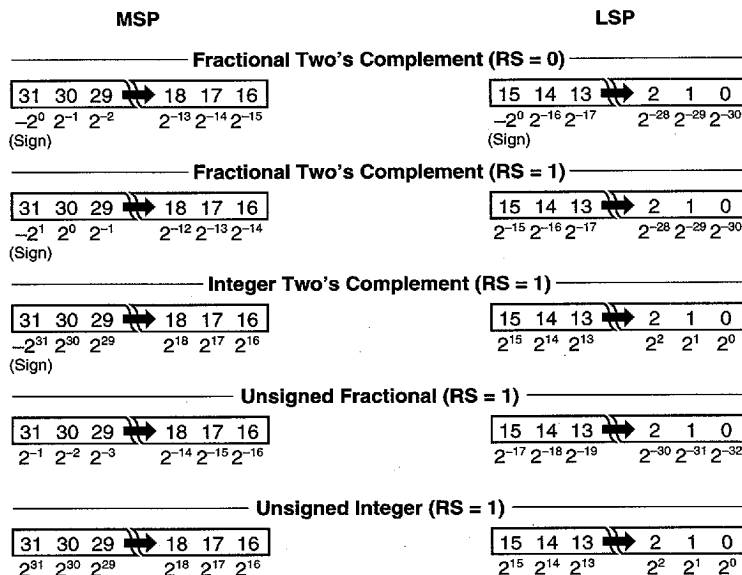## LMU16/216 BLOCK DIAGRAM

Multipliers

FIGURE 1A. INPUT FORMATS

AIN | BIN

——— Fractional Two's Complement (TCA, TCB = 1) ———

| 15 14 13 ➡ 2 1 0 |
-2^0 2^{-1} 2^{-2} $\quad$ 2^{-13} 2^{-14} 2^{-15}
(Sign)

| 15 14 13 ➡ 2 1 0 |
-2^0 2^{-1} 2^{-2} $\quad$ 2^{-13} 2^{-14} 2^{-15}
(Sign)

——— Integer Two's Complement (TCA, TCB = 1) ———

| 15 14 13 ➡ 2 1 0 |
-2^{15} 2^{14} 2^{13} $\quad$ 2^2 2^1 2^0
(Sign)

| 15 14 13 ➡ 2 1 0 |
-2^{15} 2^{14} 2^{13} $\quad$ 2^2 2^1 2^0
(Sign)

——— Unsigned Fractional (TCA, TCB = 0) ———

| 15 14 13 ➡ 2 1 0 |
2^{-1} 2^{-2} 2^{-3} $\quad$ 2^{-14} 2^{-15} 2^{-16}

| 15 14 13 ➡ 2 1 0 |
2^{-1} 2^{-2} 2^{-3} $\quad$ 2^{-14} 2^{-15} 2^{-16}

——— Unsigned Integer (TCA, TCB = 0) ———

| 15 14 13 ➡ 2 1 0 |
2^{15} 2^{14} 2^{13} $\quad$ 2^2 2^1 2^0

| 15 14 13 ➡ 2 1 0 |
2^{15} 2^{14} 2^{13} $\quad$ 2^2 2^1 2^0

FIGURE 1B. OUTPUT FORMATS

MSP | LSP

——— Fractional Two's Complement (RS = 0) ———

| 31 30 29 ➡ 18 17 16 |
-2^0 2^{-1} 2^{-2} $\quad$ 2^{-13} 2^{-14} 2^{-15}
(Sign)

| 15 14 13 ➡ 2 1 0 |
-2^0 2^{-16} 2^{-17} $\quad$ 2^{-28} 2^{-29} 2^{-30}
(Sign)

——— Fractional Two's Complement (RS = 1) ———

| 31 30 29 ➡ 18 17 16 |
-2^1 2^0 2^{-1} $\quad$ 2^{-12} 2^{-13} 2^{-14}
(Sign)

| 15 14 13 ➡ 2 1 0 |
2^{-15} 2^{-16} 2^{-17} $\quad$ 2^{-28} 2^{-29} 2^{-30}

——— Integer Two's Complement (RS = 1) ———

| 31 30 29 ➡ 18 17 16 |
-2^{31} 2^{30} 2^{29} $\quad$ 2^{18} 2^{17} 2^{16}
(Sign)

| 15 14 13 ➡ 2 1 0 |
2^{15} 2^{14} 2^{13} $\quad$ 2^2 2^1 2^0

——— Unsigned Fractional (RS = 1) ———

| 31 30 29 ➡ 18 17 16 |
2^{-1} 2^{-2} 2^{-3} $\quad$ 2^{-14} 2^{-15} 2^{-16}

| 15 14 13 ➡ 2 1 0 |
2^{-17} 2^{-18} 2^{-19} $\quad$ 2^{-30} 2^{-31} 2^{-32}

——— Unsigned Integer (RS = 1) ———

| 31 30 29 ➡ 18 17 16 |
2^{31} 2^{30} 2^{29} $\quad$ 2^{18} 2^{17} 2^{16}

| 15 14 13 ➡ 2 1 0 |
2^{15} 2^{14} 2^{13} $\quad$ 2^2 2^1 2^0

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Multipliers

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

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SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol	Parameter	LMU16/216–											
		65		55		45		35		25		20	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		55		45		35		25		20
t_{MUC}	Unclocked Multiply Time		85		75		65		55		38		30
t_{PW}	Clock Pulse Width	15		15		15		10		10		9	
t_S	Input Setup Time	15		15		15		12		12		11	
t_H	Input Hold Time	1		1		1		1		1		1	
t_D	Output Delay		30		30		30		25		20		18
t_{SEL}	Output Select Delay		25		25		25		25		20		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25		25		20		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25		22		20		18

MILITARY OPERATING RANGE (–55°C to +125°C) Notes 9, 10 (ns)

Symbol	Parameter	LMU16/216–											
		75		65		55		40		30		25	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		65		55		40		30		25
t_{MUC}	Unclocked Multiply Time		95		85		75		60		43		38
t_{PW}	Clock Pulse Width	20		15		15		15		10		10	
t_S	Input Setup Time	15		15		15		15		12		12	
t_H	Input Hold Time	2		2		2		2		2		2	
t_D	Output Delay		35		30		30		25		20		20
t_{SEL}	Output Select Delay		30		30		30		25		20		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25		25		20		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25		25		22		22

SWITCHING WAVEFORMS
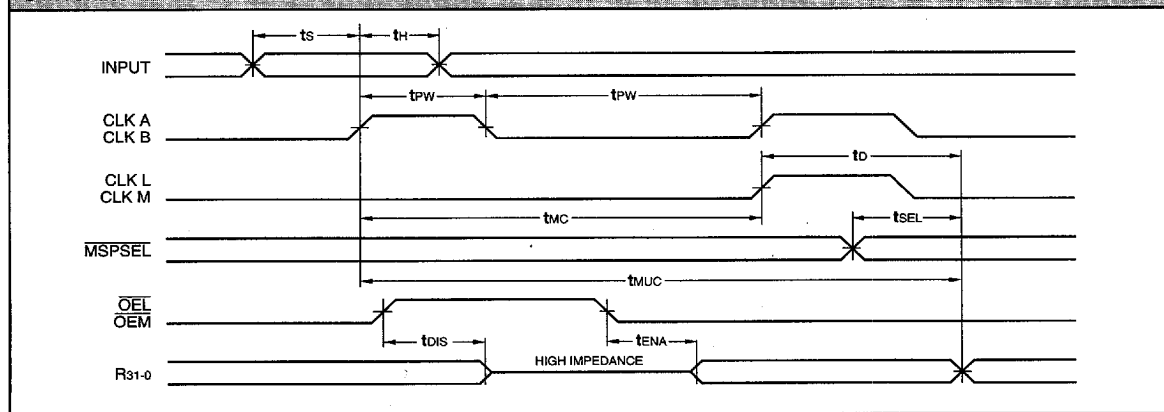
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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at –0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the tENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the tDIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.
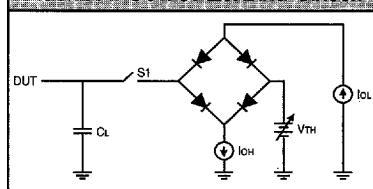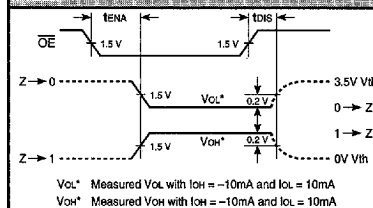

FIGURE A. OUTPUT LOADING CIRCUIT

FIGURE B. THRESHOLD LEVELS

VOL* Measured VOL with IOH = –10mA and IOL = 10mA
VOH* Measured VOH with IOH = –10mA and IOL = 10mA

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Multipliers

01/15/97–LDS.16/216-K

LMU16 — ORDERING INFORMATION

64-pin

A4	1		64	A5
A3	2		63	A6
A2	3		62	A7
A1	4		61	A8
A0	5		60	A9
$\overline{OEL}$	6		59	A10
CLK L	7		58	A11
CLK B	8		57	A12
R0, B0	9		56	A13
R1, B1	10		55	A14
R2, B2	11		54	A15
R3, B3	12		53	CLK A
R4, B4	13		52	RND
R5, B5	14		51	TCA
R6, B6	15		50	TCB
R7, B7	16		49	Vcc
R8, B8	17		48	Vcc
R9, B9	18		47	GND
R10, B10	19		46	GND
R11, B11	20		45	$\overline{MSPSEL}$
R12, B12	21		44	FT
R13, B13	22		43	RS
R14, B14	23		42	$\overline{OEM}$
R15, B15	24		41	CLK M
R16	25		40	R31
R17	26		39	R30
R18	27		38	R29
R19	28		37	R28
R20	29		36	R27
R21	30		35	R26
R22	31		34	R25
R23	32		33	R24

68-pin

Top View
Through Package
(i.e., Component Side Pinout)
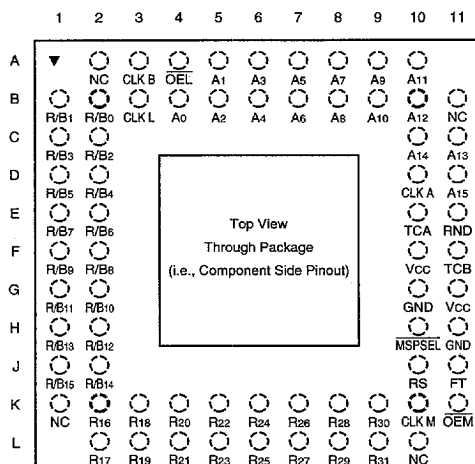
* 64-pin DIP not recommended for new designs

Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
0°C to +70°C — COMMERCIAL SCREENING		
65 ns	LMU16DC65	LMU16GC65
55 ns	LMU16DC55	LMU16GC55
45 ns	LMU16DC45	LMU16GC45
35 ns	LMU16DC35	LMU16GC35
25 ns		LMU16GC25
20 ns		LMU16GC20
–55°C to +125°C — COMMERCIAL SCREENING		
75 ns	LMU16DM75	LMU16GM75
65 ns	LMU16DM65	LMU16GM65
55 ns	LMU16DM55	LMU16GM55
40 ns	LMU16DM40	LMU16GM40
30 ns		LMU16GM30
25 ns		LMU16GM25
–55°C to +125°C — MIL-STD-883 COMPLIANT		
75 ns	LMU16DMB75	LMU16GMB75
65 ns	LMU16DMB65	LMU16GMB65
55 ns	LMU16DMB55	LMU16GMB55
40 ns	LMU16DMB40	LMU16GMB40
30 ns		LMU16GMB30
25 ns		LMU16GMB25

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Multipliers

LMU216 — ORDERING INFORMATION

68-pin

Top View

Pin labels (top, left to right): NC, CLK M, OEM, RS, FT, MSPSEL, GND, GND, Vcc, Vcc, TCB, TCA, RND, CLK A, A15, A14, A13

Left side (top to bottom, pins 10–26): R31 10, R30 11, R29 12, R28 13, R27 14, R26 15, R25 16, R24 17, R23 18, R22 19, R21 20, R20 21, R19 22, R18 23, R17 24, R16 25, NC 26

Right side (top to bottom, pins 60–44): 60 NC, 59 A12, 58 A11, 57 A10, 56 A9, 55 A8, 54 A7, 53 A6, 52 A5, 51 A4, 50 A3, 49 A2, 48 A1, 47 A0, 46 OEL, 45 CLK L, 44 CLK B

Bottom pins (27–43): R15, B15 27; R14, B14 28; R13, B13 29; R12, B12 30; R11, B11 31; R10, B10 32; R9, B9 33; R8, B8 34; R7, B7 35; R6, B6 36; R5, B5 37; R4, B4 38; R3, B3 39; R2, B2 40; R1, B1 41; R0, B0 42; NC 43

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Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
0°C to +70°C — COMMERCIAL SCREENING				
65 ns	LMU216JC65			
55 ns	LMU216JC55			
45 ns	LMU216JC45			
35 ns	LMU216JC35			
25 ns	LMU216JC25			
20 ns	LMU216JC20			
–55°C to +125°C — COMMERCIAL SCREENING				
–55°C to +125°C — MIL-STD-883 COMPLIANT				
75 ns		LMU216KMB75		
65 ns		LMU216KMB65		
55 ns		LMU216KMB55		
40 ns		LMU216KMB40		
30 ns		LMU216KMB30		
25 ns		LMU216KMB25		