Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60
t_{RAC}	$\overline{\text{RAS}}$ Access Time	60ns
t_{CAC}	$\overline{\text{CAS}}$ Access Time	15ns
t_{AA}	Access Time From Address	30ns
t_{RC}	Cycle Time	104ns
t_{HPC}	EDO Mode Cycle Time	25ns

- High Performance CMOS process
- Single 3.3 ± 0.3V Power Supply
- Low active current consumption
- All inputs & outputs are LVTTL(3.3V) compatible
- Extended Data Out (EDO) access cycle
- Refresh Modes: $\overline{\text{RAS}}$-Only, CBR, Hidden and Self Refresh
- 1024 refresh cycles distributed across 128ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au contacts

Description

The IBM11S2325LP is an 8MB industry standard 72-pin 4-byte small outline dual in-line memory module (SO DIMM). The module is organized as a 2Mx32 dual bank high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with four 1Mx16 TSOP devices, each in a 400mil package.

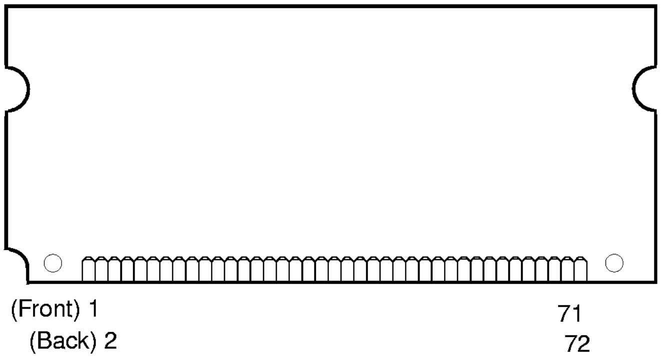
The IBM11S1325LP is a 4MB half populated version, manufactured with two 1Mx16 TSOP devices and is organized as a single bank 1Mx32 high speed memory array.

The use of EDO DRAMs allows for a reduction in cycle time from 40ns (Fast Page) to 25ns (EDO, 60ns sort). The use of TSOP packages allows for tight DIMM spacing (.3” on center). Input loading is consistent with 4Mb device-based assemblies due to the addition of discrete capacitors maximizing compatibility at the system level.

These assemblies are intended for use in space constrained and or low power applications.

The IBM 72-Pin SO DIMMs provide a high performance, flexible 4-byte interface in a 2.35” long footprint.

Card Outline



Pin Description

$\overline{\text{RAS}}$0, $\overline{\text{RAS}}$2	Row Address Strobe (4MB)
$\overline{\text{RAS}}$0 - $\overline{\text{RAS}}$3	Row Address Strobe (8MB)
$\overline{\text{CAS}}$0 - $\overline{\text{CAS}}$3	Column Address Strobe
$\overline{\text{WE}}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

Pinout

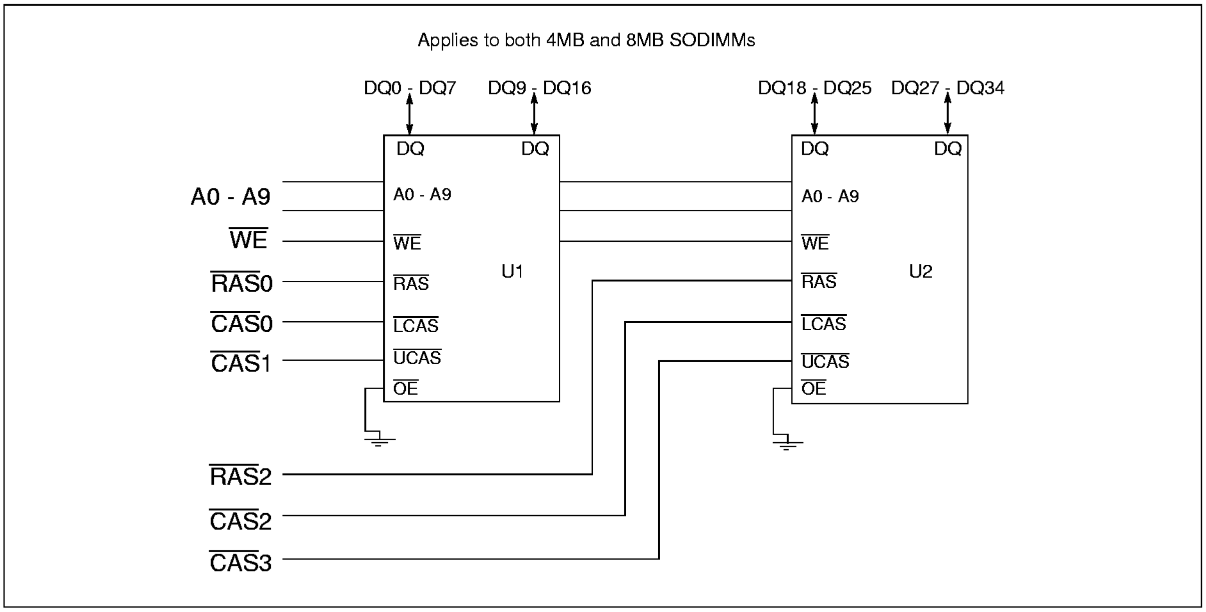
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{\text{CAS}}$0	52	DQ23	64	DQ34
5	DQ3	17	A5	29	NC	41	$\overline{\text{CAS}}$2	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{\text{CAS}}$3	54	DQ25	66	PD2
7	DQ5	19	NC	31	A8	43	$\overline{\text{CAS}}$1	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{\text{RAS}}$0	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	$\overline{\text{RAS}}$3*	45	$\overline{\text{RAS}}$1*	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{\text{RAS}}$2	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{\text{WE}}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

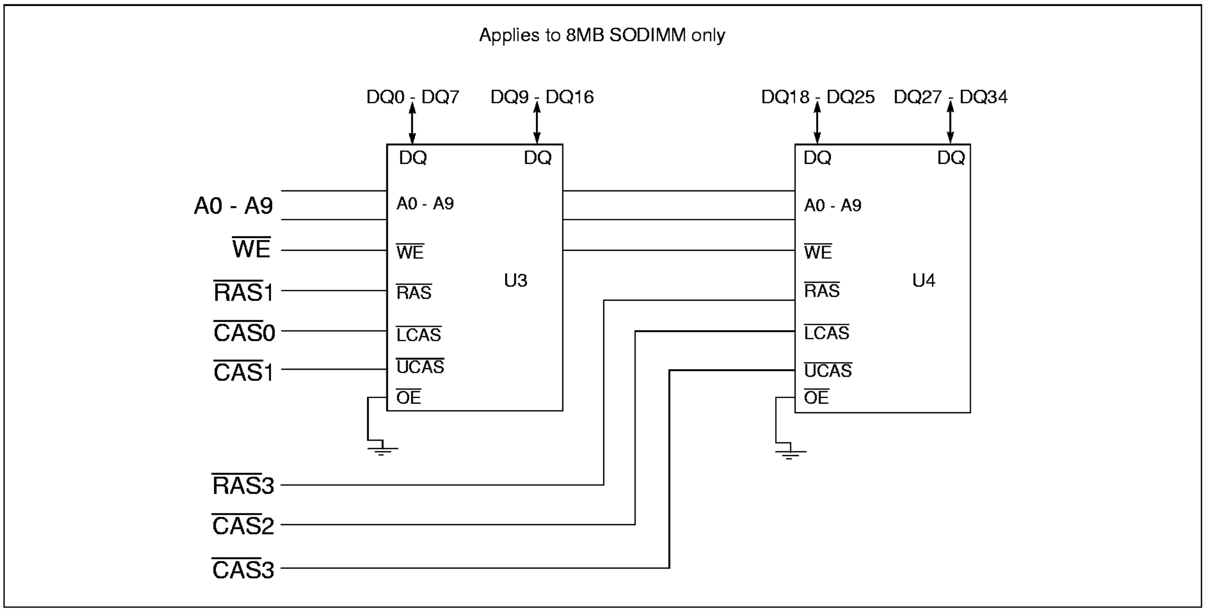
1. * $\overline{\text{RAS}}$1 and $\overline{\text{RAS}}$3 are “NC” on 4MB SO DIMM.

Ordering Information

Part Number	Organization	Speed	Dimensions	Power	Notes
IBM11S1325LP-60T	1M x 32	60ns	2.35” x 1” x .0965”	3.3V	
IBM11S2325LP-60T	2M x 32	60ns	2.35” x 1” x .1496”	3.3V	

Block Diagram





Truth Table

Function		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Row Address	Column Address	All DQ bits
Standby		H	X	X	X	X	High Impedance
Read		L	L	H	Row	Col	Valid Data Out
Early-Write		L	L	L	Row	Col	Valid Data In
EDO Mode - Read: 1st Cycle		L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles		L	H→L	H	N/A	Col	Valid Data Out
EDO Mode - Write: 1st Cycle		L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles		L	H→L	L	N/A	Col	Valid Data In
$\overline{\text{RAS}}$-Only Refresh		L	H	X	Row	N/A	High Impedance
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh		H→L	L	H	X	X	High Impedance
Hidden Refresh	Read	L→H→L	L	H	Row	Col	Data Out
	Write	L→H→L	L	L→H	Row	Col	Data In
Self Refresh		H→L	L	H	X	X	High Impedance

Presence Detect

Pin	1M x 32	2M x 32
	-60	-60
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	V_{SS}	V_{SS}
PD4	NC	V_{SS}
PD5	NC	NC
PD6	NC	NC
PD7	V_{SS}	V_{SS}

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter		Rating 3.3 Volt	Units	Notes
V_{CC}	Power Supply Voltage		-0.5 to + 4.6	V	1
V_{IN}	Input Voltage		-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
V_{OUT}	Output Voltage		-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature		0 to +70	°C	1
T_{STG}	Storage Temperature		-55 to +150C	°C	1
P_D	Power Dissipation	1Mx32	0.8	W	1
		2Mx32	1.5	W	1, 2
I_{OUT}	Short Circuit Output Current		50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active (refresh cycle).

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			Units	Notes
		Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 1.2V for pulse widths of $\leq$ 4.0ns with 3.3 Volt. Additionally, V_{IL} may undershoot to -2.0V for pulse widths $\leq$ 4.0ns. Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, $V_{CC} = 3.3 \pm 0.3$V)

Symbol	Parameter	1M x 32 Max	2M x 32 Max	Units
C_{I1}	Input Capacitance (A0-A9)	35	45	pF
C_{I2}	Input Capacitance (4MB: $\overline{\text{RAS}}$0, 8MB: $\overline{\text{RAS}}$0, 1)	16	16	pF
C_{I2}	Input Capacitance (4MB: $\overline{\text{RAS}}$2, 8MB: $\overline{\text{RAS}}$2, 3)	16	16	pF
C_{I4}	Input Capacitance ($\overline{\text{CAS}}$)	15	22	pF
C_{I5}	Input Capacitance ($\overline{\text{WE}}$)	36	50	pF
C_{IO}	Input - Output Capacitance (DQ0-DQ34)	16	23	pF

DC Electrical Characteristics (T_A = 0 to +70C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		1Mx32		2Mx32		Units	Notes
			Min	Max	Min	Max		
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ min)		—	210	—	210	mA	1, 2, 3
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS} = \overline{CAS} \geq V_{IH}$)		—	2	—	4	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH}$: $t_{RC} = t_{RC}$ min)		—	210	—	210	mA	1, 3, 4
I_{CC4}	EDO Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ min)		—	80	—	80	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC}$ - 0.2V)		—	.2	—	.4	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: $t_{RC} = t_{RC}$ min)		—	210	—	210	mA	1, 3, 4
I_{CC7}	Self Refresh Current Average Power Supply Current during Self Refresh (CBR Cycle with $\overline{RAS} \geq t_{RASS}$ (min))		—	400	—	400	µA	4
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input ($0.0 \leq V_{IN} \leq (V_{CC} < 6.0V)$) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-5	+5	-5	+5	µA	
		$\overline{CAS}$	-5	+5	-10	+10		
		Add & $\overline{WE}$	-10	+10	-20	+20		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, $0.0 \leq V_{OUT} \leq V_{CC}$)		-5	+5	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -2mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS} = V_{IL}$. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS} = V_{IH}$.
4. Refresh current is specified for one bank

AC Characteristics

(T_A = 0 to +70°C, V_{CC} = 3.3V ± 0.3V)

1. An initial pause of 200µs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles is required.
2. AC measurements assume t_T=2ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. When both $\overline{\text{CAS}}$0 & $\overline{\text{CAS}}$1 or $\overline{\text{CAS}}$2 & $\overline{\text{CAS}}$3 go low at the same time, all 16 bits of data are read/written into the device. $\overline{\text{CAS}}$0 & $\overline{\text{CAS}}$1 or $\overline{\text{CAS}}$2 & $\overline{\text{CAS}}$3 ($\overline{\text{CAS}}$'s to the same DRAM) cannot be staggered within the same read/write cycle.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	—	ns	
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	40	—	ns	
t_{CP}	$\overline{\text{CAS}}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	60	10K	ns	
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	10	10K	ns	
t_{ASR}	Row Address Setup Time	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	ns	
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	14	45	ns	1
t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	12	30	ns	2
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	10	—	ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	45	—	ns	
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	ns	
t_{DZC}	$\overline{\text{CAS}}$ Delay Time from D_{IN}	0	—	ns	
t_T	Transition Time (Rise and Fall)	2	30	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	1
t_{WCH}	Write Command Hold Time	10	—	ns	
t_{WP}	Write Command Pulse Width	10	—	ns	
t_{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	10	—	ns	
t_{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	10	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	10	—	ns	

1. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If neither of the above condition is not satisfied, the condition of the data out (at access time) is indeterminate.

Read Cycle

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{\text{RAS}}$	—	60	ns	1, 2, 3
t_{CAC}	Access Time from $\overline{\text{CAS}}$	—	15	ns	1, 3
t_{AA}	Access Time from Address	—	30	ns	2, 3
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	—	ns	4
t_{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	0	—	ns	4
t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	30	—	ns	
t_{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z	0	—	ns	3
t_{CDD}	$\overline{\text{CAS}}$ to D_{IN} Delay Time	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	—	15	ns	5, 6

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Measured with the specified current load and 100pF at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. t_{OFF} is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, which ever is last.

Extended Data Out Cycle

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{HCAS}	$\overline{\text{CAS}}$ Pulse Width (EDO Mode)	10	10K	ns	
t_{HPC}	EDO Mode Cycle Time (Read/Write)	25	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{\text{CAS}}$	5	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{\text{WE}}$	0	10	ns	
t_{WPZ}	$\overline{\text{WE}}$ Pulse Width to Output Disable at $\overline{\text{CAS}}$ High	10	—	ns	
t_{CPRH}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	35	—	ns	
t_{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge	—	35	ns	1
t_{RASP}	EDO Mode $\overline{\text{RAS}}$ Pulse Width	60	125K	ns	

1. Measured with the specified current load and 100pF at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.

Refresh Cycle

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle)	10	—	ns	
t_{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle)	5	—	ns	
t_{WRP}	$\overline{\text{WE}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle)	10	—	ns	
t_{WRH}	$\overline{\text{WE}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle)	10	—	ns	
t_{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	5	—	ns	
t_{REF}	Refresh Period	—	128	ms	1

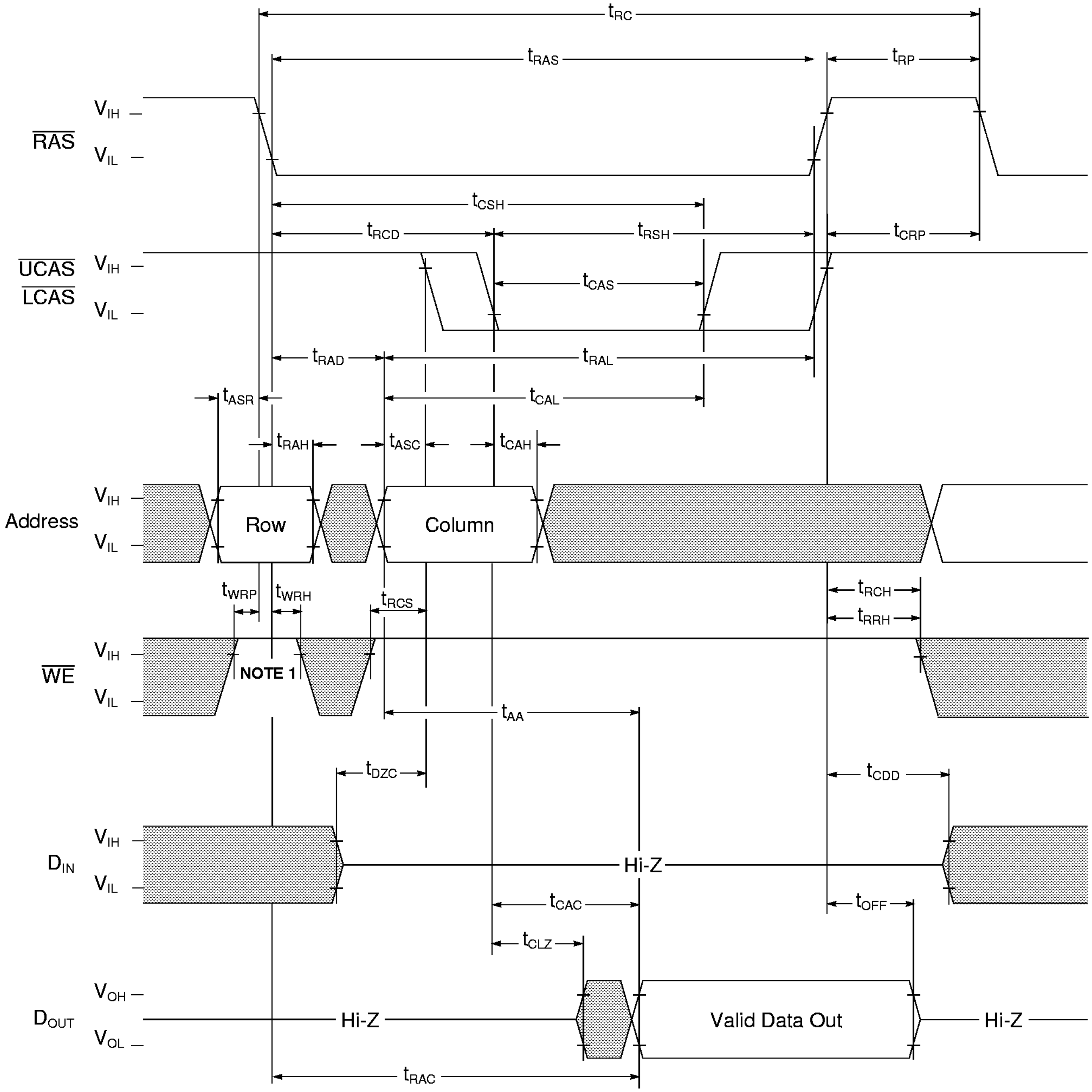
1. 1024 refreshes are required every 128ms.

Self Refresh Cycle

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{RASS}	$\overline{\text{RAS}}$ Pulse Width During Self Refresh Cycle	100	—	µs	1
t_{RPS}	$\overline{\text{RAS}}$ Precharge Time During Self Refresh Cycle	104	—	ns	1
t_{CHS}	$\overline{\text{CAS}}$ Hold Time During Self Refresh Cycle	-50	—	ns	1, 2
t_{CHD}	$\overline{\text{CAS}}$ Hold Time From RAS Falling During Self Refresh Cycle	350	—	µs	1, 2

1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in a EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.
2. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies. If $t_{RASS} \leq t_{CHD}$ (min) then t_{CHS} applies.

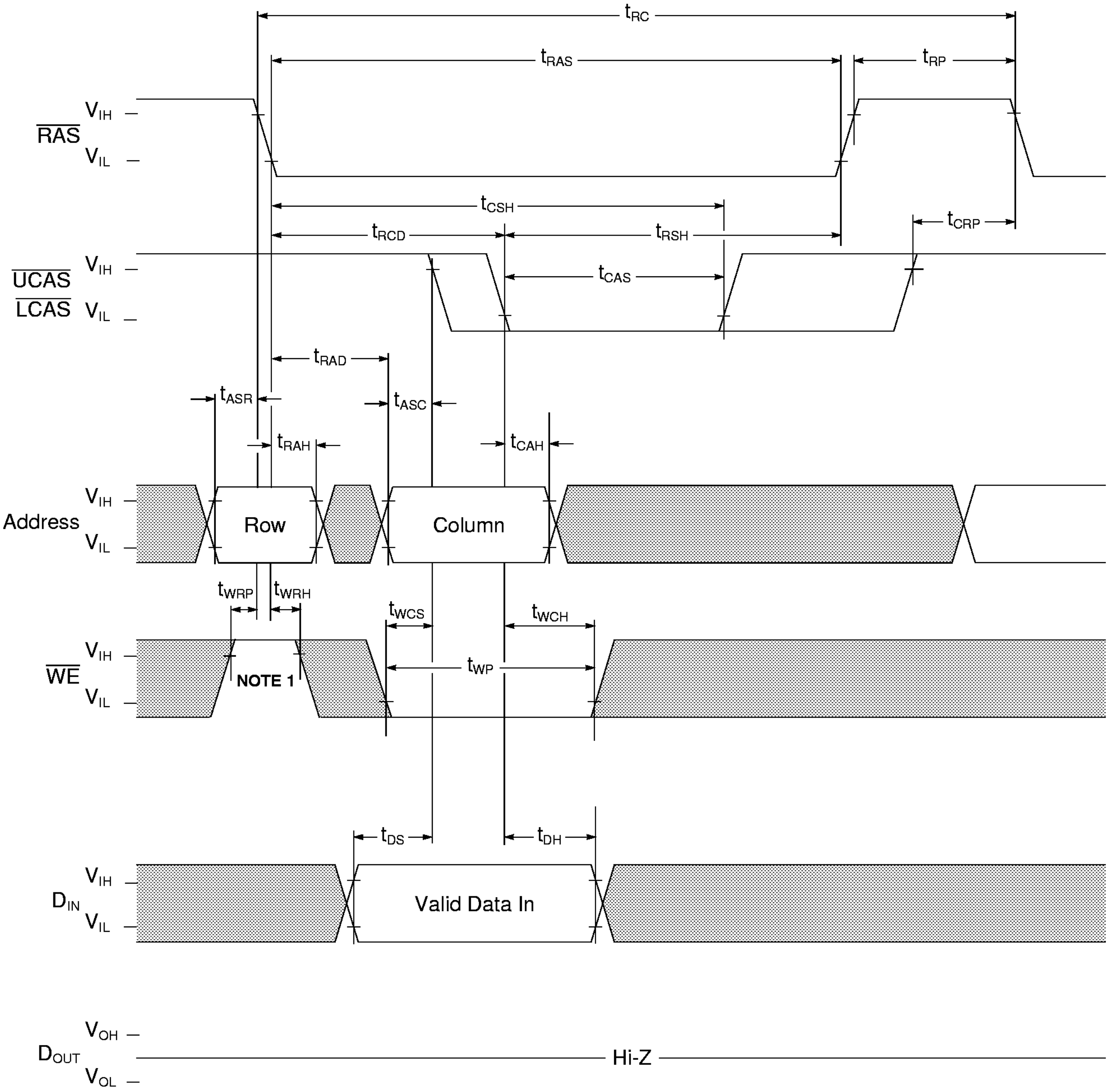
Read



▨ : “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

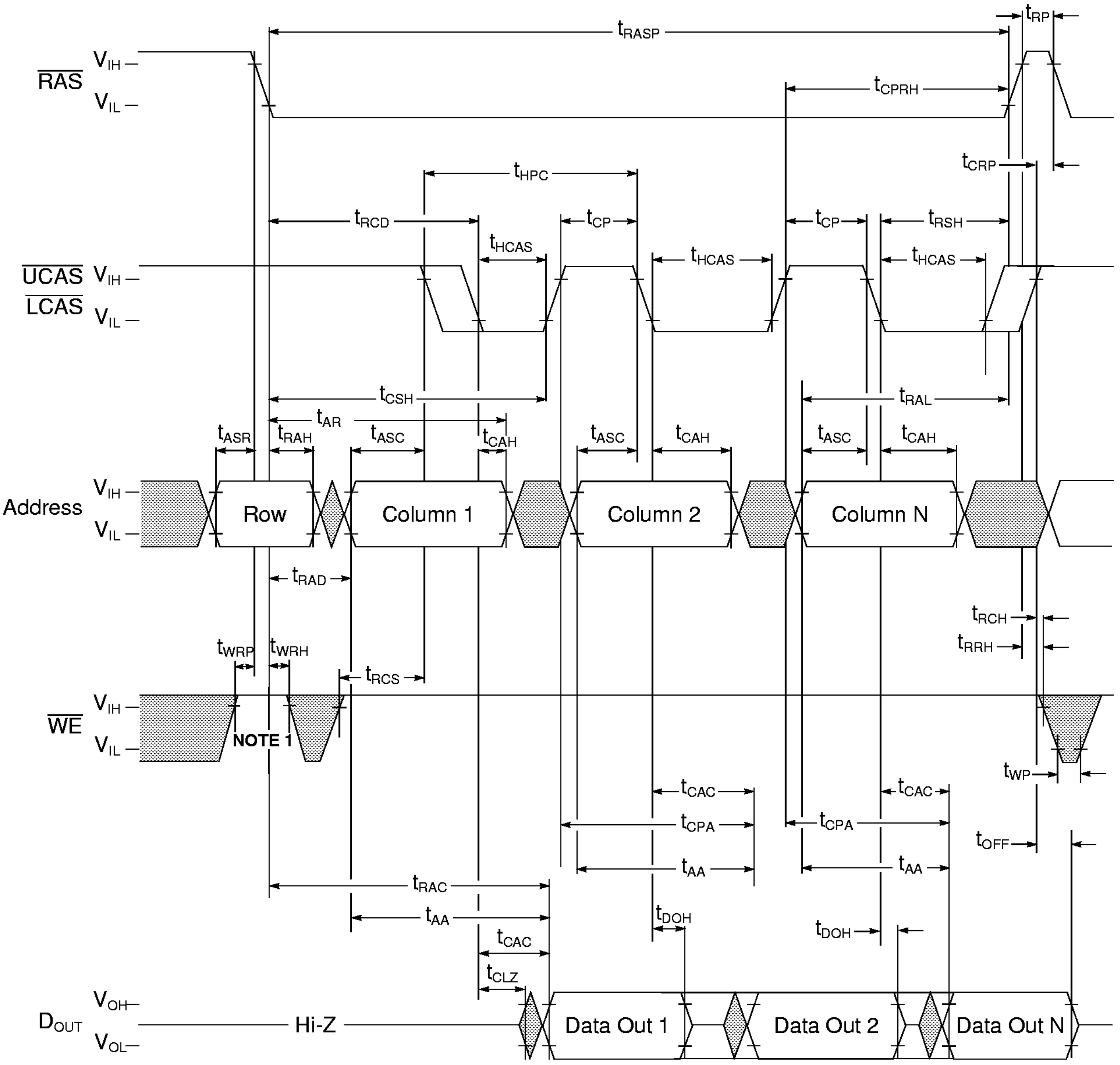
Write Cycle (Early Write)



▨ : “H” or “L”

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

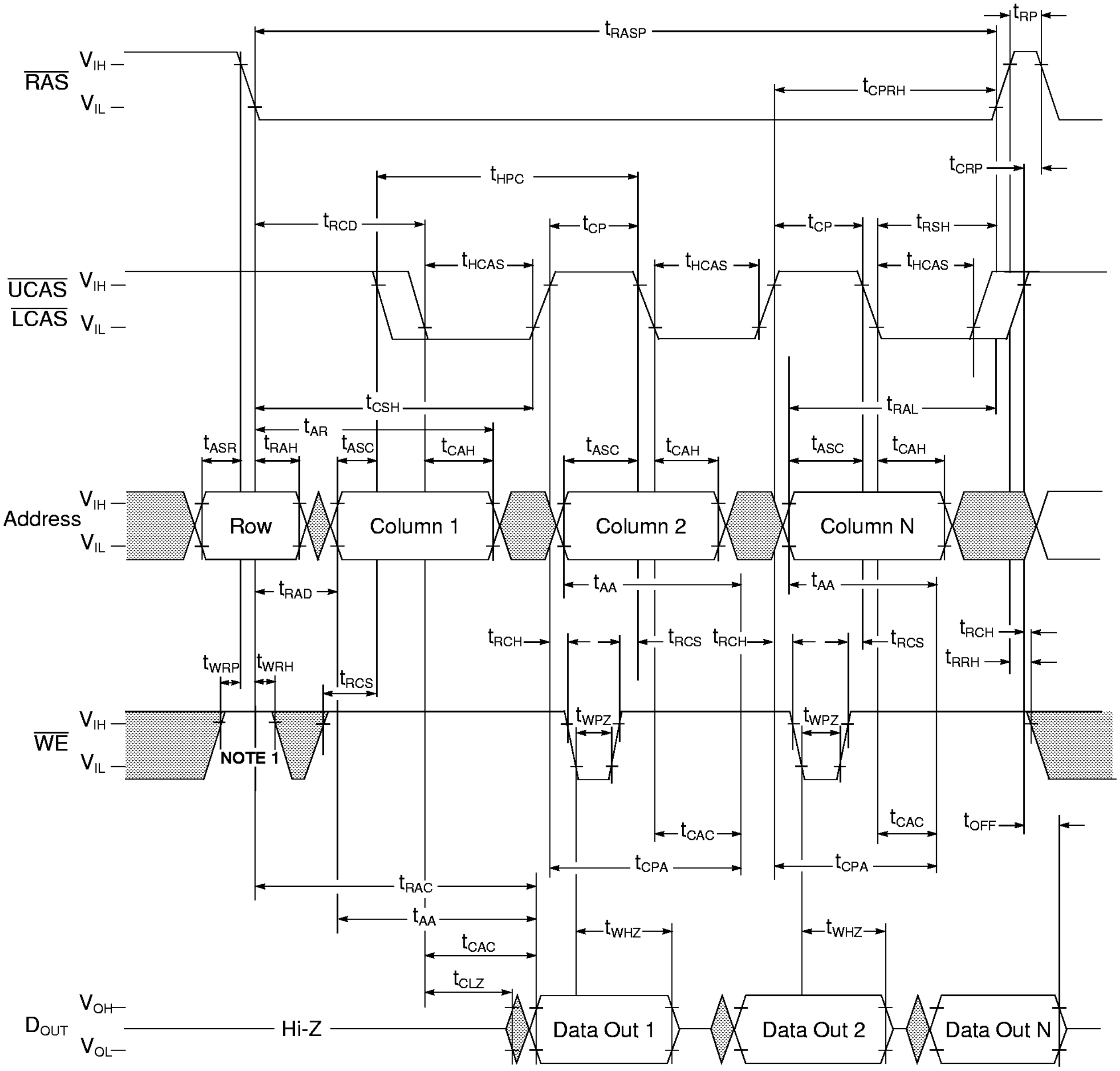
Extended Data Out Mode Read Cycle



▨ : "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

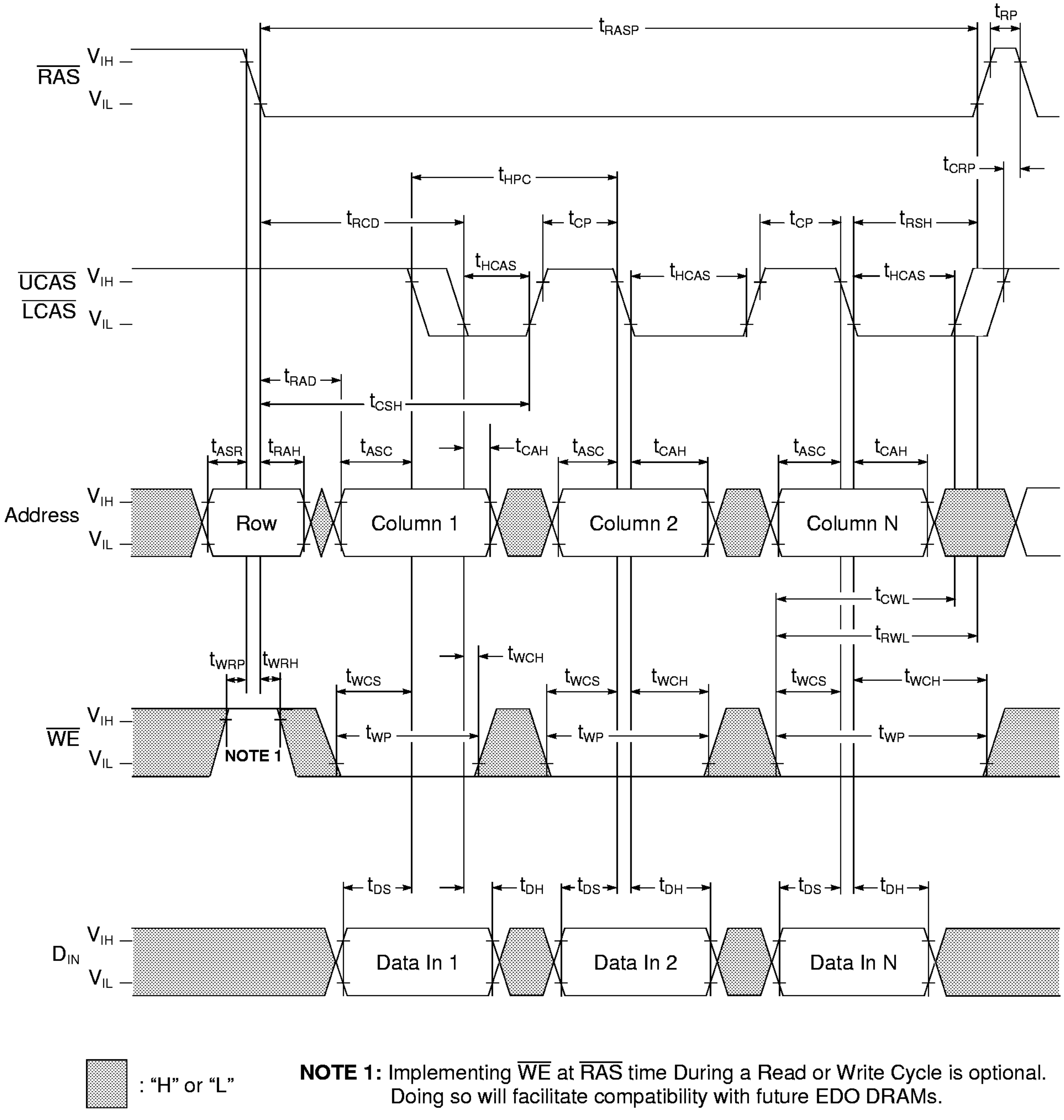
Extended Data Out Mode Read Cycle ($\overline{WE}$ Control)



▨ : "H" or "L"

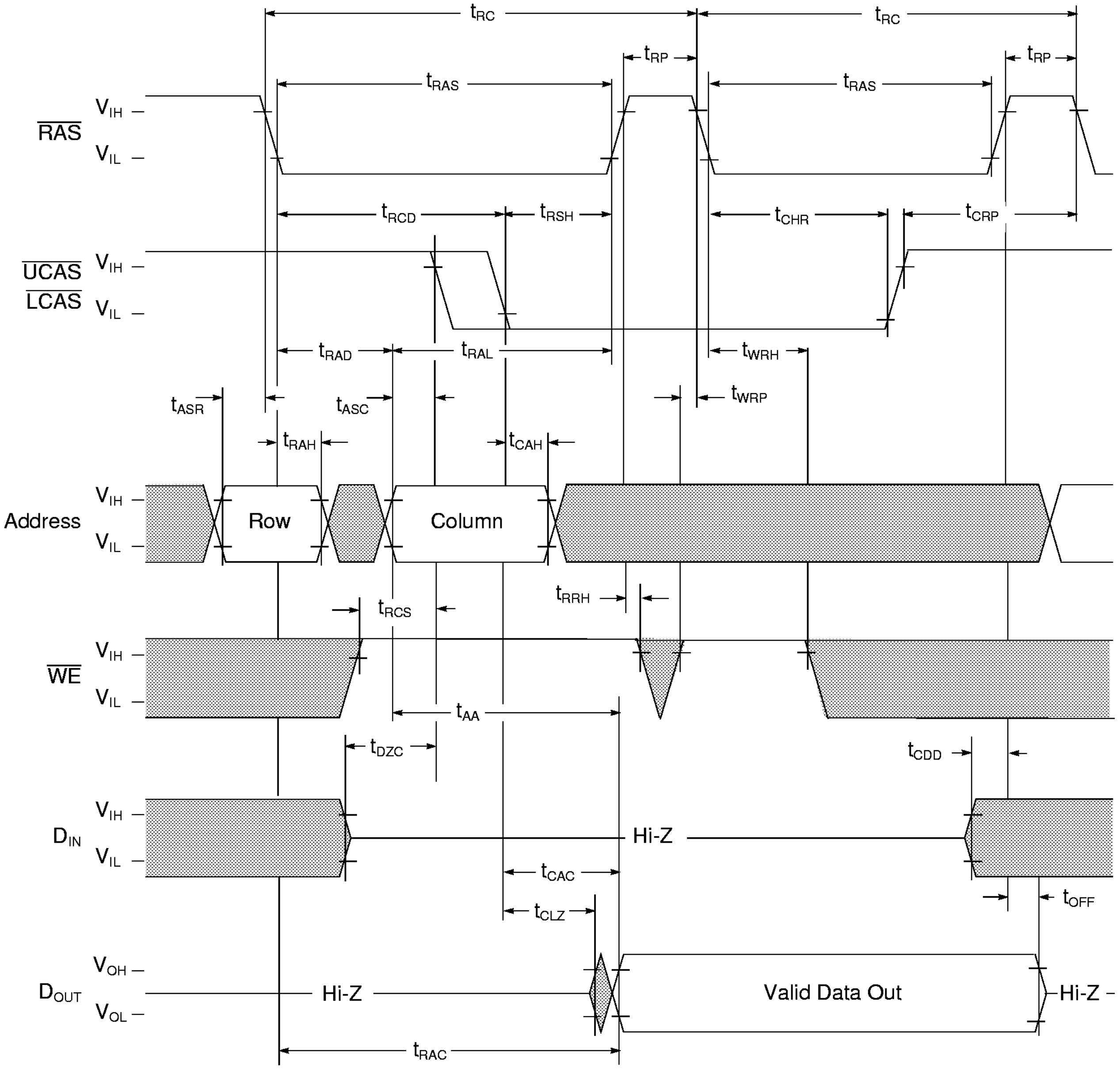
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Extended Data Out Mode Write Cycle



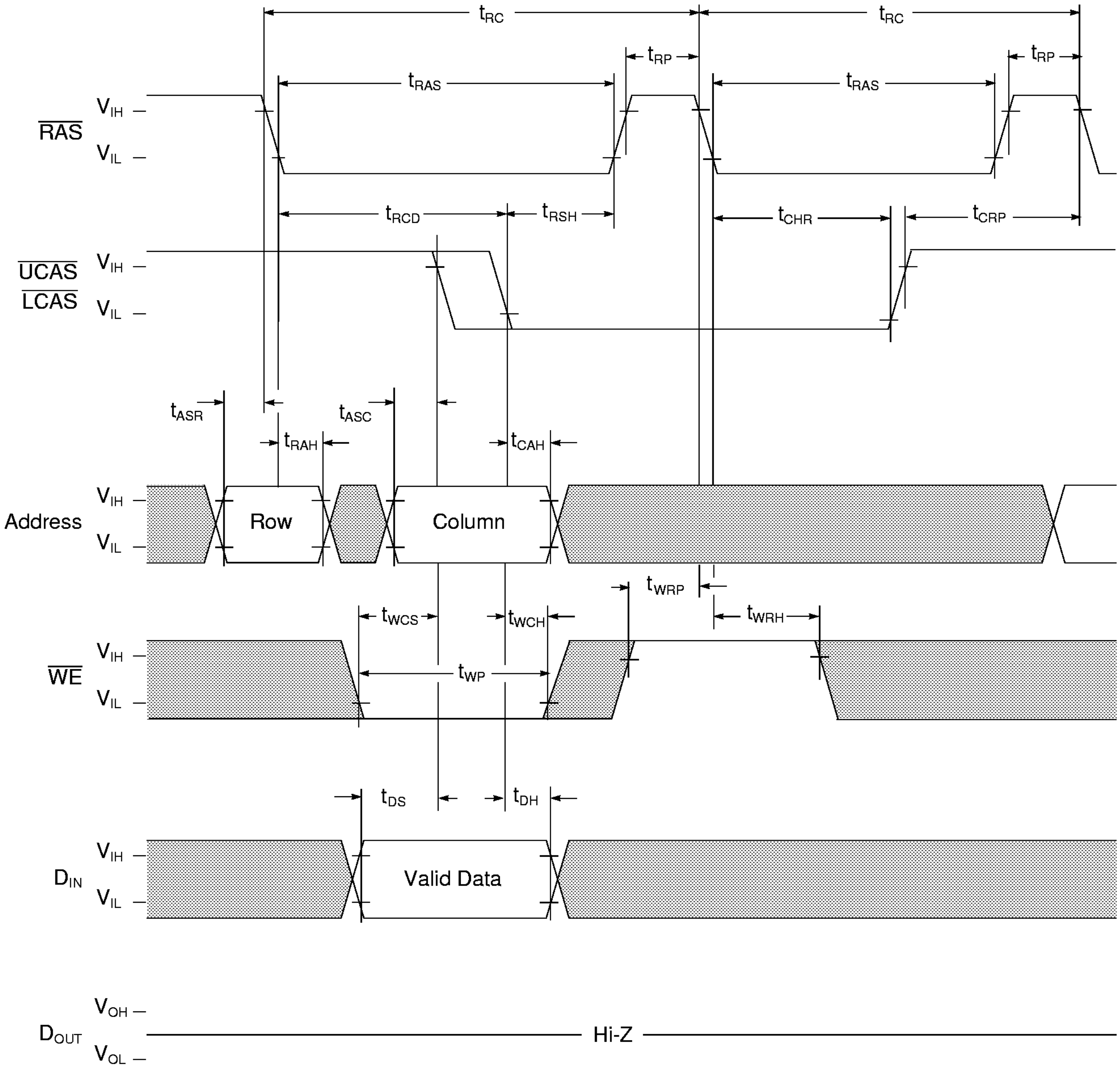
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Hidden Refresh Cycle (Read)



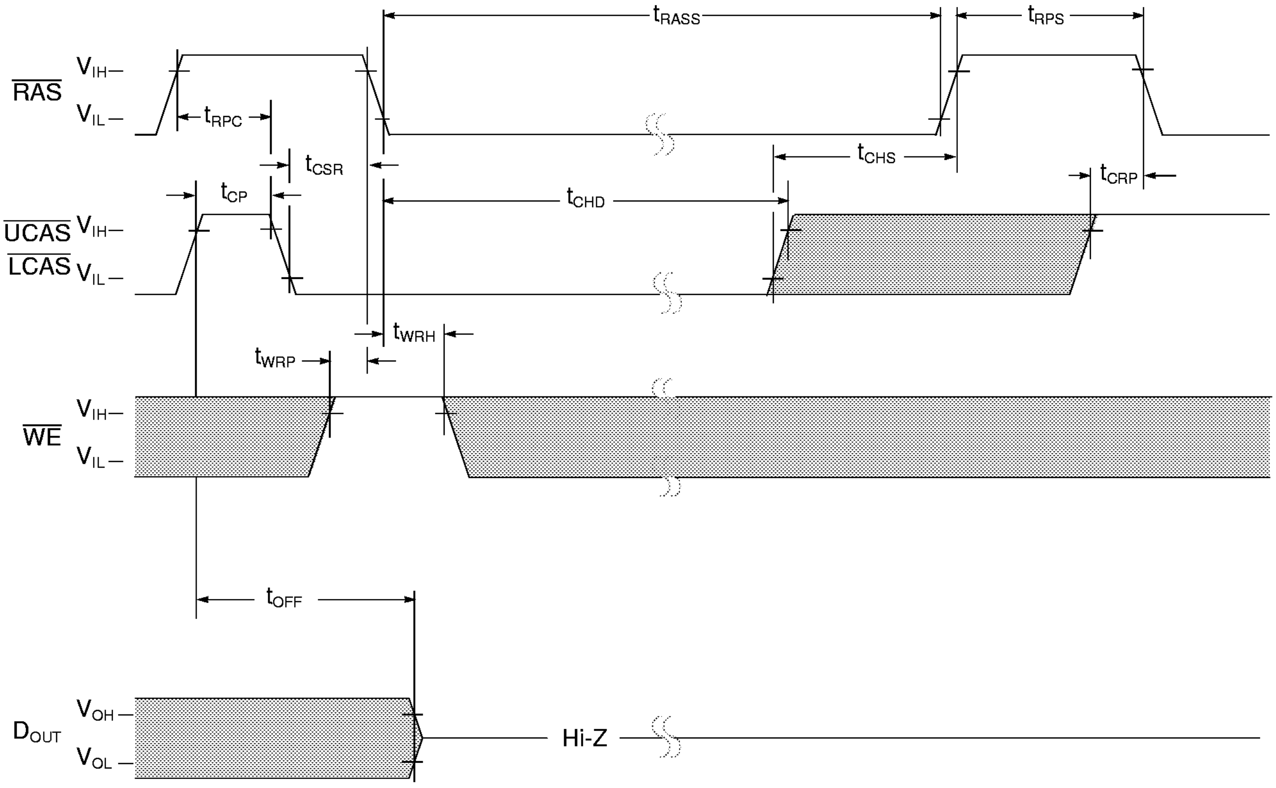
▨ : “H” or “L”

Hidden Refresh Cycle (Write)



▨ : “H” or “L”

Self Refresh Cycle (Sleep Mode)

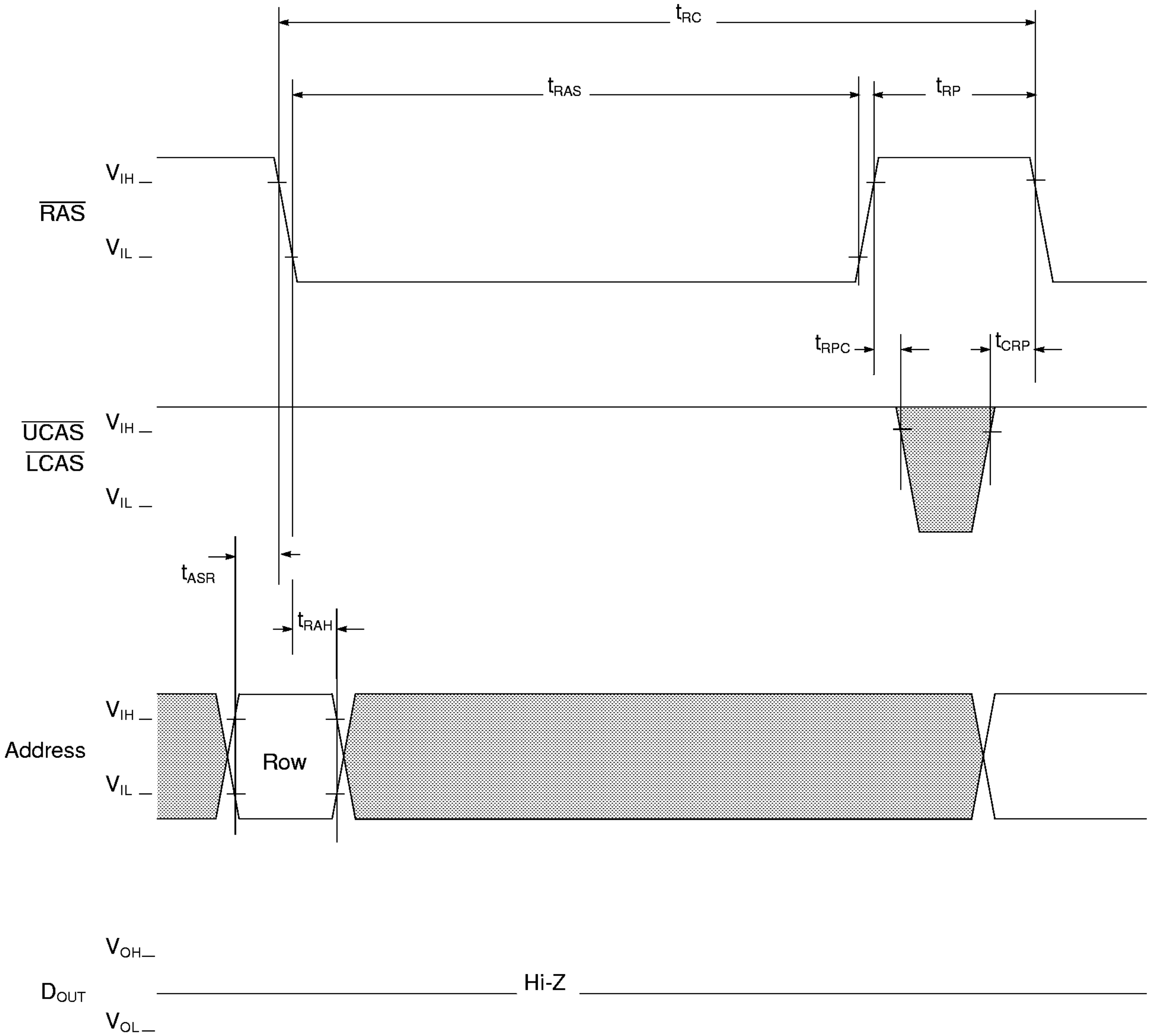


▨ : "H" or "L"

NOTES:

1. Address is "H" or "L"
2. Once t_{RASS} (min) is provided and $\overline{RAS}$ remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."
3. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies.
   If $t_{RASS} \leq t_{CHD}$ (min) then t_{CHS} applies.

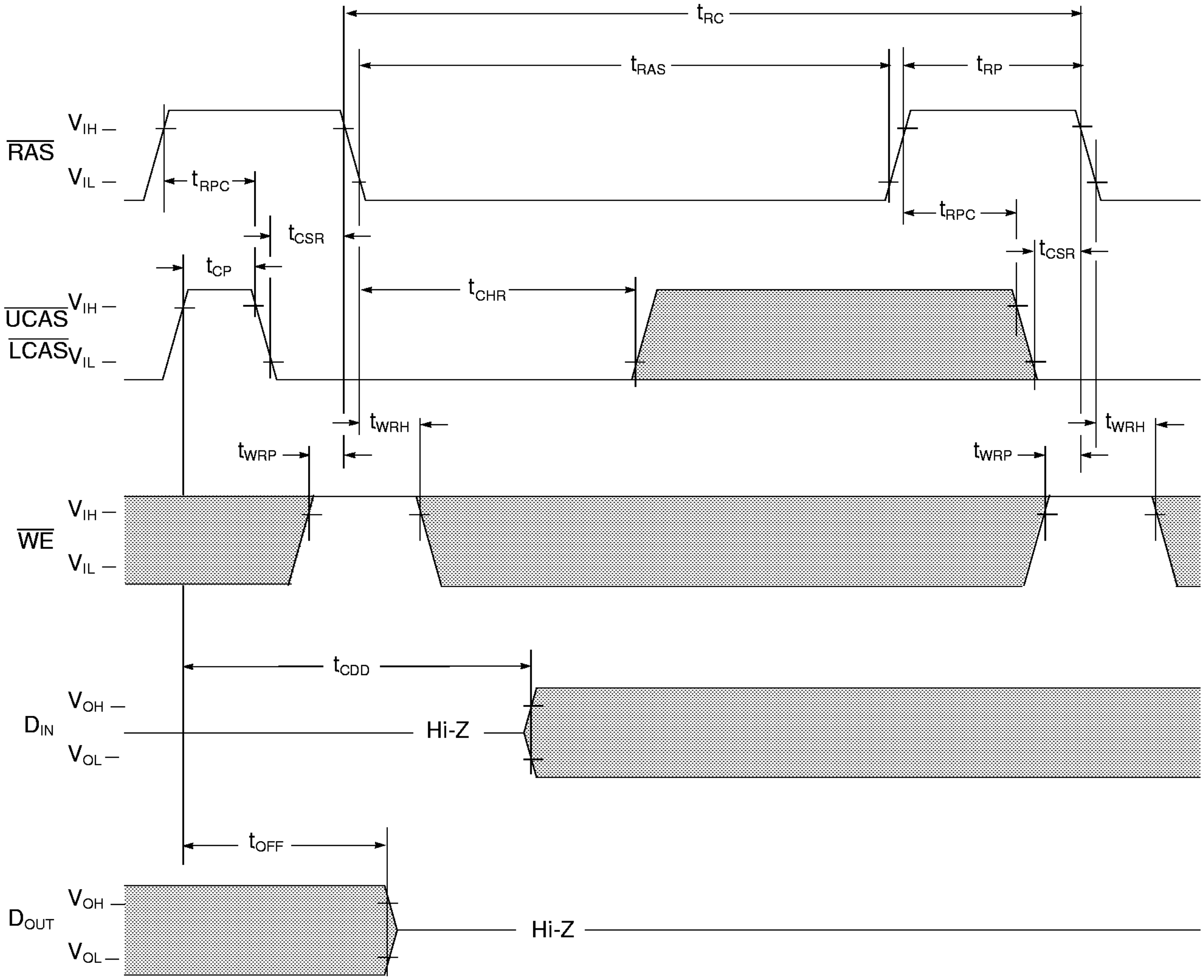
$\overline{\text{RAS}}$ Only Refresh Cycle



▨ : “H” or “L”

Note: $\overline{\text{WE}}$, D_{IN} are “H” or “L”

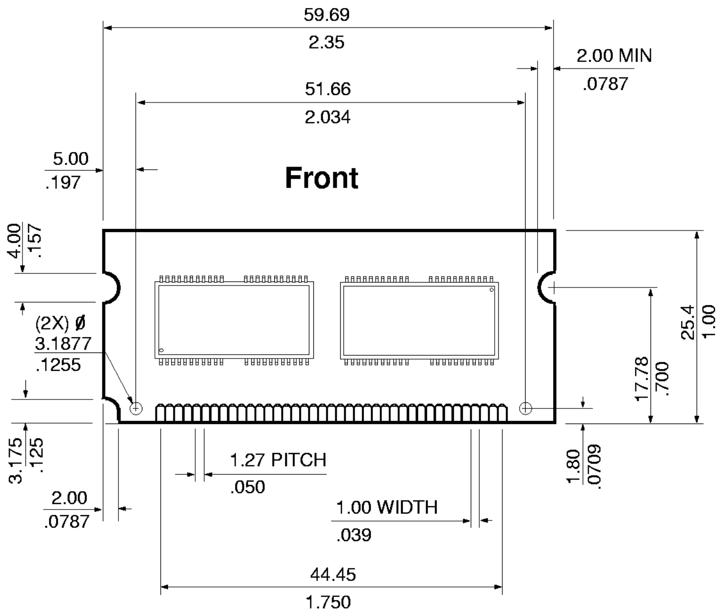
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

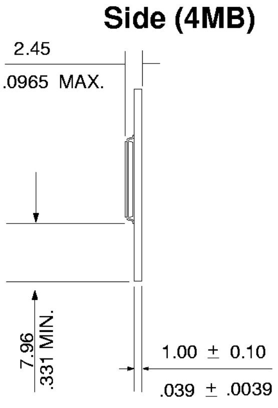


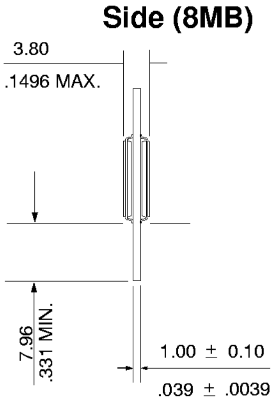
▨ : “H” or “L”

NOTE: Address is “H” or “L”

Layout Drawing







Note: All dimensions are typical unless otherwise stated.

$\frac{\text{Millimeters}}{\text{Inches}}$

Revision Log

Rev	Contents of Modification
4/96	Initial release of combined spec for 1M x 32, 2M x 32. Includes -6R speed sort offering. (originally released as spec #'s 50H4742 and 50H4743)
6/97	Removal of 5.0V, -6Rns, and 70ns parts from this specification $\overline{\text{WE}}$ for Hidden Refresh Write Cycle in the Truth Table was changed Updated currents/power based on DRAM Die Revision

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