T-46-23-12

MATRA M H S

September 1990

DATA SHEET

HM 65764

8 k x 8
HIGH SPEED CMOS SRAM

4

FEATURES

- **FAST ACCESS TIME**
  INDUSTRIAL/MILITARY : 35/45/55 ns (max)
  COMMERCIAL : 15*/20/25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 380 mW (typ)
  STANDBY : 110mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO 125°C
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

DESCRIPTION

The HM 65764 is a high speed CMOS static RAM organized as 8192x8 bits. It is manufactured using MHS high performance CMOS technology.
Access times as fast as 15 ns are available with maximum power consumption of only 550 mW.
The HM 65764 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 73 % when the circuit is deselected.

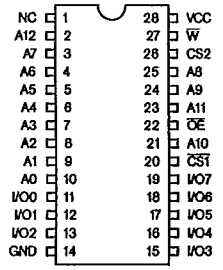
Easy memory expansion is provided by active low chip select (CS1), an active high chip select (CS2), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65764 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65764 is processed following the test methods of MIL STD 883C.

PACKAGES

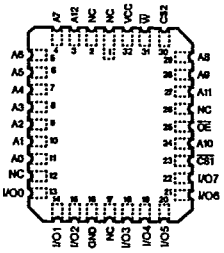
Plastic 300 & 600 mil, 28 pins, DIL.
Ceramic 300 mils, 600 mils, 28 pins, DIL

SOIC & SOJ 300 mils, 28 pins, DIL.
SOIC 330 mils, 28 pins
LCC 32 pins.

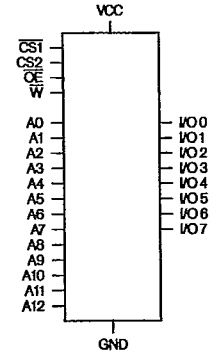
Pinout DIL 28 pins (top view)



Pinout LCC 32 pins (top view)



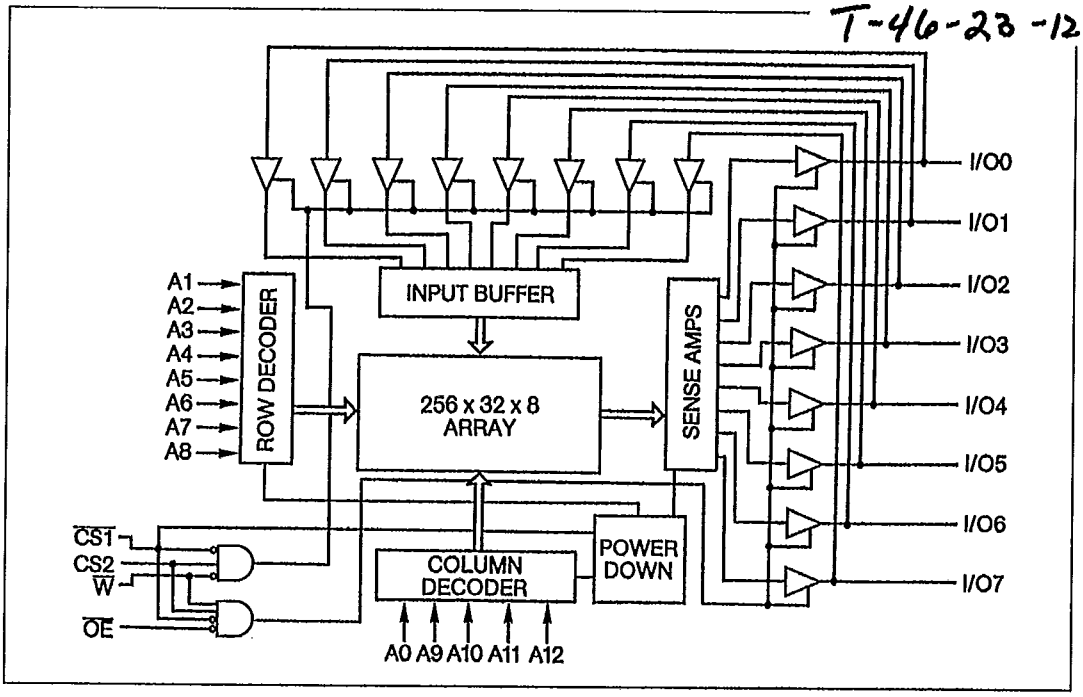
LOGIC SYMBOL



BLOCK DIAGRAM

MATRA M H S

T-46-23-12



4

PIN NAMES

A0-A13 : Address inputs	$\overline{CS1}$: Chip Select 1
I/O0-I/O7 : Inputs/Outputs	CS2 : Chip Select 2
VCC : Power	$\overline{OE}$: Output enable
GND : Ground	$\overline{W}$: Write enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable

L = low - H = high - X = H or L-Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V
Storage temperature : – 65°C to + 150°C

Output current into outputs (low) : 20 mA
Electro static discharge voltage : > 2000 V (MIL STD 883C method 3015.2)

T-46-23-12

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

4

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C - f = 1 MHz - Vcc = 5.0 V, these parameters are not tested.

AC TEST LOADS WAVEFORMS

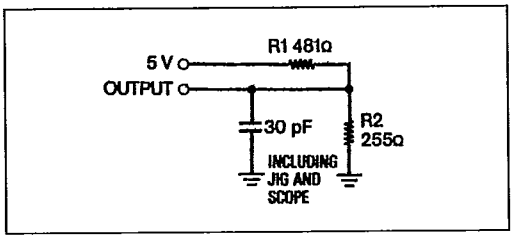


Fig. 1a.

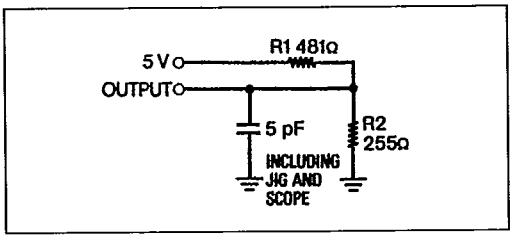
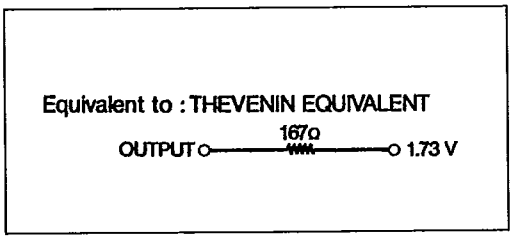


Fig. 1b.



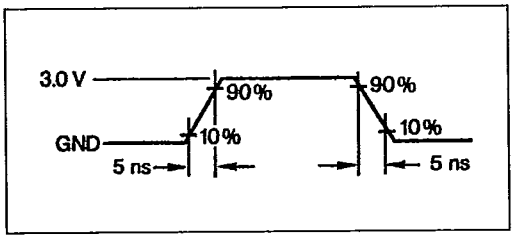


Fig. 2

T-46-23-12

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(3)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 300.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = – 4.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65764 E-5*	65764 F-5	65764 H-5	65764 K-5	65764 M-5	65764 N-5	UNIT	VALUE
ICCSB	(6)	Standby supply current	40	40	30	30	30	30	mA	max
ICCSB1	(7)	Standby supply current	20	20	20	20	20	20	mA	max
ICCOP	(8)	Dynamic operating current	135	125	125	125	125	125	mA	max

Consumption for Industrial (– 9) and Military specification (2) :

SYMBOL		PARAMETER	65764 H-9/2	65764 K-9/2	65764 M-9/2	65764 N-9/2	UNIT	VALUE
ICCSB	(6)	Standby supply current	40	30	30	30	mA	max
ICCSB1	(7)	Standby supply current	20	20	20	20	mA	max
ICCOP	(8)	Operating supply current	125	125	125	125	mA	max

Notes : 6. $\overline{CS1} \geq VIH$, $CS2 \leq VIL$ min duty cycle = 100 %, a pull-up resistor to VCC on the $\overline{CS}$ is required to keep the device unselected during Vcc power-up. Otherwise IccSB will exceed above values.
7. $\overline{CS1} \geq Vcc - 0.3\ V$ $CS2 < 0.3\ V$ Iout = 0 mA.
8. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
* Preliminary.

T-46-23-12

ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 10 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH (see figure 1 and 1b) : + 30 pF

WRITE CYCLE : Commercial specification

SYMBOL	PARAMETER	65764 E-5*	65764 F-5	65764 H-5	65764 K-5	65764 M-5	65764 N-5	UNIT	VALUE
TAVAV	Write cycle time	15	20	20	25	40	50	ns	min
TAVWL	Address set-up time	0	0	0	0	0	0	ns	min
TAVWH	Address valid to end of write	10	15	20	25	30	40	ns	min
TDVWH	Data set-up time	8	10	10	15	15	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	10	15	20	25	30	40	ns	min
TEH2WH	CS2 high to write end	10	15	20	20	25	30	ns	min
TWLQZ (9)	Write low to high Z	7	7	7	10	15	20	ns	max
TWLWH	Write pulse width	10	15	25	20	20	25	ns	min
TWHAX	Address hold from end of write	0	0	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	0	0	ns	min
TWHQX (8, 9)	Write high to low Z	3	5	5	5	5	5	ns	min

* Preliminary.

WRITE CYCLE : Industrial and Military specification

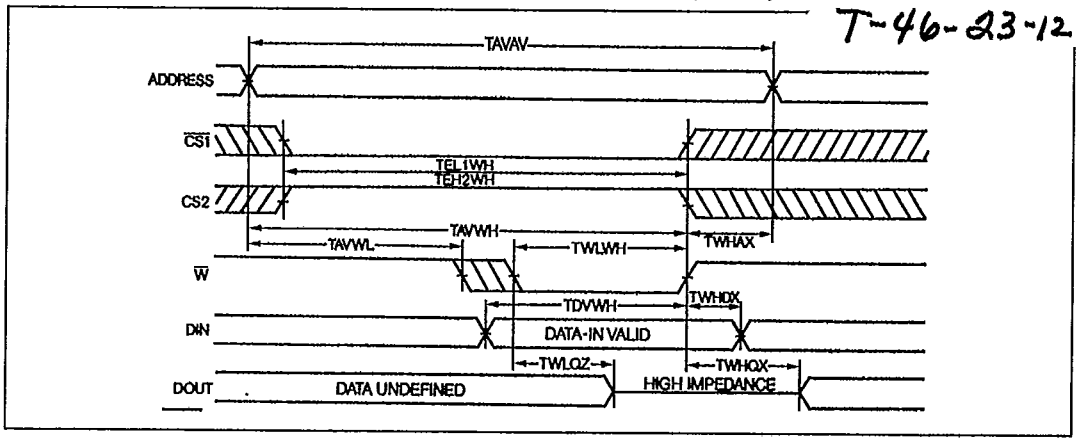
SYMBOL	PARAMETER	65764 H-9/-2	65764 K-9/-2	65764 M-9/-2	65764 N-9/-2	UNIT	VALUE
TAVAV	Write cycle time	20	25	40	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	25	30	40	ns	min
TDVWH	Data set-up time	10	15	15	25	ns	min
TEL1WH	$\overline{CS1}$ low to write end	20	25	30	40	ns	min
TEH2WH	CS2 high to write end	20	20	25	30	ns	min
TWLQZ (8)	Write low to high Z	7	10	15	20	ns	max
TWLWH	Write pulse width	25	20	20	25	ns	min
TWHAX	Address hold to end from write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8, 9)	Write high to low Z	5	5	5	5	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

4

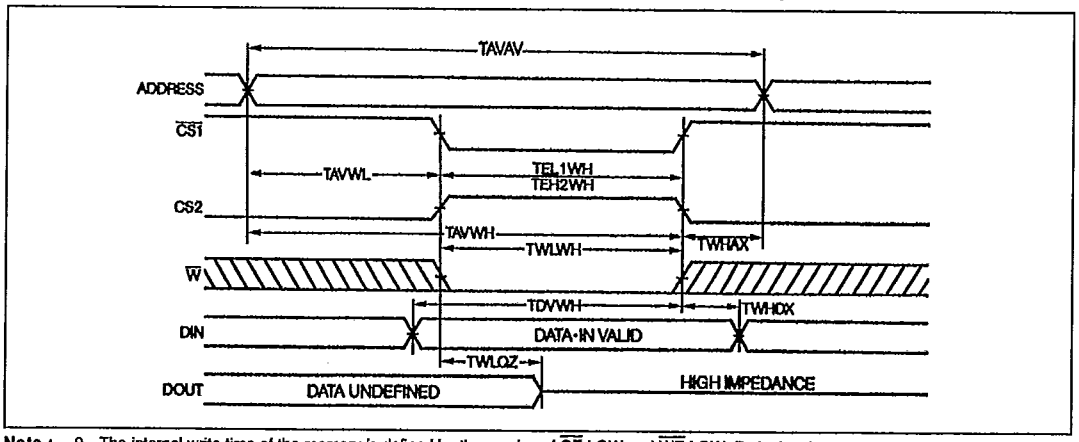
T-46-23-12

WRITE CYCLE 1 $\overline{W}$ CONTROLLED (note 9)



4

WRITE CYCLE 2 $\overline{CS1}$ CONTROLLED (note 9)



Note : 9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write. Data out is HIGH impedance if $\overline{OE}$ = VIH.

READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65764 E-5*	65764 F-5	65764 H-5	65764 K-5	65764 M-5	65764 N-5	UNIT	VALUE
TAVAV	READ cycle time	15	20	25	35	45	55	ns	min
TAVQV	Address access time	15	20	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	15	20	25	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	15	20	25	25	30	40	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	3	5	5	5	5	5	ns	min
TEH2QX	CS2 high to high Z	3	3	3	3	3	3	ns	min
TEH1QZ (11)	$\overline{CS1}$ high to high Z	8	8	10	15	15	20	ns	max
TEL2QZ (11)	CS2 low to high Z	8	8	10	15	15	20	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	0	0	0	ns	min
TEL1ICCL	CS1 high to power down	15	20	20	20	25	25	ns	max
TGLQV	Output enable access time	10	10	12	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	8	8	10	12	15	20	ns	max

* Preliminary.

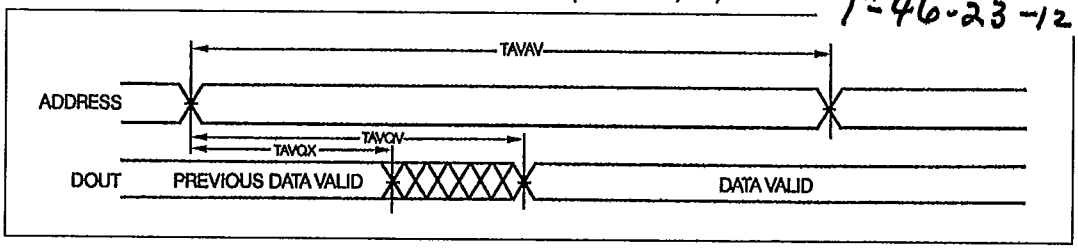
READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65764 H-9/-2	65764 K-9/-2	65764 M-9/-2	65764 N-9/-2	UNIT	VALUE
TAVAV	READ cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TEL1QV	Chip-select 1 access time	25	35	45	55	ns	max
TEH2QV	Chip-select 2 access time	25	25	30	40	ns	max
TEL1QX	$\overline{CS1}$ low to low Z	5	5	5	5	ns	min
TEH2QX	CS2 high to high Z	3	3	3	3	ns	min
TEH1QZ (11)	$\overline{CS1}$ high to high Z	10	15	15	20	ns	max
TEL2QZ (11)	CS2 high to high Z	10	15	15	20	ns	max
TEL1IC	$\overline{CS1}$ low to power up	0	0	0	0	ns	min
TEH1ICCL	CS1 high to power down	20	20	25	25	ns	max
TGLQV	Output enable access time	12	15	20	25	ns	max
TGLQX	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ	$\overline{OE}$ high to high Z	10	12	15	20	ns	min

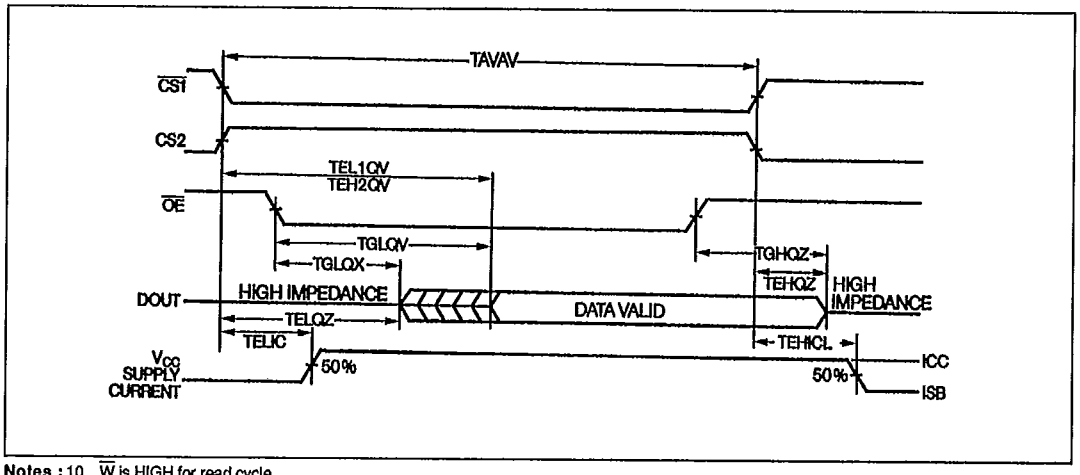
4

T-46-23-12

READ CYCLE nb 1 (notes 10, 11)



READ CYCLE nb 2 (notes 10, 12)



Notes : 10. $\overline{W}$ is HIGH for read cycle.
11. Device is continuously selected. $\overline{CS_1}$ & $\overline{OE}$ = VIL and CS_2 = VIH.
12. Address valid prior to or coincident with CS transition LOW.

T-46-23-12

ORDERING INFORMATION

Package	Device type	Grade	Level
HM1	65764	H	–5 : R

0 - Chip form
1 - Ceramic 28 pins 300 mils
1E - Ceramic 28 pins 600 mils
3 - Plastic 28 pins 300 mils
3E - Plastic 28 pins 600 mils
4 - LCC 32 pins
T - SOIC 28 pins 300 mils
TP - SOIC 28 pins 330 mils
U - SOJ 28 pins

8 k x 4 High speed static RAM

E* = 15 ns
F = 20 ns
H = 25 ns
K = 35 ns
M = 45 ns
N = 55 ns

–5 : Commercial
–9 : Industrial
–2 : Military
–8 : Military with B.I.
(B.I. = Burn-In)

Tape and Reel Service

* Preliminary

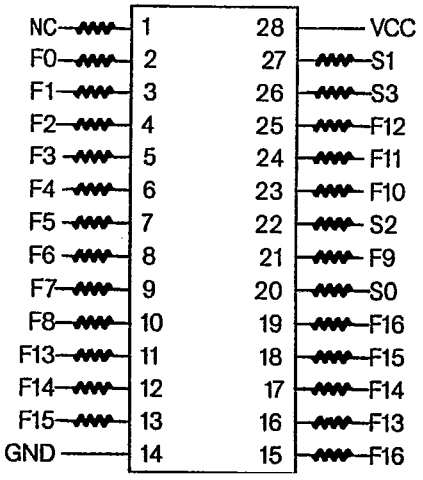
4

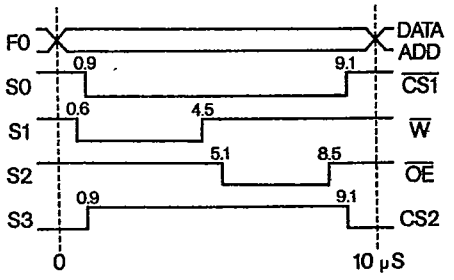
PACKAGE OUTLINE

For the package information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 28 pins
Plastic DIL, 600 mils, 28 pins
SOIC DIL, 300 mils, 28 pins
Ceramic, 300 mils, 28 pins
LCC rectangular, 32 pins

BURN-IN SCHEMATICS





VCC = 5 V (– 0, + 0.5)
R = 1 KΩ per pin
FO = 50 KHz ± 20 %

Fn = 1/2 F n-1
S0 to S3 : programmable signals for write / read cycles
NC = Not connected