CL-MD562X/MD342X

Preliminary Data Book

FEATURES

- **Complete PC telephony solution**
  - — Up to 56-kbps receive data rates (CL-MD562X only)
  - — Highly integrated two- or three-chip set
  - — Host-based controller
  - — PCI (Peripheral Component Interconnect) 2.1-compliant
  - — Future versions include ACPI (advanced configuration power interface) power management
  - — Exceeds Microsoft® PC 97 requirements
  - — Microsoft® Windows® TAPI-compliant
  - — Full-duplex, echo-cancelled digital speakerphone
- **Data modulation**
  - — 3Com® x2™ Technology (software-upgradable to ITU-V.90)
  - — ITU-V.34 (33.6 to 2.4 kbps) symmetric and asymmetric operation (CL-MD342X and CL-MD562X)
  - — ITU V.32 bis, V.23, V.22 bis, V.21
  - — Bell® 212A and 103
- **Fax modulation**
  - — ITU-T V.17, V.29 to 14.4 kbps
- **Voice telephony**
  - — Full-duplex, echo-cancelled digital speakerphone
  - — IS-101 voice commands
  - — Telephone emulation for headset applications
  - — ITU-V.80 videoconferencing future upgrade option
  - — ITU-V.70 future DSVD (digital simultaneous voice and data) upgrade option

(cont.)

56K/V.34 FastPath™ Data/Fax/Voice Controllerless Modems

OVERVIEW

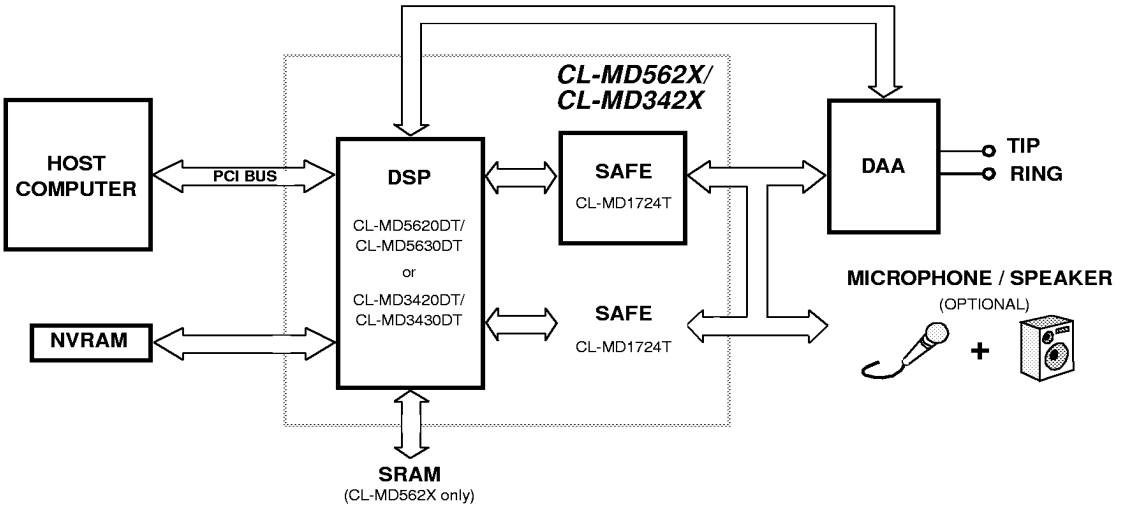
The CL-MD562X is the industry's first x2™ controllerless modem chipset featuring an integrated PCI (peripheral component interconnect) interface. This V.90-upgradable 56K solution uses the 3Com® x2 Technology to receive data at rates of up to 53.333 kbps. The V.34 version of the chip, the CL-MD342X, receives and sends data at 33.6 kbps. Both chipset families provide a complete set of industry-standard voice, data, and fax features, plus extras that include full-duplex speakerphone and simultaneous voice and data operation.

Integrated PCI Interface

The CL-MD562X/MD342X chipsets are based on the FastPath platform, a proprietary high-bandwidth DSP (digital signal processor). The integrated PCI interface allows the device to transfer data from the DSP to the host system's CPU faster than current ISA-based 56K solutions. The integrated PCI interface also eliminates

(cont.)

System Block Diagram



FEATURES (cont.)

- **Voice coder**
  - — Voice compression: 3- and 4- bit ADPCM and CL1 (linear)
  - — 4800, 7200, 8000, 9600, and 11025 samples per second
- **Data link layer protocols**
  - — Error correction: ITU V.42 and MNP® 2–4
  - — Data compression: ITU V.42 bis and MNP® 5
- **DTE integrated interface alternatives**
  - — PCI 2.1-compliant
- **Host-based controller**
  - — Fax Class 1 commands
  - — Voice IS-101 commands
- **Minimal-component design**
  - — Direct connection to PCI bus
  - — Single crystal
  - — Passive hybrid
- **Low power requirements**
  - — Single +5-V power source; 3.3-V DSP
  - — Automatic sleep and wake-up modes
- **Small package options**
  - — DSP: 160-pin PQFP or 176-pin VQFP
  - — SAFE: 44-pin VQFP

OVERVIEW (cont.)

the ISA bridge chip requirement, thus reducing the chip count, board space, and cost. The FastPath platform's scalability allows the addition of computer telephony features such as speakerphone and telephone emulation and the future addition of DSVD and ACPI power management. The CL-MD562X/MD342X chipset families exceed Microsoft® PC 97 specifications for Windows®, and they are TAPI- and PCI 2.1-compliant.

Satisfies Legacy Applications

The CL-MD562X/MD342X chipsets support all requirements for PC-based communications. With the FastPath platform's robust host-based controller software and powerful DSP, the chipsets support all industry-standard AT commands for data, IS-101 voice, and Class 1 fax.

Versatile 56K Platform

The CL-MD562X chipsets offer data receive speeds of up to 56 kbps using 3Com x2 Technology, although Federal Communications Commission power restrictions limit actual receive speeds to 53.333 kbps. The CL-MD562X will support the ITU-V.90 standard. Products can be designed for complete software upgradability.

Comprehensive Telephony Features

Voice telephony is becoming increasingly important in modem-based products. The FastPath platform has a complete telephony interface (including Caller ID and voice mail), telephone emulation, and answering machine capabilities (including tone generation and detection and call progress control). The DSVD future upgrade option enables realtime data transfer during a voice conversation, an essential for whiteboard applications and sophisticated customer support. Additionally, the CL-MD562X/MD342X's full-duplex, echo-cancelled digital speakerphone offers the latest technology for hands-free computer telephony. The speakerphone operates in all modes, including DSVD. All voice features are fully compliant with Microsoft's Unimodem V and TAPI standards, and all voice commands comply with IS-101 voice command standards.

International Telephony Support

CL-MD562X/MD342X chipsets support international applications. Cirrus Logic also provides international DAA design recommendations.

Platform of the Future

The CL-MD562X/MD342X chipset families are a solid base for future innovation. The controller code is open for modification in a C code development environment.

The DSP delivers the bandwidth to handle multiple tasks simultaneously and to support specialized functions. Many advanced features are already built in, including a full-duplex, echo-cancelled speakerphone. Concurrent operation is enabled for even the most advanced features, such as Voice Call First videoconferencing and full-duplex speakerphone operation in DSVD mode. Other built-in features are call progress and tone generation, including DTMF, calling tone, and Caller ID. Tones can be tailored to special requirements.

AT COMMAND CHANGES

The following changes were made to Section 5 on page 22 of the previous version of this data book, the *CL-MD56XXT Preliminary Data Book* version 0.5, July 1997.

Table	Command
Table 5-1, "Data Mode Command Summary," on page 23	The following commands were removed: **Bn**, **Nn**, **&M**, **&Q**, **&T4–&T8** The following commands were changed: **-Cn** default changed to 0 from 1 **%Gn** default changed to 1 from 0 Moved **+A8E** and **+ES** here from V.80 table Added **C3**
Table 5-2, "V.42 / V.42 bis MNP® AT Commands," on page 28	The following commands were removed: **\Bn**, **\Kn**, **\Nn**, **\O**, **\Qn**, **\U**, **\Y**, **\Z**
Table 5-4, "Fax Class 1 Command Summary," on page 29	Removed **+FAE**
Table 5-5, "IS-101 Voice Command Summary," on page 30	Removed **#VCSD** Changed default for **#VSPS** to 1 from manufacturer-specified
Table 5-6, "Voice DTE→DCE Character Pairs," on page 31	Removed **<FS>** Changed ~ to **<DEL>**, hex code 7F
Table 5-6, "Voice DTE←DCE Character Pairs," on page 31	Removed the following character pairs: **I**, **L**, **P**, **p**, **% ' , ( )**
VoiceView™ command and response code tables	Removed tables — VoiceView now a future upgrade option
V.80 Videoconferencing table	Removed table — V.80 videoconferencing now a future upgrade option
Table 5-9, "S-Register Summary," on page 33	Removed **S37;** changed default for **S23** to 31 from none.
Table 5-10, "DTE-Modem Data Rate Response Codes," on page 34	Changed response codes
Table 5-8, "Manufacturing-Only Command Summary," on page 32	The following commands were removed: **%L**, **-Tn** Changed range for **S91** to 9-16 from 10-15

OTHER REVISIONS

The following other changes were made to the previous version of this data book, the *CL-MD56XXT Preliminary Data Book* version 0.5, July 1997.

Section	Section Title	Revision
Section 1.1 on page 11	"Functional Block Diagrams"	The SAFE part number is 1724T, not 1724DT.
Table 3-3 on page 18	"Communication Modes and Data Rates"	Corrected the number of constellation points for V.21 fax mode, V.21 data mode, and Bell 103 data mode.
Section 3.5 on page 14	"ACPI"	Explains the advanced configuration power interface feature to be added in future chip versions.
Section 3.7 on page 15	"Videoconferencing (V.80) Support"	ITU-V.80 videoconferencing now a future upgrade option.
Section 7.1 on page 40	"DSP Pin Descriptions"	1. Changed the DSP pin 36 (160-pin PQFP) and pin 38 (176-pin VQFP) from Reserved to No Connect. 2. Changed the DSP pin 117 (160-pin PQFP) and pin 128 (176-pin VQFP) from GPI15/RING* to RING*.
Section 6.3 on page 39	"SAFE 44-pin VQFP Pin Diagram"	Changed the SAFE pin 26 from RXENA to No Connect.
Section 8.3 on page 48	"DSP 3.3-V Power Consumption"	Added power consumption numbers for selected modes.
Table 8-7 on page 54	"DSP Expansion Bus Timing Diagram — Write Cycle"	Added timing diagram.
Table 8-8 on page 55	"DSP Expansion Bus Timing Diagram — Read Cycle"	Added timing diagram.

CONVENTIONS

This section lists conventions used in this data book.

Abbreviations

Symbol	Units of measure
°C	degree Celsius
µF	microfarad
µs	microsecond (1,000 nanoseconds)
Hz	hertz (cycle per second)
K (memory)	kilobit (1,024 bits)
kbits/second	kilobit (1,000 bits) per second
kHz	kilohertz
kΩ	kilohm
Mbyte (memory)	megabyte (1,048,576 bytes)
MHz	megahertz (1,000 kilohertz)
mA	milliampere
ms	millisecond (1,000 microseconds)
ns	nanosecond
pV	picovolt
V	volt
W	watt

Acronyms

Acronym	Definition
AC	alternating current
AT	'Attention' command prefix for Hayes AT® command set (for example, 'ATDT 123')
CMOS	complementary metal-oxide semiconductor
DC	direct current
DAA	data access arrangement
DRAM	dynamic random-access memory
DSVD	digital simultaneous voice and data
EPROM	electrically programmable read-only memory
FIFO	first in/first out
HDLC	high-level data link control
ISA	industry-standard architecture
ITU-T	International Telecommunications Union — Telecommunications
LSB	least-significant bit
MSB	most-significant bit
NVRAM	non-volatile random-access memory
PCI	peripheral component interconnect
RAM	random-access memory
ROM	read-only memory
R/W	read/write
SQFP	shrink quad flat pack
SRAM	static random-access memory
TAPI	telephony application program interface
TTL	transistor-transistor logic
UART	universal asynchronous receiver transmitter
VQFP	very-tight-pitch quad flat pack

Notes

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APPENDIXES

LIST OF FIGURES

LIST OF TABLES

1. AVAILABLE 56K AND V.34 CHIPSETS

Features	CL-MD562X	CL-MD342X
Data/fax voice	CL-MD5620T DSP CL-MD5620DT SAFE CL-MD1724T	CL-MD3420T DSP CL-MD3420DT SAFE CL-MD1724T
Data/fax voice, full-duplex speakerphone	CL-MD5622T DSP CL-MD5620DT SAFE CL-MD1724T SAFE CL-MD1724T	CL-MD3422T DSP CL-MD3420DT SAFE CL-MD1724T SAFE CL-MD1724T
Data/fax voice, full-duplex speakerphone, future DSVD upgrade option	CL-MD5632T DSP CL-MD5630DT SAFE CL-MD1724T SAFE CL-MD1724T	CL-MD3432T DSP CL-MD3430DT SAFE CL-MD1724T SAFE CL-MD1724T

Figure 1-1. CL-MD562X/MD342X Family Chipset Composition

1.1 Functional Block Diagrams

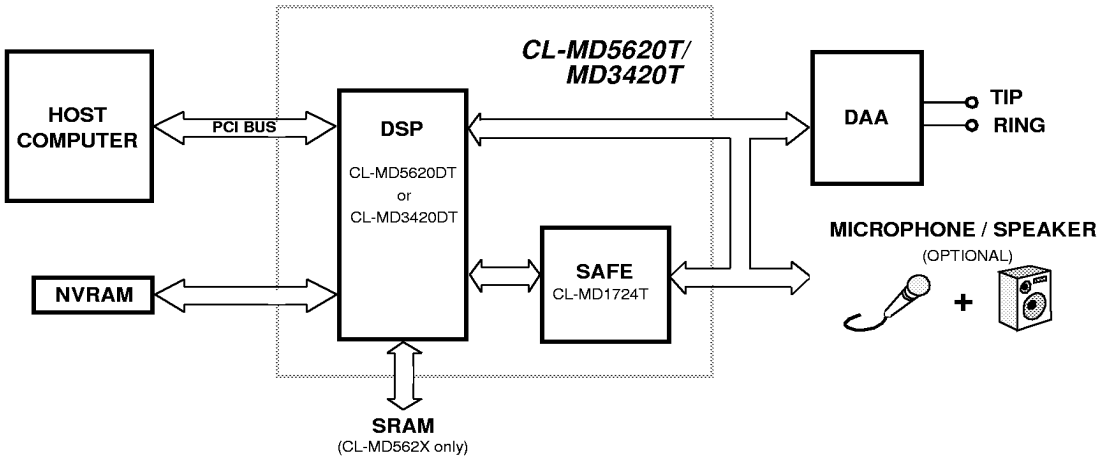

Figure 1-2. CL-MD5620T Functional Block Diagram

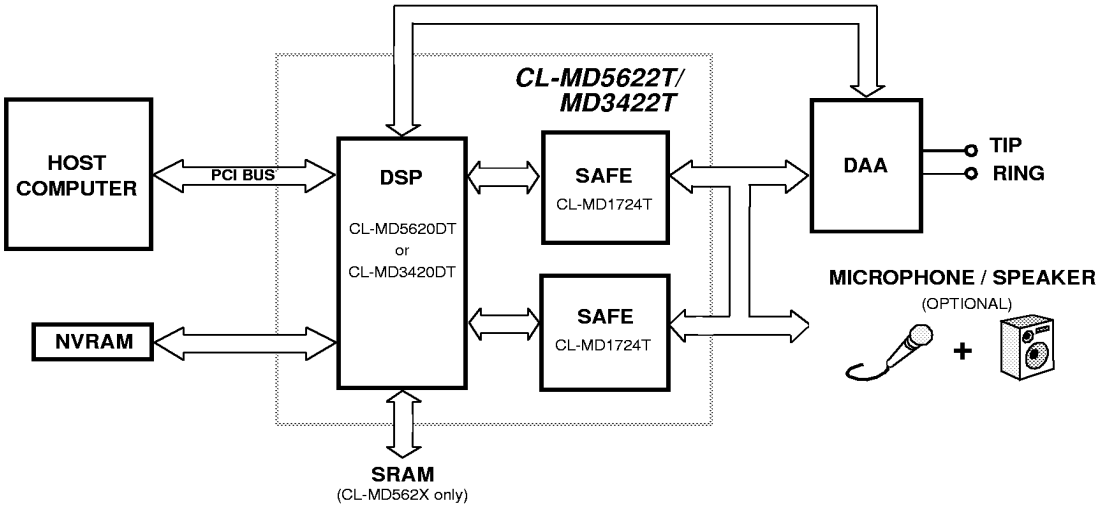

Figure 1-3. CL-MD5622T/MD3422T Functional Block Diagram

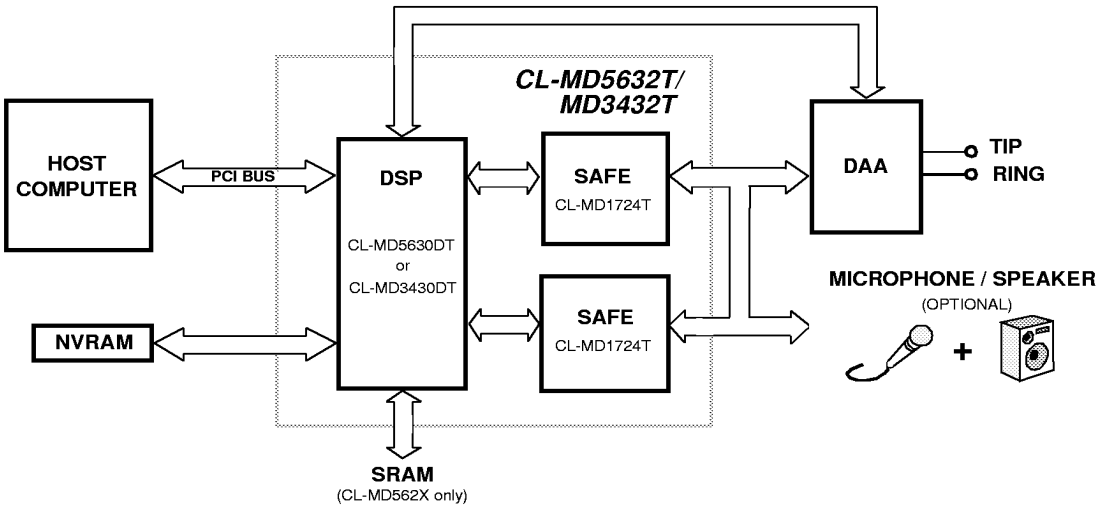

Figure 1-4. CL-MD5632T/MD3432T Functional Block Diagram

2. CHIPSET DESCRIPTIONS

The CL-MD562X/MD342X chipsets are two- or three-chip controllerless modems consisting of a DSP (digital signal processor), and one or two SAFE (sigma-delta analog front end) devices. These products support a variety of applications and need no additional firmware development. Currently, there are three chipset solutions. These are shown in Figure 1-1 on page 11 with their corresponding DSP and SAFE device part numbers.

2.1 Host Controller Software

The host-based controller software contains code for all controller functions for Group 3 Fax mode, Data mode (including error correction and data compression), and Voice mode.

2.2 Digital Signal Processor

The digital signal processor (DSP) performs all digital signal processing functions for the chipset, including modulation, echo cancellation, call progress monitoring, and voice processing.

The DSP requires a 3.3-V power supply, which takes advantage of the latest manufacturing technologies. The PCI bus accommodates either 5-V or 3.3-V designs. The 3.3-V DSP not only reduces power consumption, it also enables the concurrent operation of speakerphone and DSVD using a single DSP.

2.3 Sigma-Delta Analog Front End Device

The SAFE device uses sigma-delta techniques to convert analog information from a telephone line to digital information that can be processed by the DSP. In addition to its analog circuitry, the modem's sigma-delta function incorporates unique and proprietary digital-to-analog and analog-to-digital features. These features improve receiver accuracy, which in turn improves performance at low levels of receive signal.

Compared to other analog front-end technologies, the sigma-delta implementation better stabilizes the function of the SAFE devices and makes them less sensitive to board layout than other analog front end technologies. Since a significant amount of signal processing is performed by digital rather than analog techniques, sigma-delta analog-to-digital conversion considerably improves signal quality.

For basic Data, Fax, and Voice modes of operation, a single SAFE device is needed. To support DSVD or full-duplex speakerphone with echo cancellation, a second SAFE device is required.

The SAFEs require a 5-V power supply; however, the interface is 3.3-V–capable.

3. MODES OF OPERATION

The CL-MD562X/MD342X chipset families provide complete modem functions for the following modes: Group 3 Fax, Data, Voice, V.42/MNP 2–4, and V.42 bis/MNP 5 (Microcom Networking Protocol Class 5). Each mode has its own unique AT command set. The data rates and modulation schemes for Data and Fax modes are presented in Table 3-3 on page 18. Additionally, special modes of operation exist for power management and loopback testing.

3.1 Data Mode

In Data mode, the CL-MD342X chipsets send and receive at 33.6 kbps. The CL-MD562X chipsets send at an effective rate of 33.6 kbps and receive at 53.333 kbps using x2 Technology or a V.90 upgrade. The 56K receive rates can be achieved only in connections with equipment-compatible ISPs (internet service providers). See Table 3-3 on page 18 for connection rates. Both chipset families implement all data rates and modulation schemes for ITU-T (International Telecommunications Union — Telecommunications) standards V.34, V.32 bis, V.32, V.22 bis, V.22, V.21, Bell 212A, and Bell 103. Both families implement a standard (TIES) Data mode AT command set, which is compatible with any communication application software that supports the Hayes® AT command set. See Table 5-1 on page 23 for Data mode commands.

3.2 V.42/MNP® 2–4 and V.42 bis/MNP® 5 Modes

The FastPath platform supports error correction (V.42/MNP 2–4) and data compression (V.42 bis/MNP 5). Error correction ensures error-free data transfer. Data compression substantially increases the modem data throughput over the basic data rate throughput. Depending on the data stream, MNP 5 can provide compression ratios of up to two-to-one. Alternately, ITU-T V.42 bis can provide up to four-to-one compression. A description of the AT commands that support error correction and data compression are provided in Table 5-2 on page 28.

3.3 Fax Mode

In Fax mode, the FastPath chipsets operate at up to 14.4 kbps (transmit and receive) and implement all the data rates and modulation schemes for ITU-T standards V.17, V.29, V.27 ter, and V.21 ch2. The chipsets implement a standard Fax mode AT command set compatible with any communication application software that supports EIA/TIA-578 Fax Class 1 standards. The standard AT commands for Fax mode are listed in Table 5-3 and Table 5-4 on page 29.

3.4 Voice Mode

All chipsets support Telephone-Emulation mode, IS-101 voice commands, and record and playback message capabilities. Telephone-Emulation mode allows a handset/microphone-speaker and modem to be used as a complete telephone. In Telephone-Emulation mode, the received data from the SAFE (CL-MD1724T) microphone interface is looped back to the SAFE analog transmit pins. In Voice mode, the message record and playback abilities are accessed by the extended AT command set, shown in Table 5-5 on page 30 through Table 5-6 on page 31.

3.5 ACPI

Future versions of the CL-MD562X/MD342X chipsets will support the ACPI (advanced configuration power interface) power management specification, where the operating system puts system components

into low-power states when not active. The chipsets support three power modes: D0, a fully active power mode; D2, a low-power mode where the modem chipset answers calls and saves all Caller ID information and data downloads received; and D3, a low-power mode similar to D2 except that no information can be sent over the PCI interface.

3.6 DSVD

DSVD (digital simultaneous voice and data) allows data to be transferred realtime during a voice conversation. This future ITU-V.70 DSVD upgrade option can be used for interactive applications such as whiteboard conferencing or realtime action games. DSVD is transparent to the application software.

3.7 Videoconferencing (V.80) Support

All versions of the CL-MD562X/MD342X chipset families will support the ITU-V.80 recommendation. This future upgrade option ensures compatibility with host-based H.324 videoconferencing application software. The CL-MD562X/MD342X chipsets will support both transparent and framed submodes of the V.80 synchronous access mode, plus Voice Call First and full-duplex speakerphone.

3.8 Full-Duplex Speakerphone

The CL-MD562X/MD342X support full-duplex speakerphone with internal adaptive echo cancellation. Phone users can talk simultaneously without the remote user hearing an echo. This speakerphone feature also is supported by DSVD.

3.9 Power Management Modes

The CL-MD562X/MD342X families provide both Sleep and Stop modes to reduce power consumption when the modem is inactive. Stop mode turns off all modem power except for the circuitry needed to maintain the host interface signals at the appropriate high-impedance state. To enter Stop mode, the host asserts the STOP* pin. When the STOP* pin is deasserted, the modem exits Stop mode, performs an internal reset, and enters Power-on mode. After the modem internal reset, the DTE reconfigures the modem.

Power-on mode consists of an Operational mode and a Sleep (or power-down) mode. In Operational mode, the modem chipset is fully powered and is either communicating with the host and/or another modem or is performing internal processing. In Sleep mode, power is turned off to most of the internal circuitry of the DSP and SAFE. Sleep mode is controlled by S-register **S33**. When enabled, the modem enters Sleep or Power-down mode whenever the modem has been inactive for a user-programmable time delay.

The modem is considered to be in an inactive state when:

1) No internal processing is being performed;
2) No activity occurs between the host and the modem within a specified time period (S-register **S33**); or
3) The modem is on-hook.

The modem exits Sleep mode whenever the host writes to the modem or when a ring signal is detected. The modem does not wake up when the host reads the UART registers.

3.10 Loopback Test Modes

In all modes except x2, modem-to-DTE and modem-to-modem communication integrity can be tested with loopback tests. The **AT&T1** command initiates the local analog loopback test. For more information about loopback tests, see the controllerless modem programmer's guide.

3.11 Transmit Levels

The factory default transmit level for x2 and V.34 transmission is –10 dBm ±1 dB at Tip and Ring. Data and fax use separate transmission levels. The transmit level can be programmed using the international configuration utility.

IMPORTANT: Current download speeds are limited to 53.33 kbps due to FCC rules that restrict modem power output.

3.12 Transmit Tone Levels

The modem generates DTMF, answer, call, and guard tones. The specifications for each tone are provided in Table 3-1 and Table 3-2 on page 17. DTMF tones are transmitted at –6 dBm for Tone 1 and –4 dBm for Tone 2. The transmit level can be programmed using the Cirrus Logic configuration utility.

3.13 Receive Level

The receiver can accommodate a receive signal from –9 dBm to –43 dBm. The DCD (data carrier detect) function is activated at –43 dBm and above; it is deactivated at –48 dBm and below.

3.14 Receiver Tracking

The receiver compensates for up to ±7 Hz of carrier-frequency offset in V.34 mode.

3.15 Equalizers

Automatic adaptive and compromise equalizers are provided to compensate for line distortions.

3.16 Call Progress

The modem monitors the detection of call-progress tones during call origination and reports them to the DTE. Call-progress tones include dial, busy, ringback, and answer.

3.17 Caller ID

Caller ID is a service that allows the user to see the caller's telephone number and name. Caller ID also provides information on call date and time. For more information, refer to Appendix A of the controllerless modem programmer's guide.

3.18 International Support

The FastPath chipsets support international applications. For information on specific countries, contact your local Cirrus Logic sales office at the address listed on the back cover of this document.

Table 3-1. Transmit Tones

Tone	Value	Application
Calling tone	1100 Hz	Fax originator
	1300 Hz	Data originator
Answer tone	2100 Hz	Data/fax (ITU-T)
	2225 Hz	Data (Bell mode)
Guard tone	1800 Hz	Data/fax (answer mode)
	550 Hz	

Table 3-2. DTMF Tone Pairs

Dial Digit	Tone 1 (Hz)	Tone 2 (Hz)
0	941	1336
1	697	1209
2	697	1336
3	697	1447
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1447
*	941	1209
#	941	1447
A	697	1633
B	770	1633
C	852	1633
D	941	1633

Table 3-3. Communication Modes and Data Rates

Application	Mode	Data Rate (bps)	Modulation	Baud Rate (symbols/sec.)	Carrier Frequency (Hz) (originate/answer)	Constellation Points
Fax	V.17	14,400	TCM	2400	1800	128
		12,000	TCM	2400	1800	64
		9600	TCM	2400	1800	32
		7200	TCM	2400	1800	16
	V.29	9600	QAM	2400	1700	16
		7200	QAM	2400	1700	8
		4800	QAM	2400	1700	4
	V.27 ter	4800	DPSK	1600	1800	8
		2400	DPSK	1200	1800	4
	V.21	300	FSK	300	1650 M/1850 S	2
Data	x2™ Technology[a] (receive only)	57,333[b], 56,000[b], 54,666[b], 53,333, 52,000, 50,666, 49,333, 48,000, 46,666, 45,333, 44,000, 42,666, 41,333, 37,333, 33,333	PCM	8000	N/A	Variable[c]
	x2™ Technology[a] (transmit only)	31,200, 28,800, 26,400, 24,000, 21,600, 19,200, 16,800, 14,400, 12,000, 9600, 7200, 4800	TCM	3200	1920	Variable[c]
	V.34	33,600, 31,200, 28,800, 26,400, 24,000, 21,600, 19,200, 16,800, 14,400, 12,000, 9600, 7200, 4800, 2400	TCM	Variable[d]	Variable[e]	Variable[c]
	V.32 bis	14,400	TCM	2400	1800	128
		12,000	TCM	2400	1800	64
		9600	TCM	2400	1800	32
		7200	TCM	2400	1800	16
		4800	TCM	2400	1800	4
	V.32	9600	TCM	2400	1800	32
		9600	QAM	2400	1800	16
		4800	QAM	2400	1800	4
	V.22 bis	2400	QAM	600	1200/2400	16
	V.22	1200	DPSK	600	1200/2400	4
	V.21	300	FSK	300	980 M/1650 M 1180 S/1850 S	2
	Bell® 212A	1200	DPSK	600	1200/2400	4
	Bell® 103	300	FSK	300	1270 M/2225 M 1070 S/2025 S	2

[a] x2 Technology is a proprietary technology of 3Com® and licensed by Cirrus Logic. The x2 Technology data receive rates of up to 56 kbps can be achieved only in connections with equipment-compatible ISPs (internet service providers).

[b] FCC regulations do not allow the 57.333, 56, and 54.666 kbps data rates to be supported.

[c] Cirrus Logic supports the normal and expanded constellations for each baud and data rate.

[d] Cirrus Logic supports five of the six baud rates specified by the ITU-T (International Telecommunications Union-Telecommunications): 2400, 2743, 3000, 3200, and 3429 symbols/second. The ITU-T's optional baud rate of 2800 symbols/second is not supported.

[e] The high and low carrier frequencies specified by ITU-T are supported for each baud rate.

4. HARDWARE INTERFACES

The controllerless modems support hardware interfaces for the host, flash memory, expansion bus, NVRAM, DAA, speaker, microphone, and general-purpose I/O functions. The hardware interfaces are demonstrated in Figure 4-1.

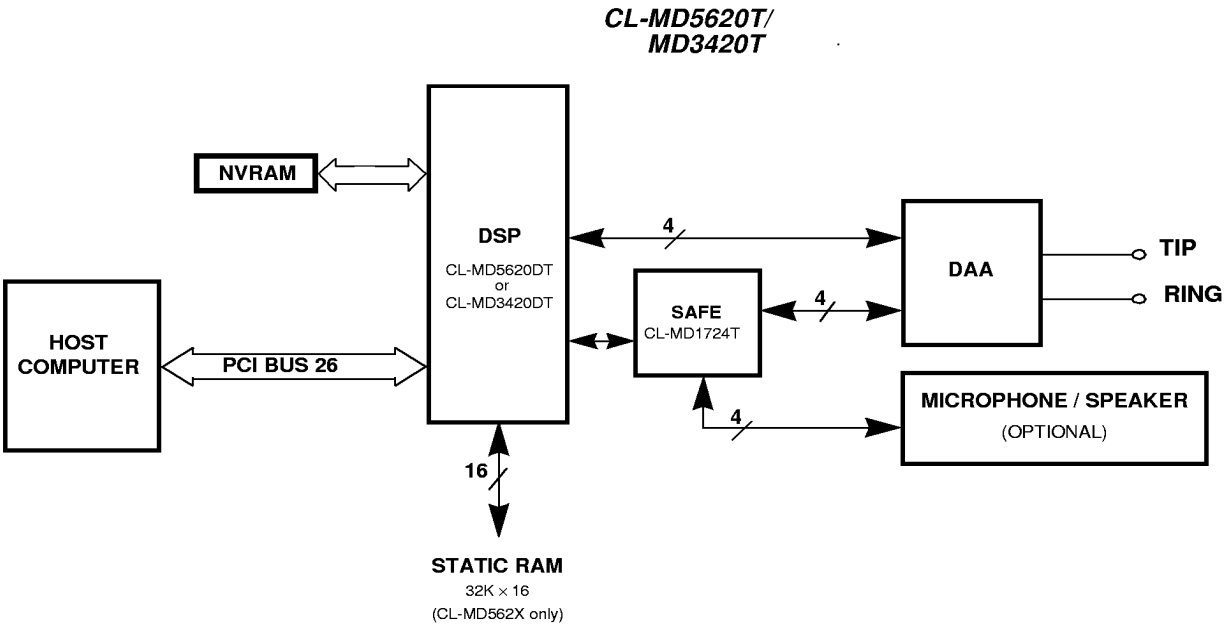

Figure 4-1. Modem System Block Diagram (CL-MD5620T/CL-MD3420T)

4.1 DSP Bus Interface

A 32K × 16 bit, 12-ns SRAM is required for CL-MD562X-based modems. The SRAM is used to store DSP code for the x2 mode. This SRAM is not required for the CL-MD342X chipset family.

4.2 NVRAM Interface

A serial interface is provided for the 2 K (× 8 configuration) non-volatile RAM (NVRAM). The NVRAM can be used for storing modem configurations. Plug-and-play designs can use NVRAM to store the board's serial number information.

4.3 DAA Interface

A DAA (Data Access Arrangement) is the interface between the modem chipset and the telephone network. The DAA interface controls the telephone line off-hook relays, detects ring signals, and transmits and receives analog signals.

4.4 Speaker Interface

The SAFE device internally implements both the volume control and amplifier necessary to drive an external speaker. The output of the internal amplifier can be connected directly to a speaker or to the input of the host speaker amplifier. The internal amplifier is capable of driving a maximum load of 8 Ω. The speaker volume is controlled by the **ATLn** command.

4.5 Microphone Interface

The CL-MD1724T SAFE device provides a microphone interface that connects a microphone or handset to the modem with a minimum of external parts. This microphone input can then be used for local Voice record mode or for Telephone-Emulation mode.

4.6 General-Purpose I/O Interface

To customize the modem design, the DSP provides 16 general-purpose pins that can be used to control or monitor external circuitry.

Some of the general-purpose pins can be configured for specific functions (such as a Caller ID relay, CIDREL*). Pin functions can be controlled via the host controller code. Some Voice mode functions are enhanced by adding external circuitry for remote hang-up detection, extension phone pickup, or hang-up detection (see Table 5-6 on page 31).

3Com® x2™ Technology

The CL-MD562X modem chipsets are compliant with the 3Com® x2™ Technology standard.

General DataComm, Inc.

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Table 4-1. Parallel Host Interface UART Register Bit Assignments

REGISTER ADDRESS	REGISTER NAME	BIT NUMBER							
		7	6	5	4	3	2	1	0
7	Scratch Register (SCR)	Scratch Register (SCR)							
6	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCDD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
5	Line Status Register (LSR)	Error in RCVR FIFO (Note 1)	Transmitter Empty (TEMT)	Transmitter Holding Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
4	Modem Control Register (MCR)	0	0	0	Loop	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
3	Line Control Register (LCR)	Divisor Latch Access Bit (DLAB)	Set Break (SBRK)	Stick Parity (SPAR)	Even Parity Select (EPS)	Parity Enable (PEN)	Number of Stop Bits (STB)	Word Length Select Bit 1 (WLS1)	Word Length Select Bit 0 (WLS0)
2	FIFO Control Register [Write only] (FCR)	RCVR Trigger (MSB)	RCVR Trigger (LSB)	Reserved	Reserved	Reserved	XMIT FIFO Reset (XFIFOR)	RCVR FIFO Reset (RFIFOR)	FIFO Enable (FIFOE)
2	Interrupt Identity Register [Read only] (IIR)	FIFOs Enabled (See note)	FIFOs Enabled (See note)	0	0	Interrupt ID Bit 2 (See note)	Interrupt ID Bit 1	Interrupt ID Bit 0	'0' if Interrupt pending
1 DLAB=0	Interrupt Enable Register (IER)	0	0	0	0	Modem Status Interrupt Enable (MSIE)	Receiver Line Status Interrupt Enable (RLSIE)	Transmitter Holding Reg. Empty Int. Enable (THREIE)	Received Data Available Int. Enable (RDAIE)
0 DLAB=0	Transmit Holding Register [Write only] (THR)	Transmit Holding Register (THR) [Write only]							
0 DLAB=0	Receiver Buffer Register [Read only] (RBR)	Receiver Buffer Register (RBR) [Read only]							
1 DLAB=1	Divisor Latch (MS) (DLM)	Divisor Latch (MS)							
0 DLAB=1	Divisor Latch (LS) (DLL)	Divisor Latch (LS)							

NOTE: These bits are always '0' in 16C450 mode.

5. AT COMMAND SET

The CL-MD562X/MD342X's AT command set and S-registers are divided into four categories: Group 3 fax, data, V.42/MNP, and voice. Summaries of all commands are provided in Table 5-1 on page 23 through Table 5-10 on page 34. Table 5-9 on page 33 provides a summary of all S-registers.

5.1 Sending Commands

All command lines sent to the modem, except for **A**/, must be preceded by an 'AT' and terminated by the contents of S-register **S3** (typically a carriage return <CR>). AT stands for 'attention' and prompts the modem to receive a command line from the DTE. A <CR> informs the modem that the entire command string has been transmitted and to begin processing all the commands in the command line. A command line can include one or more AT commands. The commands can be separated by a space, if desired, but no punctuation is needed except for extended commands. Extended commands begin with a '+', such as fax, voice, and V.25 ter commands. In a multiple-command line, extended AT commands must be separated from following commands by a semicolon (;).

Examples:

```
ATS1?<CR>
A/
AT &F &D2 +FCLASS=?<CR>
AT +FCLASS=80; S0=1<CR>
```

The modem provides status information to the DTE in the form of response codes. The supported response codes are listed in Table 5-10 on page 34.

After sending an AT command string to the modem, the DTE must wait for a response code from the modem before sending a new AT command string to the modem.

5.2 AT Escape Sequences

The CL-MD562X/MD342X chipsets provide the industry-standard escape sequence, TIES (Time Independent Escape Sequence). TIES is designed to work with existing communication software written for the Hayes Escape Sequence.

Upon special request, Cirrus Logic provides the Hayes® Escape Sequence; however, please note that licensing can be required.

TIES/Hayes® Escape Sequences

The CL-MD562X/MD342X modem chipset is manufactured with TIES (Time Independent Escape Sequence) as the default setting. It is Hayes' position that you must have a valid license from Hayes Micro Computer of Norcross, Georgia, before producing modem systems that use the Hayes Escape Sequence.

Cirrus Logic accepts no responsibility and does not indemnify nor in any way provide protection for patent or possible patent violations to its customers or users of its products.

5.3 AT Command Summaries

Table 5-1. Data Mode Command Summary

Note	Command	Function	Default	Range	Reported by &Vn
**	A/	Repeat last command	none	–	no
	A	Answer	none	–	no
	Cn	Carrier control option	1	0, 1	no
	C0	Transmit carrier always off			
	C1	Normal transmit carrier			
	D	Dial command	none	–	no
*	En	Command mode echo	1	0, 1	yes
	E0	Disables echo			
	E1	Enables echo			
	Fn	Online echo	1	0, 1	no
	F0	Enables online echo			
	F1	Disables online echo			
	Hn	Switch hook control	0	0, 1	no
	H0	Hangs up the telephone line			
	H1	Picks up the telephone line			
	In	Identification/checksum option	0	0–7, 10–11, 20	no
	I0	Reports product code			
	I1	Reports modem chip firmware version			
	I2	Verifies ROM checksum			
	I3	Reports chipset name			
	I4	Reserved			
	I5	Reserved for modem chip hardware configuration			
	I6	Country code			
	I7	Version of board manufacturer firmware			
	I8	Features of modem firmware			
	I10	Modem board configuration — bits set by board manufacturer			
	I11	Modem board configuration — bits set by board manufacturer			
	I14	SAFE device			
	I20	Cirrus Logic silicon version			
	I21	Cirrus Logic firmware version			
	I22	Cirrus Logic manufacturer name			
	I23	Cirrus Logic product model			

Table 5-1. Data Mode Command Summary *(cont.)*

Note	Command	Function	Default	Range	Reported by &Vn
*	Ln	Speaker volume control	2	0–3	yes
	L0	Low speaker volume			
	L1	Low speaker volume			
	L2	Medium speaker volume			
	L3	High speaker volume			
*	Mn	Speaker control	1	0–3	yes
	M0	Speaker always off			
	M1	Speaker on until carrier present			
	M2	Speaker always on			
	M3	Speaker off during dialing; speaker on until carrier present			
	On	Go online	0	0, 1	no
	O0	Returns modem to Data mode			
	O1	Retrains equalizer and then returns to Data mode			
	O3	Renegotiates rate and then returns to Data mode			
*	P	Select pulse dialing	none	–	yes
*	Qn	Result code display control	0	0, 1	yes
	Q0	Enables result codes			
	Q1	Disables result codes			
	Sn	Select an S-register	none	0–33	no
	Sn=x	Write to an S-register	none	n=0–33 x=0–255	no
	Sn?	Read from an S-register	none	0–33	no
*	T	Select tone dialing	none	–	no
*	Vn	Result code form	1	0, 1	yes
	V0	Choose numeric form			
	V1	Choose verbose (text) form			
*	Wn	Response code data rate	0	0–4	yes
	W0	Reports DTE speed response codes			
	W1	Reports DTE speed response codes			
	W2	Reports DCE speed response codes			
	W3	Reports DTE speed response codes and information on error correction and data compression			
	W4	Reports protocol, data compression, and DTE data rate			

Table 5-1. Data Mode Command Summary *(cont.)*

Note	Command	Function	Default	Range	Reported by &Vn
*	Xn	Result code type	4	0–4	yes
	X0	Enables result codes 0–4; disables detection of busy and dial tone			
	X1	Enables result codes 0–5, 10, and above; disables busy and dial tone detection			
	X2	Enables result codes 0–6 and 10 and above; disables busy detection and enables dial tone detection			
	X3	Enables result codes 0–5, 7, and 10 and above; enables busy detection and disables dial tone detection			
	X4	Enables result codes 0–7 and 10 and above; enables busy and dial tone detection			
*	Yn	Long space disconnect	0	0, 1	yes
	Y0	Disables long space disconnect			
	Y1	Enables long space disconnect			
	Zn	Recall stored profile	0	0, 1	no
	Z0	Resets modem and recalls user profile 0			
	Z1	Resets modem and recalls user profile 1			
*	&Cn	DCD (data carrier detect) option	1	0, 1	yes
	&C0	Ignores remote modem status; DCD always on			
	&C1	DCD set according to remote modem status			
	&Dn	DTR (data terminal ready) option	2	0–3	yes
	&D0	In Async mode, modem ignores DTR			
	&D1	Modem switches from data mode to command mode when an on-to-off transition of DTR occurs			
	&D2	When DTR switches off, the modem goes on-hook and disables Auto-answer mode; when DTR switches on, auto-answer is enabled			
	&D3	Turning off DTR re-initializes the modem and resets values except UART registers			
	&F	Load factory defaults	none	–	no
*	&Gn	Guard tone option (1200 bps and 2400 bps only)	0	0–2	yes
	&G0	Disables guard tone			
	&G1	Enables 550-Hz guard tone			
	&G2	Enables 1800-Hz guard tone			
*	&Jn	Auxiliary relay control	0	0, 1	yes
	&J0	Auxiliary relay never operated			
	&J1	Activates auxiliary relay when modem is off-hook			

Table 5-1. Data Mode Command Summary *(cont.)*

Note	Command	Function	Default	Range	Reported by &Vn
	&Kn	Select serial flow control	3	0, 3, 4	yes
	&K0	Disables flow control			
	&K3	Bidirectional hardware flow control			
	&K4	XON/XOFF software flow control			
*	&Pn	Dial pulse ratio	0	0, 1	yes
	&P0	Sets 10-pps pulse dial with 39%/61% make-break			
	&P1	Sets 10-pps pulse dial with 33%/67% make-break			
*	&Sn	DSR (data set ready) option	0	0, 1	yes
	&S0	DSR is always active			
	&S1	DSR active only during handshaking and when carrier is lost			
	&Tn	Self test commands	0	0, 1	no
	&T0	Terminates test in progress			
	&T1	Initiates local analog loopback			
*	&Un	Disable Trellis coding	0	0, 1	yes
	&U0	Enables Trellis coding with QAM as fallback			
	&U1	QAM modulation only			
	&Vn	View active and stored profiles	0	0, 1, 3	no
	&V0	View active profile and stored profile 0			
	&V1	View active profile and stored profile 1			
	&V3	View relay and general-purpose input-output status			
	&Wn	Stored active profile	0	0, 1	no
	&W0	Store in user profile 0			
	&W1	Store in user profile 1			
*	&Yn	Select stored profile on power up	0	0, 1	yes
	&Y0	Recall stored profile 0 on power-up			
	&Y1	Recall stored profile 1 on power-up			
	&Zn=x	Store telephone number (up to 30 digits) to location ‘n’ (0–3)	none	n = 0–3 x = 0–9 A B C D # * T P R W @ , ! ;	no
*	%En	Auto-retrain control	1	0, 1	yes
	%E0	Disables auto-retrain			
	%E1	Enables auto-retrain			
*	%Gn	Rate renegotiation	1	0, 1	yes
	%G0	Disabled			
	%G1	Enabled			

Table 5-1. Data Mode Command Summary *(cont.)*

Note	Command	Function	Default	Range	Reported by &Vn
*	-Cn	Generate data mode calling tone	0	0–2	yes
	-C0	Calling tone disabled			
	-C1	1300-Hz calling tone enabled			
	-C2	V.8 calling tone and 1300-Hz calling tone			
	+A8E=m	V.8 and V.8 bis operation controls	1,1,C1,0,0	See note [a]	no
*	+DS=m	Controls V.42 bis data compression	3,0,2048,6	See note [a]	yes
	+ES=m	Error control selection	3,0,2	See note [a]	no
	+GMI?	Identify modem manufacturer	none	–	no
	+GMM?	Identify product model	none	–	no
	+GMR?	Identify product revision	none	–	no
	+MS=m	Modulation selections	X2, 1, 0, 0, 0, 0	See note [b]	no

[a] See the controllerless modem programmer's guide for full command description and parameter ranges.

[b] For Data mode, the factory default setting is AT+MS=X2, 1, 0, 0, 0, 0 to send at speeds of 31,200 bps or below and receive at speeds of 53,333 bps and below.

* Value saved in NVRAM. **Command not preceded by an 'AT'.

Table 5-2. V.42 / V.42 bis MNP® Command Summary

Note	Command	Function	Default	Range	Reported by &Vn
*	%An	Set auto-reliable fallback character	13	0–127	yes
*	%Cn	MNP 5 data compression control	1	0, 1	yes
	%C0	No compression			
	%C1	Enables MNP5 data compression			
*	\An	MNP block size	3	0–3	yes
	\A0	Maximum 64 characters			
	\A1	Maximum 128 characters			
	\A2	Maximum 192 characters			
	\A3	Maximum 256 characters			
*	\Cn	Set auto-reliable buffer	0	0–2	yes
	\C0	No data buffering			
	\C1	Four-second buffer until 200 characters in the buffer or detection of a SYN character			
	\C2	No buffering. Connects non-V.42 modems to V.42 modem			
*	\Gn	Set modem port flow control	0	0, 1	yes
	\G0	Disables port flow control			
	\G1	Sets port flow control to XON/XOFF			
*	\Jn	bps rate adjust control	0	0, 1	yes
	\J0	Disables rate adjust			
	\J1	Enables rate adjust			
*	\T0	Disables inactivity timer	0	0–90	yes
*	\Xn	Set XON/XOFF pass-through	0	0, 1	yes
	\X0	Processes flow control characters			
	\X1	Processes flow control characters and passes to local or remote			
*	-Jn	Set V.42 detect phase	1	0, 1	yes
	-J0	Disables the V.42 detect phase			
	-J1	Enables the V.42 detect phase			
*	"Hn	V.42 bis compression control	3	0–3	yes
	“H0	Disables V.42 bis			
	“H1	Enables V.42 bis only when transmitting data			
	“H2	Enables V.42 bis only when receiving data			
	“H3	Enables V.42 bis for both transmitting and receiving data			
	"On	V.42 bis string length	32	6–250	yes

* Value saved in NVRAM.

Table 5-3. Fax Identity Command Summary

Command	Function	Default	Range	Reported by &Vn
+FMDL?	Identifies product model	none	–	no
+FMFR?	Identifies modem manufacturer	none	–	no
+FMI?	Identifies modem manufacturer	none	–	no
+FMM?	Identifies product model	none	–	no
+FMR?	Identifies product version number	none	–	no
+FREV?	Identifies product version number	none	–	no

Table 5-4. Fax Class 1 Command Summary

Command	Function	Default	Range	Reported by &Vn
+FCLASS=1	Mode selection	0	0, 1, 8, 80	no
+FRH=n	Receive HDLC data	none	3	no
+FRM=n	Receive data	none	24, 48, 72, 73, 74, 96, 97, 98, 121, 122, 145, 146	no
+FRS=n	Wait for silence	none	1–255	no
+FTH=n	Transmit HDLC data	none	3	no
+FTM=n	Transmit data	none	24, 48, 72, 73, 74, 96, 97, 98, 121, 122, 145, 146	no
+FTS=n	Stop transmission and pause	none	0–255	no

Table 5-5. IS-101 Voice Command Summary

Command	Function	Default	Range	Reported by &Vn
+FCLASS=8	Voice mode selection	0	0, 1, 8, 80	no
+FLO=n	Flow Control Select	1	0–2	no
+VBT=m	Buffer threshold setting	192, 320	192, 320	no
+VCID=n	Caller ID selection	0*	0–2	no
+VDR=m	Distinctive Ring selection	0,0	0–255, 0–255	no
+VEM=m	Event reporting and masking	'C' BB860980 BFE63883 BB863EE0	–	no
+VGM=n	Speakerphone microphone gain	128	121–131	no
+VGR=n	Receive gain selection	128	121–131	no
+VGS=n	Speakerphone speaker gain	128	121-131	no
+VGT=n	Volume selection	128	121–131	no
+VIP	Initialize parameter	–	–	no
+VIT=n	DTE/DCE inactivity timer	0	0–255	no
+VLS=n	Hardware type control	0	0–15	no
+VNH=n	Automatic hang-up control	0	0–2	no
+VRA=n	Ringback-goes-away timer	50	0–50	no
+VRN=n	Ringback-never-appeared timer	10	0–255	no
+VRX	Record mode	none	–	no
+VSD=m	Silence detection (quiet and silence)	128, 50	See note	no
+VSM=m	Compression method selection	140, 8000, 0, 0	See note	no
+VSP=n	Speakerphone on/off control	0	0, 1	no
#VSPS=n	Speakerphone type selection	1	0, 1	no
+VTD=n	Beep tone duration timer	100	5–255	no
+VTS=m	DTMF and tone generation	none	See note	no
+VTX	Play mode	none	–	no

NOTE: See the complete command description in the controllerless modem programmer's guide for range information.

* The noted parameters, commands, and responses depend on the capability to receive.

Table 5-6. Voice DTE→DCE Character Pairs

Response	Hex Code	Function
<NUL>	00	Do nothing
<DLE>	10	Two contiguous <DLE><DLE> codes indicate a single <DLE> in the data stream
<SUB>	1A	<DLE><DLE> in data stream
<ETX>	03	End transmit data state
/	2F	Start of DTMF tone shielding
<DEL>	7F	DTMF transition to off
u	75	Bump up the volume
d	64	Bump down the volume
<ESC>	1B	End receive data state
!	21	Receive data abort
<CAN>	18	Clear transmit buffer of voice data
?	3F	Transmit buffer space available query
<DLE>	10	Single <DLE> character in the data stream
<SUB>	1A	<DLE><DLE> in data stream
<ETX>	3	End of Record mode data
X	58	Packet header for 'Complex Event Detection Report'
.	2E	Packet terminator for the 'Complex Event Detection Report'
/	2F	Start of DTMF tone shielding
<DEL>	7F	DTMF transition to off
0–9	30–39	DTMF tones 0–9
A–D	41–44	DTMF tones A–D
*	2A	DTMF tone *
#	23	DTMF tone #
o	6F	Receive buffer overrun
c	63	1100-Hz fax calling tone
e	65	1300-Hz data calling tone
h	68	Local phone goes on hook
H	48	Local phone goes off hook
s	73	Presumed hang-up silence time-out
q	71	Presumed end-of-message quiet time-out
r	72	Ringback
b	62	Busy/reorder/fast busy
d	64	Dial tone detected
u	75	Transmit buffer under-run
a	61	Fax or data answer tone (2100 Hz)
f	66	Data answer detected (2225 Hz)
R	52	Incoming ring

Table 5-7. Dial Modifiers

Command	Function
0 to 9	Dialing digits
A, B, C, D, *, #	Tone dial characters
P	Pulse dial
R	Reverse Originate mode
S=n	Dial NVRAM telephone number
T	Tone dial
W	Wait for dial tone
,	Pause
!	Flash hook
@	Wait for quiet answer
;	Return to command state
- ( )	Ignored by modem

Table 5-8. Manufacturing-Only Command Summary[a]

Note	Command	Function	Default	Range
*	*NCnn	Country Select	0	–
	!P=m	Set plug-and-play board serial number	none	0–255, 0–255, 0–255, 0–255
*	S91	Select transmit level	–10	9–16
*	S92	DTMF transmit level	–10	0–15
	#VGP0=n	Read/write to general-purpose pins 0–7	See note	–
	#VGP1=n	Read/write to general-purpose pins 8–15	See note	–
	#VGP2=n	Read/write to general-purpose pins 16–23	See note	–

[a] These commands are meant to be used by the board manufacturer and not in generic applications software for end users.

* Value saved in NVRAM.

NOTE: Default values for **#VGP0–2 =n** are dependent on board design.

Table 5-9. S-Register Summary

Note	Register	Function	Default	Range	Units	Reported by &Vn
*	S0	No. of rings to auto-answer on	0	0–255	ring	yes
	S1	Ring count	0	0–255	ring	yes
*	S2	Escape character	43	0–127	ASCII	yes
	S3	Carriage return character	13	0–127	ASCII	yes
	S4	Line feed character	10	0–127	ASCII	yes
	S5	Backspace character	8	0–32, 127	ASCII	yes
*	S6	Wait before dialing	2	2–255	second	yes
*	S7	Wait for carrier	60	1–255	second	yes
*	S8	Pause time for dial modifier	2	0–255	second	yes
*	S9	Carrier recovery time	6	1–255	0.1 second	yes
*	S10	Lost carrier hang up delay	14	1–255	0.1 second	yes
*	S11	DTMF dialing speed	70	50–255	ms	yes
*	S12	Guard Time	50	0–255	(0.02 second)	yes
*	S14	Bit-mapped options	138	–	–	no
	S16	Modem test options	0	–	–	no
*	S18	Modem test timer	0	0–255	second	yes
*	S21	Bit-mapped options	48	–	–	no
*	S22	Bit-mapped options	118	–	–	no
*	S23	Bit-mapped options	31	–	–	no
*	S25	Detect DTR change	5	0–255	0.01 second	yes
*	S27	Bit-mapped options	64	–	–	no
*	S30	Disconnect inactivity timer	0	0–255	minute	yes
*	S31	Bit-mapped options	49	–	–	no
*	S33	Sleep mode timer	10	0–90	second	yes

NOTE: The manufacturing-only S-registers **S91** and **S92** are listed in the Manufacturing-Only Commands in Table 5-8 on page 32.

* Value saved in NVRAM.

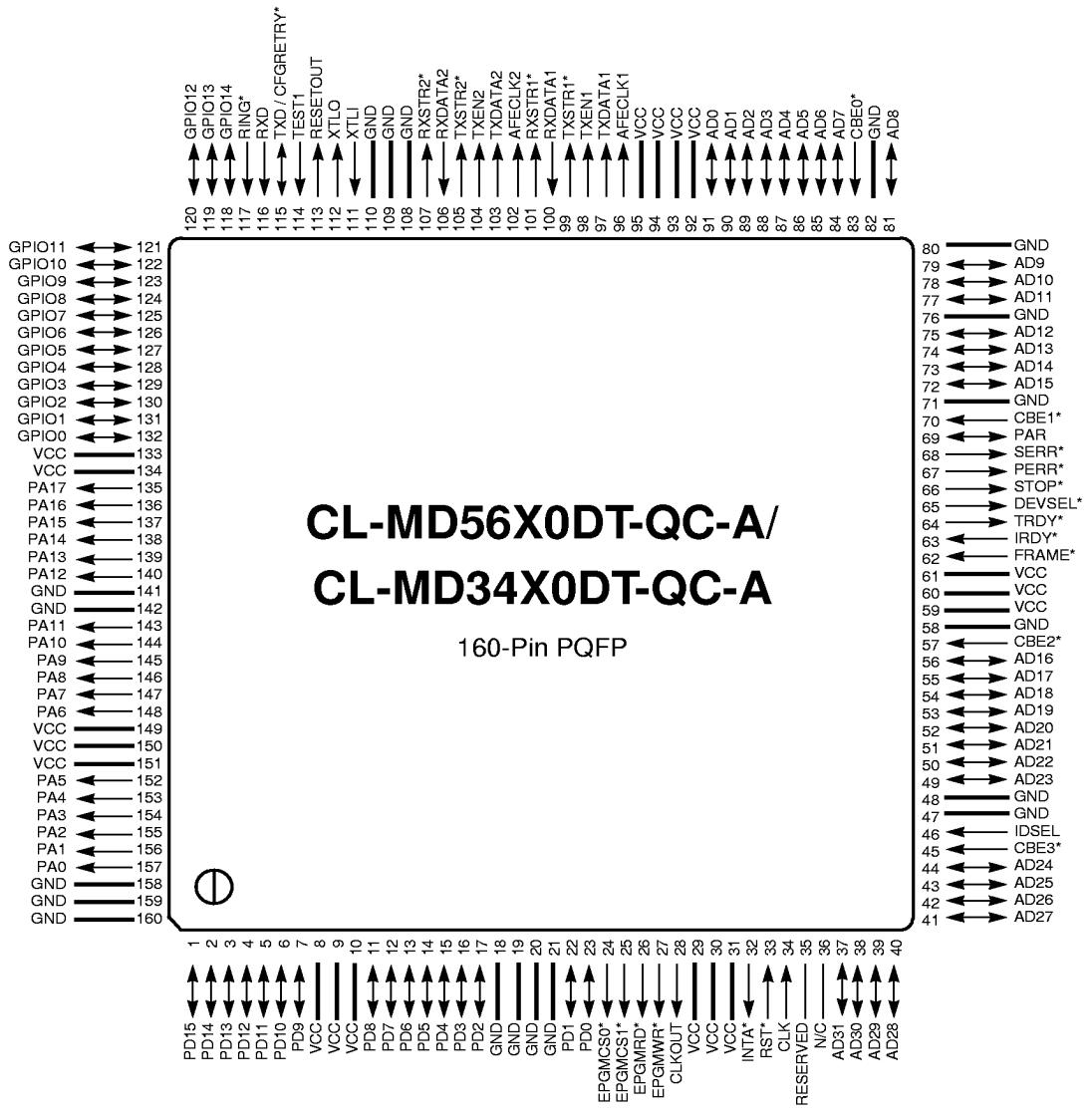
Table 5-10. DTE-Modem Data Rate Response Codes

Numeric Code	Verbose Code	Numeric Code	Verbose Code
0	OK	42	CONNECT 48000
1	CONNECT	43	CONNECT 49333
2	RING	45	RINGBACK
3	NO CARRIER	53	CONNECT 50666
4	ERROR	54	CONNECT 52000
5	CONNECT 1200	55	CONNECT 53333
6	NO DIALTONE	58	CONNECT 57333
7	BUSY	59	CONNECT 16800
8	NO ANSWER	60	CONNECT 21600
9	CONNECT 600	62	CONNECT 24000
10	CONNECT 2400	63	CONNECT 26400
11	CONNECT 4800	64	CONNECT 28800
12	CONNECT 9600	65	CONNECT 31200
13	CONNECT 14400	66	CONNECT 33600
14	CONNECT 19200	67	COMPRESSION: V.42BIS
18	CONNECT 57600	68	COMPRESSION: MNP5
22	CONNECT 1200/75	69	COMPRESSION: NONE
23	CONNECT 75/1200	70	PROTOCOL: NONE
24	CONNECT 7200	74	PROTOCOL: V80 SAM
25	CONNECT 12000	77	PROTOCOL: LAP-M
28	CONNECT 38400	80	PROTOCOL: MNP
31	CONNECT 115200	81	PROTOCOL: MNP 2
32	FCERROR	82	PROTOCOL: MNP 3
33	CONNECT 33333	83	PROTOCOL: MNP 2,4
34	CONNECT 37333	84	PROTOCOL: MNP 3,4
35	CONNECT 41333	98	CPON=
36	CONNECT 42666	99	CPOF=
37	CONNECT 44000	100	DRON=
38	CONNECT 45333	101	DROF=
39	CONNECT 46666	See Note	CONNECT (*DTE data rate*) /(*modulation*)/(*error correction*)/(*data compression*) / TX:(*DCE transmit data rate*) / RX:(*DCE receive data rate*)

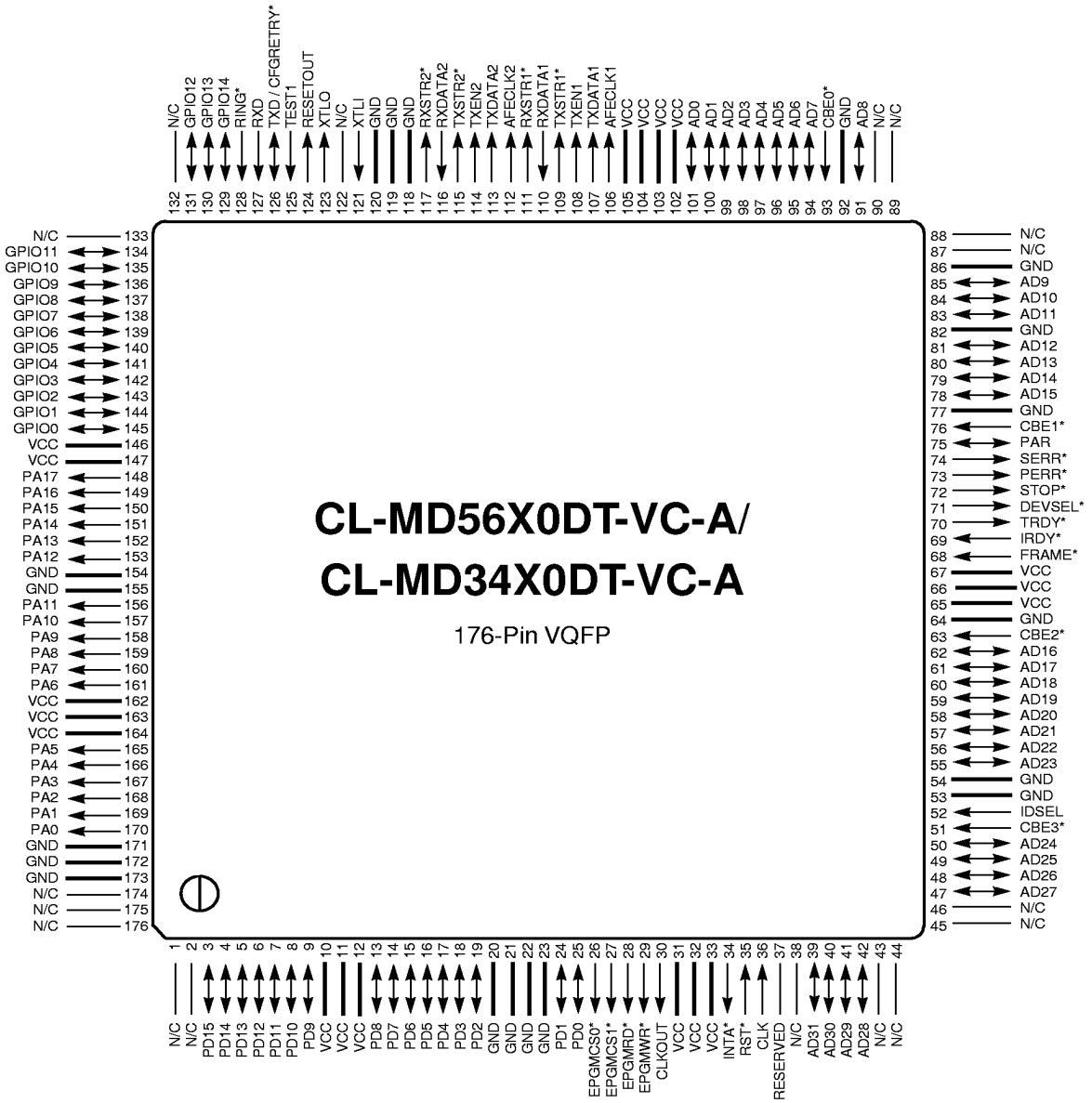
NOTE: The **W3** AT command reports the special verbose code listed, which is used to evaluate the modem connection. The **W0**, **W1**, **W2**, and **W4** AT commands report all other 'CONNECT' messages. When the modem is configured for text responses **V1**, the **W3** verbose response provides information about the DTE data rate, connection modulation, error correction protocol, data compression, and modem-to-modem data rate. When the modem is configured for **W3** and numeric responses **V0**, the modem responds as if it were set up for **W0**.

6. PIN DIAGRAMS

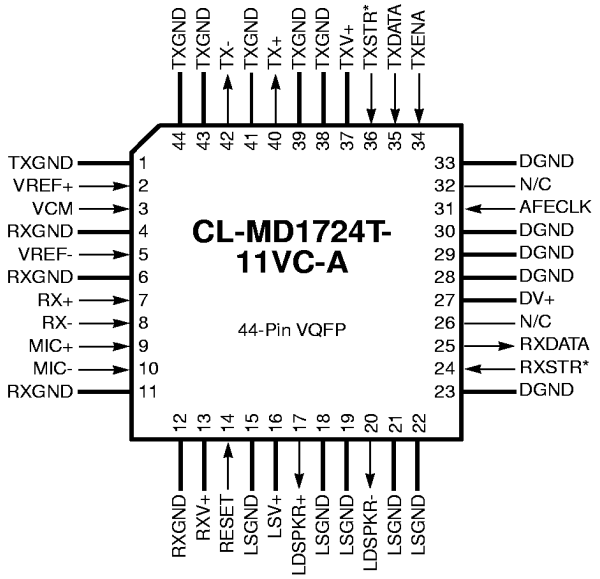
6.1 DSP 160-pin PQFP Pin Diagram



6.2 DSP 176-pin VQFP Pin Diagram



6.3 SAFE 44-pin VQFP Pin Diagram



7. PIN DESCRIPTIONS

7.1 DSP Pin Descriptions

7.1.1 General-Purpose Input/Output Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
GPIO[14:0]	118–132	129–131 134–145	I/O	**GENERAL-PURPOSE I/O**: Each pin is programmable as an input or output.
RING*	117	128	I	**RING***: This pin can be used as a general-purpose input or for ring detection. When this signal toggles, it can generate an interrupt.

7.1.2 PCI Interface Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
AD[31:0]	37–44 49–56 72–75 77–79 81 84–91	39–42 47–50 55–62 78–81 83–85 91 94–101	I/O	**PCI ADDRESS/DATA BUS[31:0]**: The primary address and data pins are multiplexed on these pins. Each transaction is initiated by a 32-bit physical address phase, which is then followed by a data phase. These pins support both reading and writing.
CBE*[3:0]	45, 57 70, 83	51, 63 76, 93	I	**PCI COMMAND/BYTE ENABLE BUS**: Both command and byte enables are multiplexed on the same active low PCI pins. These pins define the bus command during the address phase and are used as byte enables during the data phase.
CLK	34	36	I	**PCI CLOCK**: Clock for the PCI interface.
DEVSEL*	65	71	O	**PCI DEVICE SELECT**: This active low pin is driven by the target and indicates to the initiating master that the current transaction is within the target's address range.
IDSEL	46	52	I	**PCI INITIALIZATION DEVICE SELECT**: This pin is used as an ID select to access the controller configuration space.
FRAME*	62	68	I	**PCI CYCLE FRAME**: This active low pin is driven by the current initiator and indicates the start and duration of a transaction. FRAME* is deasserted to indicate that the initiator is ready to complete the final data phase.
INTA*	32	34	O	**PCI INTERRUPT A**: This active low pin requests an interrupt from the controller to the PCI bus.

7.1.2 PCI Interface Pin Descriptions *(cont.)*

Symbol	PQFP	VQFP	Type	Description
IRDY*	63	69	I	**PCI INITIATOR READY**: This active low pin indicates that the initiator of the transaction is ready to complete the current data phase. During a write, IRDY* assertion indicates that the initiator is driving valid data on the bus. During a read phase, IRDY* assertion indicates that the initiator is ready to receive data from the target.
PAR	69	75	I/O	**PCI PARITY**: This pin indicates even parity across AD[31:0] and CBE[3:0]*.
PERR*	67	73	O	**PCI PARITY ERROR**: This active low pin indicates a data parity error during all transactions except a special cycle. It may be pulsed active by any agent that detects an error condition.
RESERVED	35	37	–	**RESERVED**: This pin is reserved and should be connected to ground.
RST*	33	35	I	**DSP RESET**: Resets input to the DSP. This signal is driven by the PCI bus, but it also acts as a chip reset.
SERR*	68	74	O	**PCI SYSTEM ERROR**: This active low pin indicates either an address or data parity error on special cycles or any other system error where the results could be catastrophic.
STOP*	66	72	O	**PCI STOP**: This active low pin indicates that the target is requesting the master to stop the current transaction.
TRDY*	64	70	O	**PCI TARGET READY**: This active low pin indicates to the initiating master that the target device is able to complete the current data phase of the transaction. During a read phase, TRDY* indicates that valid data is present on AD[31:0]*; during a write phase, it indicates that the device is ready to accept data.

7.1.3 Unconnected Pins

Symbol	PQFP	VQFP	Type	Description
N/C	36	38, 1, 2 43–46 87–90 122, 132 133 174–176		**NO CONNECT**: These pins should be left unconnected.

7.1.4 DSP Program Memory Interface Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
EPGMRD*	26	28	O	**EXTERNAL PROGRAM MEMORY READ ENABLE:** This signal is asserted low when the DSP reads from the external program memory. Leave unconnected during normal setup.
EPGMCS0*	24	26	O	**EXTERNAL PROGRAM MEMORY CHIP SELECT 0:** This chip select is asserted (active low) when the chip is accessing external memory. When not in use, leave this pin unconnected.
EPGMCS1*	25	27	O	**EXTERNAL PROGRAM MEMORY CHIP SELECT 1:** This chip select is asserted (active low) when the chip is accessing external memory. When not in use, leave this pin unconnected.
EPGMWR*	27	29	O	**EXTERNAL PROGRAM MEMORY READ ENABLE:** This signal is asserted low when the DSP is writing to the external program memory. Leave unconnected during normal setup in V.34 mode. For the x2 mode, connect to external SRAM.
PA[17:0]	135–140 143–148 152–157	148–153 156–161 165–170	O	**PROGRAM MEMORY ADDRESS BUS:** These pins provide the addresses necessary to address an external peripheral. Leave unconnected during normal setup in V.34 mode. For the x2 mode, connect to external SRAM.
PD[15:0]	1–7 11–17 22, 23	3–9 13–19 24, 25	I/O	**PROGRAM MEMORY DATA BUS:** These pins are used to read from or write to external memory or devices. Leave unconnected during normal setup in V.34 mode. For the x2 mode, connect to external SRAM.

7.1.5 DSP Power Pin Descriptions

Symbol	PQFP	VQFP	Type	Description
GND	18–21 47, 48 58, 71 76, 80, 82 108–110 141, 142 158, 159 160	20–23 53, 54 64, 77, 82 86, 92 118–120 154 155 171–173	GND	**DIGITAL GROUND**
V_{CC}	8–10 29–31 59–61 92–95 133, 134 149–151	10–12 31–33 65–67 102–105 146 147 162–164	PWR	**+5-V POWER SUPPLY**: The DSP requires only +3.3 V to perform all digital processing.

7.1.6 DSP UART/Clock/Control Pin Descriptions

This group of pins includes UART and DSP test functions.

Symbol	PQFP	VQFP	Type	Description
CLKOUT	28	30	O	**CLOCK OUT**: This pin provides a buffered DSP clock output signal when enabled.
RESETOUT	113	124	O	**RESET OUTPUT:** This is an inverted version of the RST* pin. The RESETOUT signal can be used to reset the SAFE.
RXD	116	127	I	**UART RECEIVE DATA**: The UART receives the input data through this pin. Connect this pin low if not in use.
TEST1	114	125	I	**MANUFACTURING TEST PIN**: This pin is used during Cirrus Logic manufacturing for testing purposes. This pin must be pulled down to ground for all applications.
TXD / CFGRETRY*	115	126	I/O	**UART TRANSMIT DATA / PCI CONFIGURATION REGISTER RETRY**: The UART transmits the output data through this register. When the UART is not use, this pin is configured as an input. Leave unconnected if not in use. On reset, TXD is configured as an input. If sampled low during reset, the chip will disconnect without data if the master tries to access a programmable PCI Configuration register that is not programmed. If sampled high during reset, the chip sends the PCI master the default value if the master tries to access a programmable PCI Configuration register. Connect low when NVRAM is present.
XTLI XTLO	111 112	121 123	I O	**DSP CRYSTAL INPUT AND OUTPUT**: These two pins provide a feedback circuit for generating the chipset system 23.04-MHz clock.

7.1.7 DSP-SAFE Interface Pin Descriptions

The DSP provides two interfaces for SAFE devices. The CL-MD5620T chipset with a single SAFE device uses interface 1, while the chipsets CL-MD5622T/5632T with two SAFE devices use interfaces 1 and 2.

Symbol	PQFP	VQFP	Type	Description
AFECLK1 AFECLK2	96 102	106 112	O O	**SAFE CLOCK**: These pins provide the clock source for the SAFE device.
RXDATA1 RXDATA2	100 106	110 116	I I	**RX DATA**: Through these pins, the DSP receives serial data from the SAFE device.
RXSTR1* RXSTR2*	101 107	111 117	O O	**RECEIVE STROBE**: The DSP uses these pins to provide the SAFE with a strobe enable signal for the serial reception of data. Polarity is programmable. Reset is active low.
TXDATA1 TXDATA2	97 103	107 113	O O	**TX DATA**: These pins transmit serial data from the DSP to the SAFE device.
TXEN1 TXEN2	98 104	108 114	O O	**TX ENABLE**: These pins enable the transmittal of data from the DSP to the SAFE device. Polarity is programmable. Reset is active high.
TXSTR1* TXSTR2*	99 105	109 115	O O	**TRANSMIT STROBE**: The DSP uses these pins to provide the SAFE with a strobe enable signal for serial transmission of data.

7.2 SAFE Pin Descriptions

7.2.1 SAFE–DAA Interface Pin Descriptions

Symbol	VQFP	Type	Description
RX+ RX-	7 8	I I	**RECEIVE ANALOG DATA**: These input pins receive the analog differential signals from the DAA.
TX+ TX-	40 42	O O	**TRANSMIT ANALOG DATA**: These pins provide the analog transmitter differential output signals to the DAA.

7.2.2 SAFE General Pin Descriptions

Symbol	VQFP	Type	Description
LDSPKR+ LDSPKR-	17 20	O O	**LOUDSPEAKER OUTPUT**: These pins provide a differential output signal for driving an external loudspeaker. These pins can be connected directly to a ≥ 8-Ω speaker or a speaker amplifier.
MIC+	9	I	**MICROPHONE + INPUT**: This input pin is a single-ended amplifier input for a microphone. It requires a 10-kΩ pull-up resistor to the SAFE VCM pin. If the microphone function is not used, then connect this pin to analog ground.

7.2.2 SAFE General Pin Descriptions *(cont.)*

Symbol	VQFP	Type	Description
MIC–	10	I	**MICROPHONE – INPUT**: This pin provides a switched ground connection that interrupts the microphone bias current during power down. If the microphone function is not used or if disabling the microphone bias current during power down is not desirable, then connect this pin to analog ground.
N/C	32	–	**NO CONNECT**: This pin must be left unconnected.
RESET	14	I	**SAFE RESET**: This pin is used to generate a SAFE reset. A reset is accomplished by pulsing the signal at the RESET pin from a low to high to low. The RESET input pin must be high for at least 10 µs. The SAFE requires 200 ms, after the high-to-low transition, before communicating with the DSP.

7.2.3 SAFE–DSP Interface Pin Descriptions (CL-MD1724T)

CAUTION: These pins provide the control/data/clock signals between the SAFE and the DSP. No external components should be connected to these pins.

Symbol	VQFP	Type	Description
AFECLK	31	I	**SAFE CLOCK**: This pin provides the clock source for the SAFE device.
RXDATA	25	O	**RX DATA**: This pin transmits the receive serial data from the SAFE device to the DSP.
N/C	26	O	**NO CONNECT:** This pin must be left unconnected.
RXSTR*	24	I	**RECEIVE STROBE**: This pin provides the clock signal required for the DSP to receive the serial receive data from the SAFE device.
TXSTR*	36	I	**TRANSMIT STROBE**: This pin provides the clock signal required for the SAFE device to receive the serial transmit data from the DSP.
TXDATA	35	I	**TX DATA**: Through this pin the SAFE device receives serial data transmitted from the DSP.
TXENA	34	I	**TX ENABLE**: This pin enables the transmittal of data from the DSP to the SAFE device.

7.2.4 SAFE Power Supply Pin Descriptions

Symbol	VQFP	Type	Description
DGND	23 28–30, 33	GND	**DIGITAL GROUND REFERENCE**
DV+	27	PWR	**DIGITAL SUPPLY** (5 V ±5%)
LSGND	15,18 19, 21 22	AGND	**LOUDSPEAKER ANALOG GROUND REFERENCE**
LSV+	16	PWR	**LOUDSPEAKER SUPPLY VOLTAGE** (5 V ±5%)
RXGND	4, 6, 11,12	AGND	**RECEIVER ANALOG GROUND REFERENCE**
RXV+	13	PWR	**RECEIVER ANALOG SUPPLY VOLTAGE** (5 V ±5%)
TXGND	1, 38, 39, 41, 43, 44	AGND	**TRANSMITTER ANALOG GROUND REFERENCE**
TXV+	37	PWR	**TRANSMITTER ANALOG SUPPLY VOLTAGE** (5 V ±5%)
VCM	3	I	**VOLTAGE COMMON MODE**: The SAFE provides an internal 2.5-V reference for the differential analog circuitry. This pin allows the reference to be bypassed using an external 1.0-µF capacitor.
VREF+ VREF-	2 5	I I	**VOLTAGE REFERENCE BUFFER**: The SAFE incorporates an internal differential voltage reference. These pins allow the internal differential reference to be bypassed using an 1.0-µF external capacitors.

8. ELECTRICAL SPECIFICATIONS

Table 8-1. Absolute Maximum Ratings

Parameter	Value
Supply voltage (V_{CC})	+3.6 V
Input voltages, with respect to ground	–0.3 V to +6.0 V
Operating temperature (T_A)	0°C to 70°C
Storage temperature	–65°C to 150°C

NOTE: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8-2. Recommended Operating Conditions

Parameter	Value
Supply voltage (V_{CC})	3.3 V ± 10%
Operating free air ambient temperature	0°C < T_A < 70°C
Crystal frequencies	23.04 MHz

8.1 DSP 3.3-V DC Electrical Characteristics (PCI Pins)

(@ V_{CC} = 3.3 V ± 10%; T_A = 0°C to 70°C.)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
V_{IL}	Input low voltage	–.5	–	.3 V_{CC}	V	
V_{IH}	Input high voltage	1.5	–	5.5	V	
V_{OL}	Output low voltage	–	–	0.1 V_{CC}	V	I_{OL} = 2.4 mA
V_{OH}	Output high voltage	0.9 V_{CC}	–	–	V	I_{OH} = –400 µA
I_{IH}	Input high leakage current	–	–	–70	µA	V_{IN} = 2.7
I_{IL}	Input low leakage current	–	–	–70	µA	V_{IN} = .5

8.2 DSP Pin 3.3-V DC Electrical Characteristics (Non-PCI Pins)

(@ V_{CC} = 3.3 V ± 10%; T_A = 0°C to 70°C.)

Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
V_{IL}	Input low voltage	–.3	–	.8	V	
V_{IH}	Input high voltage	2.0	–	V_{CC} + .3	V	
V_{OL}	Output low voltage	–	–	0.4	V	I_{OL} = 2.4 mA
V_{OH}	Output high voltage	2.4	–	–	V	I_{OH} = –400 µA
I_{IH}	Input high leakage current	–	–	1	µA	V_{IH} =V_{CC}
I_{IL}	Input low leakage current	–1	–	–	µA	V_{IL}

8.3 DSP 3.3-V Power Consumption

The following DSP power values were obtained from testing the MDK562X-0C02 controllerless modem reference design.

Parameter	MIN	TYP	MAX	Units	Test Conditions
Idle mode	–	35	–	mA	Ideal
Loopback mode	–	115	–	mA	
Online V.34 mode	–	115	–	mA	
Online 56K mode	–	95	–	mA	

8.4 AC/DC Electrical Characteristics — CL-MD1724T (SAFE)

(@ V_{CC} = 5 V ± 5%, T_A = 0°C to 70°C)

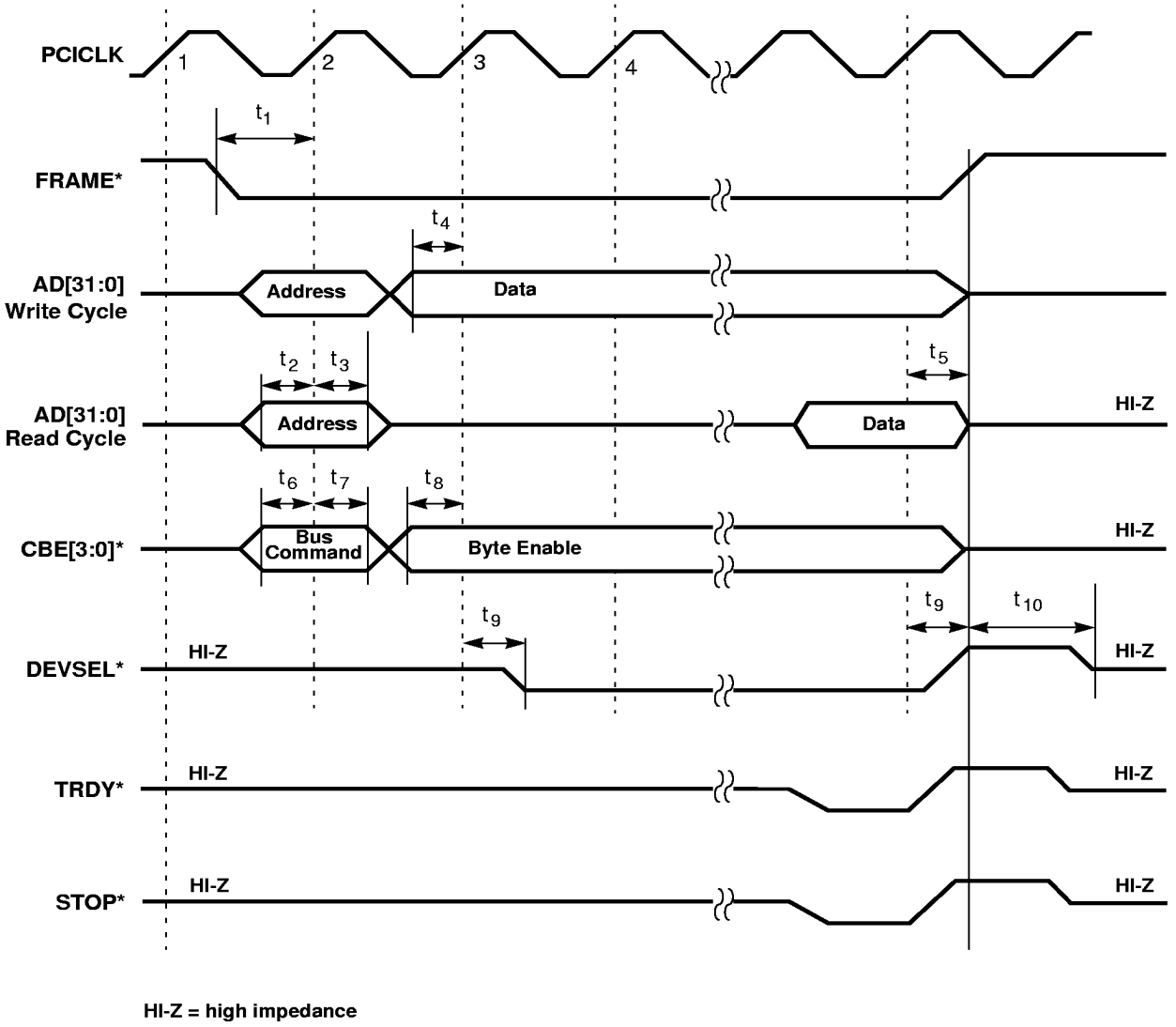
Symbol	Parameter	MIN	TYP	MAX	Units	Test Conditions
P_D	Power dissipation	–	130	195	mW	Operational mode
P_{D-PD}	Power dissipation (Power-down mode)	–	–	500	µW	Loudspeaker driver off
I_A	Analog current (TV+, RV+)	–	24	–	mA	Loudspeaker driver off
I_D	Digital current (DV+)	–	2	–	mA	
I_{IDS}	Loudspeaker current (LDSPKR+, LDSPKR–)	–	–	125	mA	
R_X	Loudspeaker impedance	8	–	100	Ω	

8.5 Timing Diagrams

8.5.1 Index of Timing Information

Table 8-3. FRAME*, AD[31:0], CBE[3:0]*, and DEVSEL* Timing Diagram

Symbol	Parameter	PCI_VCC = 3.3 V		Units
		MIN	MAX	
t_1	FRAME* setup to PCICLK	7	–	ns
t_2	AD[31:0] (address) setup to PCICLK	7	–	ns
t_3	AD[31:0] (address) hold from PCICLK	0	–	ns
t_4	AD[31:0] (data) setup to PCICLK	7	–	ns
t_5	AD[31:0] (data) active to HI-Z from PCICLK	0	28	ns
t_6	CBE[3:0]* (bus command) setup to PCICLK	7	–	ns
t_7	CBE[3:0]* (bus command) hold from PCICLK	0	–	ns
t_8	CBE[3:0]* (byte enable) setup to PCICLK	7	–	ns
t_9	DEVSEL* delay from PCICLK	–	11	ns
t_{10}	DEVSEL* high before HI-Z	1	–	PCICLK



HI-Z = high impedance

Figure 8-1. FRAME*, AD[31:0], CBE[3:0]*, and DEVSEL* Timing Diagram

Table 8-4. TRDY* and STOP* Delay Timing Diagram

Symbol	Parameter	PCI_VCC = 3.3 V		Units
		MIN	MAX	
t_1	TRDY* active delay from PCICLK	–	11	ns
t_2	TRDY* inactive delay from PCICLK	–	11	ns
t_3	TRDY* high before HI-Z	1	–	PCICLK
t_4	STOP* active delay from PCICLK	–	11	ns
t_5	STOP* inactive delay from PCICLK	–	11	ns
t_6	STOP* high before HI-Z	1	–	PCICLK

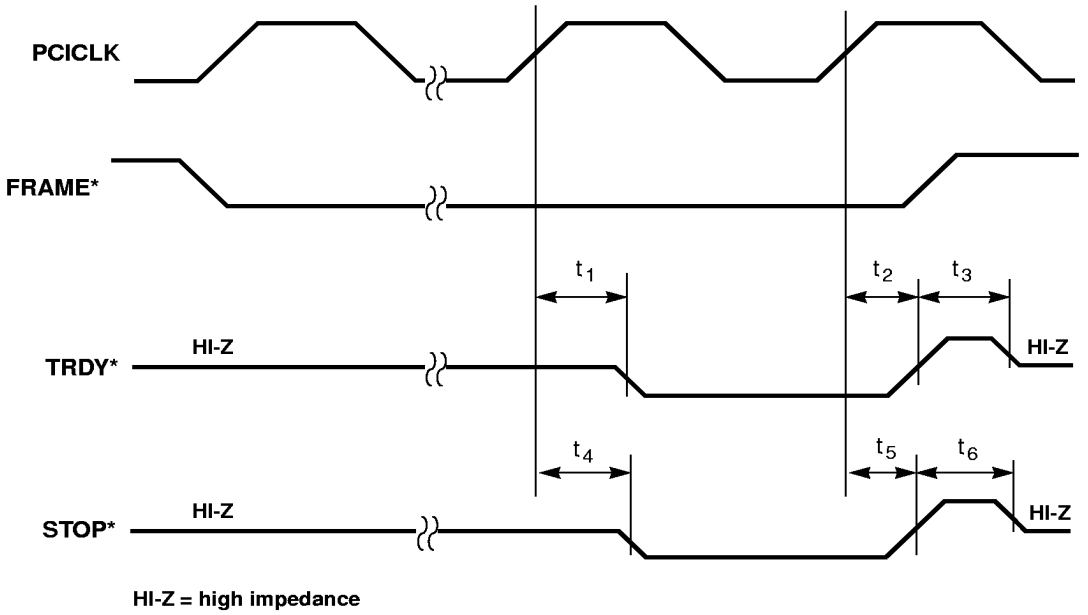


Figure 8-2. TRDY* and STOP* Delay Timing Diagram

Table 8-5. IDSEL Timing in a Configuration Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	IDSEL setup to PCICLK	7	–	ns
t_2	IDSEL hold from PCICLK	0	–	ns

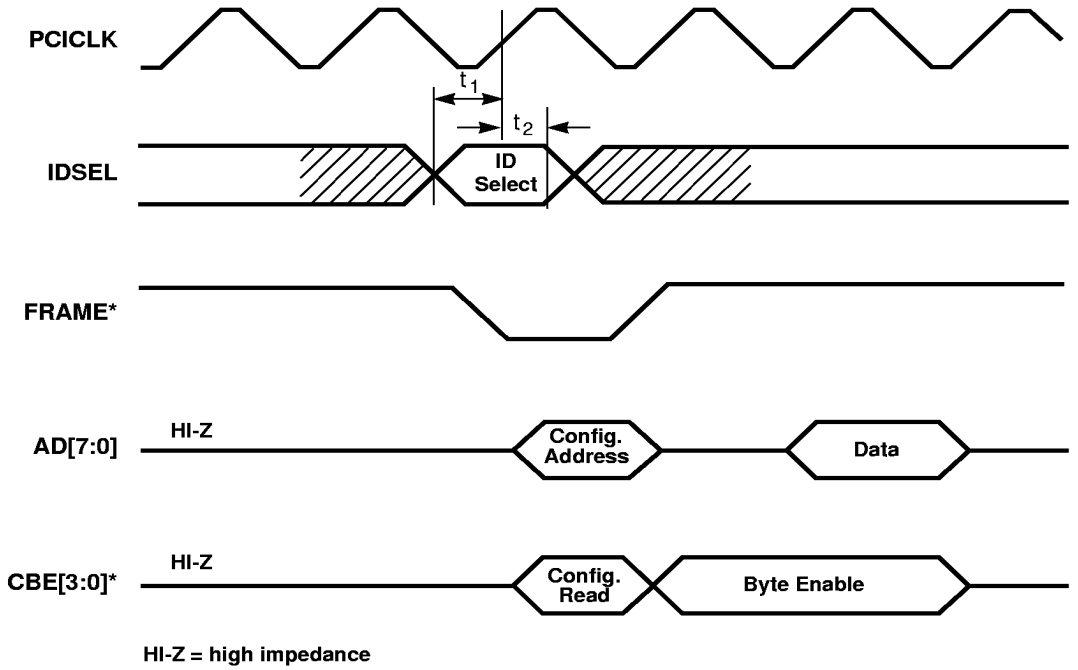


Figure 8-3. IDSEL Timing in a Configuration Cycle

Table 8-6. PAR Timing Diagram

Symbol	Parameter	MIN	MAX	Units
t_1	PAR setup to PCICLK	7	–	ns
t_2	PAR hold from PCICLK	0	–	ns
t_3	PAR valid delay from PCICLK	–	11	ns
t_4	PAR hold from PCICLK	0	–	ns

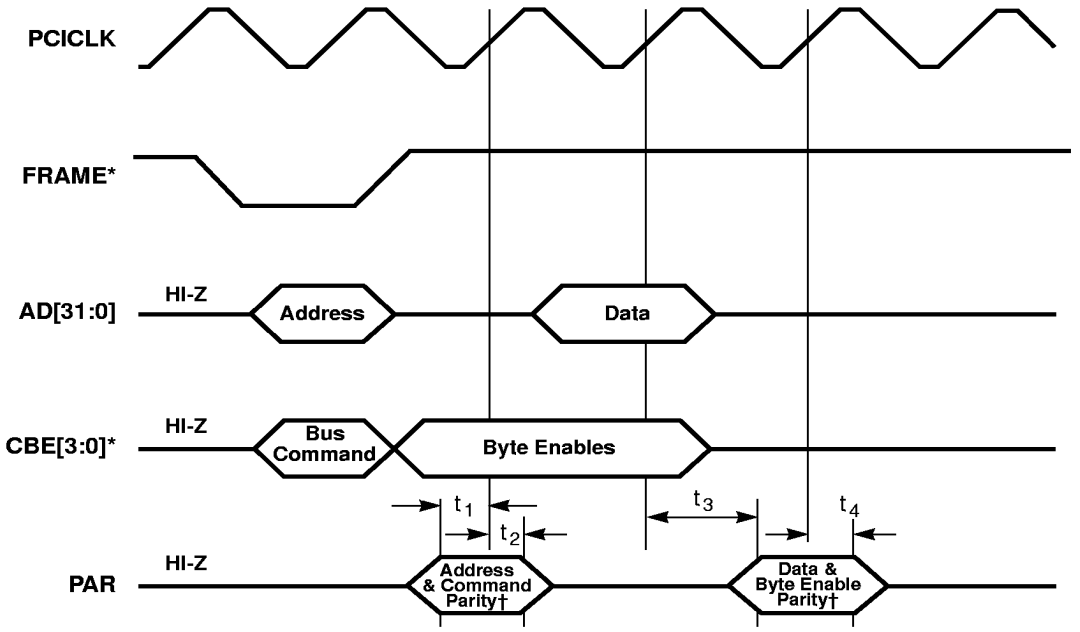


Figure 8-4. PAR Timing Diagram

Table 8-7. DSP Expansion Bus Timing Diagram — Write Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	PA[17:0] address setup time to EPGMWR* low	4	–	ns
t_2	EPGMCS* low to EPGMWR* low setup time	4	–	ns
t_3	PA[17:0] address hold time after EPGMWR* high	5	–	ns
t_4	EPGMWR* high pulse	7	–	ns
t_5	EPGMWR* high to PD[15:0] tristate	0	–	ns
t_6	EPGMWR* low pulse	20	–	ns
t_7	PD[15:0] valid to EPGMWR* high	10	–	ns

NOTE: Expansion bus timing is based on a DSP clock speed of 30.5 MHz.

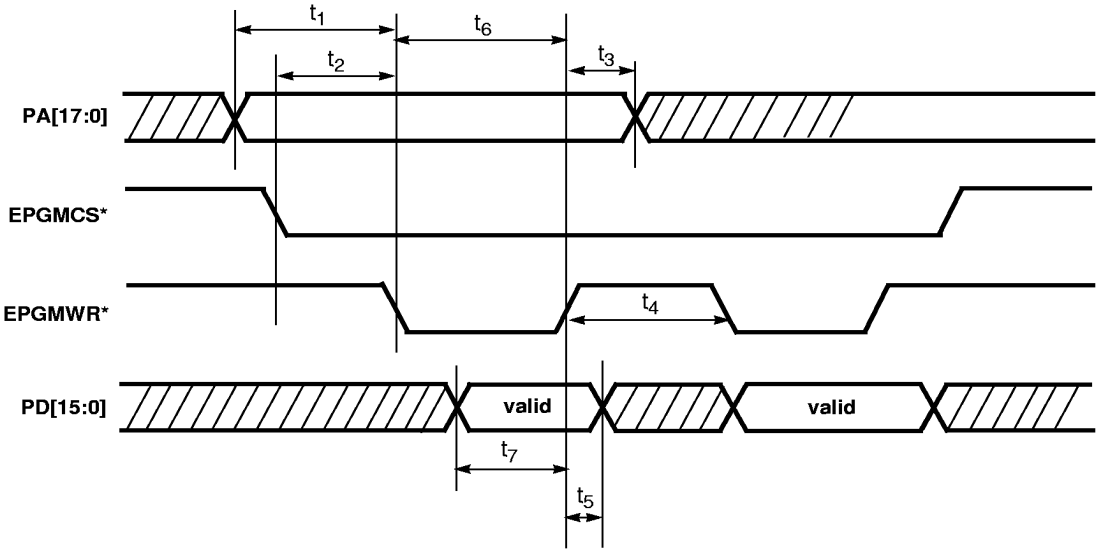


Figure 8-5. DSP Expansion Bus Timing Diagram — Write Cycle

Table 8-8. DSP Expansion Bus Timing Diagram — Read Cycle

Symbol	Parameter	MIN	MAX	Units
t_1	EPGMCS* low to PD[15:0] valid	–	12	ns
t_2	EPGMCS* high to PD[15:0] tristate	0	5	ns
t_3	EPGMCS* low	20	–	ns
t_4	EPGMCS* high when not selected	25	–	ns
t_5	PA[17:0] valid to PD[15:0] valid	—	12	ns
t_6	PD[15:0] hold time	0	–	ns
t_7	PA[17:0] valid	20	–	ns

NOTE: The SRAM's output enable, OE, is connected low. Expansion bus timing is based on a DSP clock speed of 30.5 MHz.

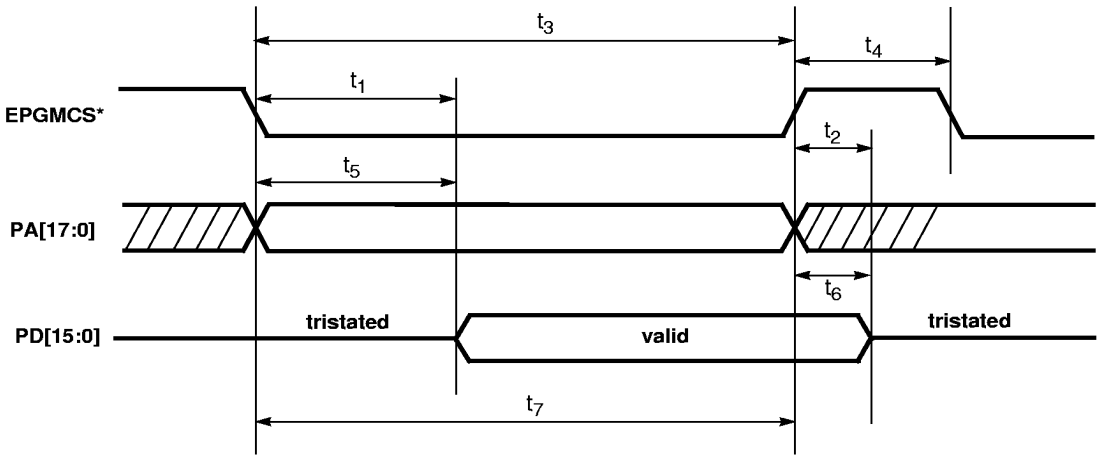
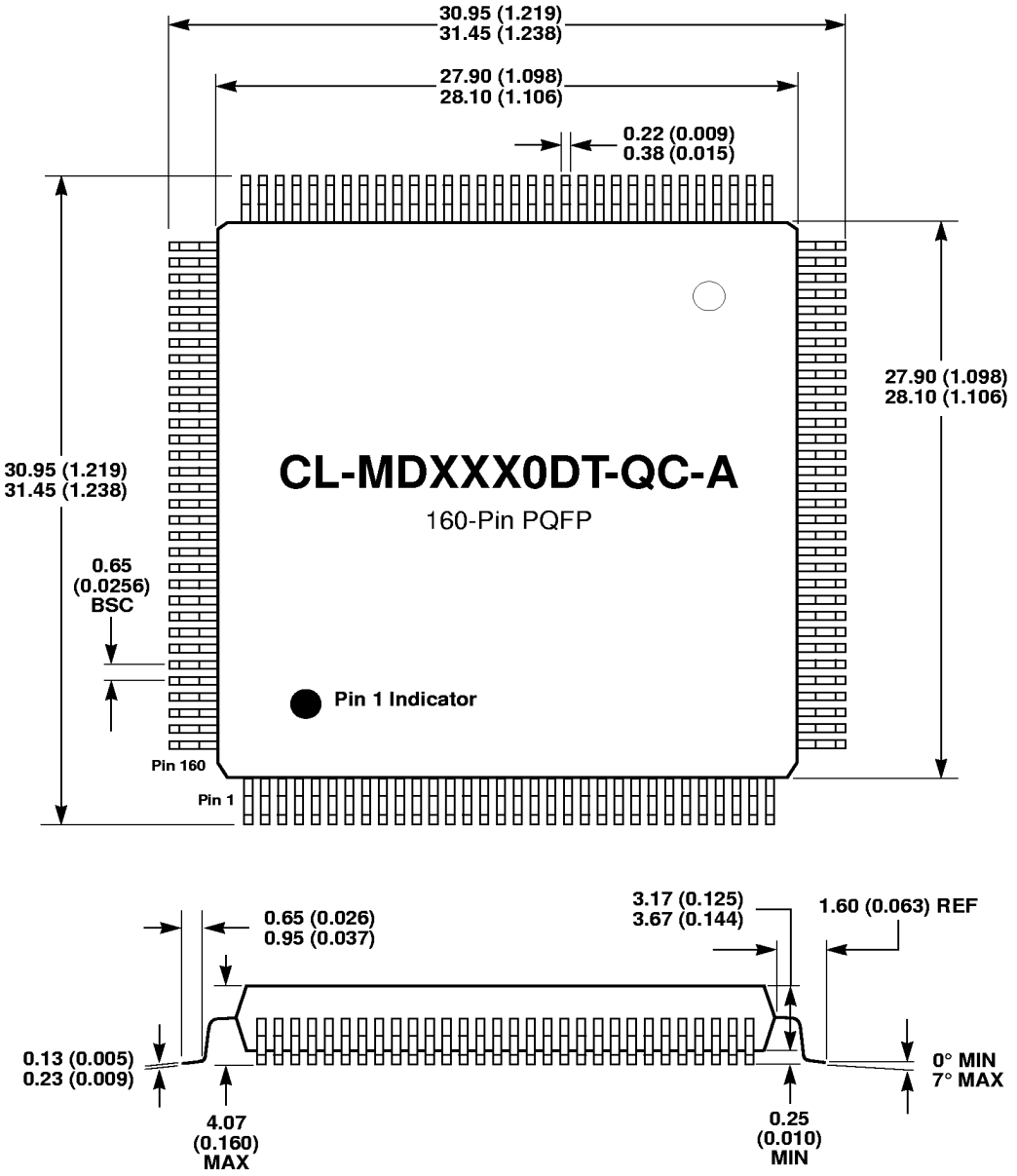


Figure 8-6. DSP Expansion Bus Timing Diagram — Read Cycle

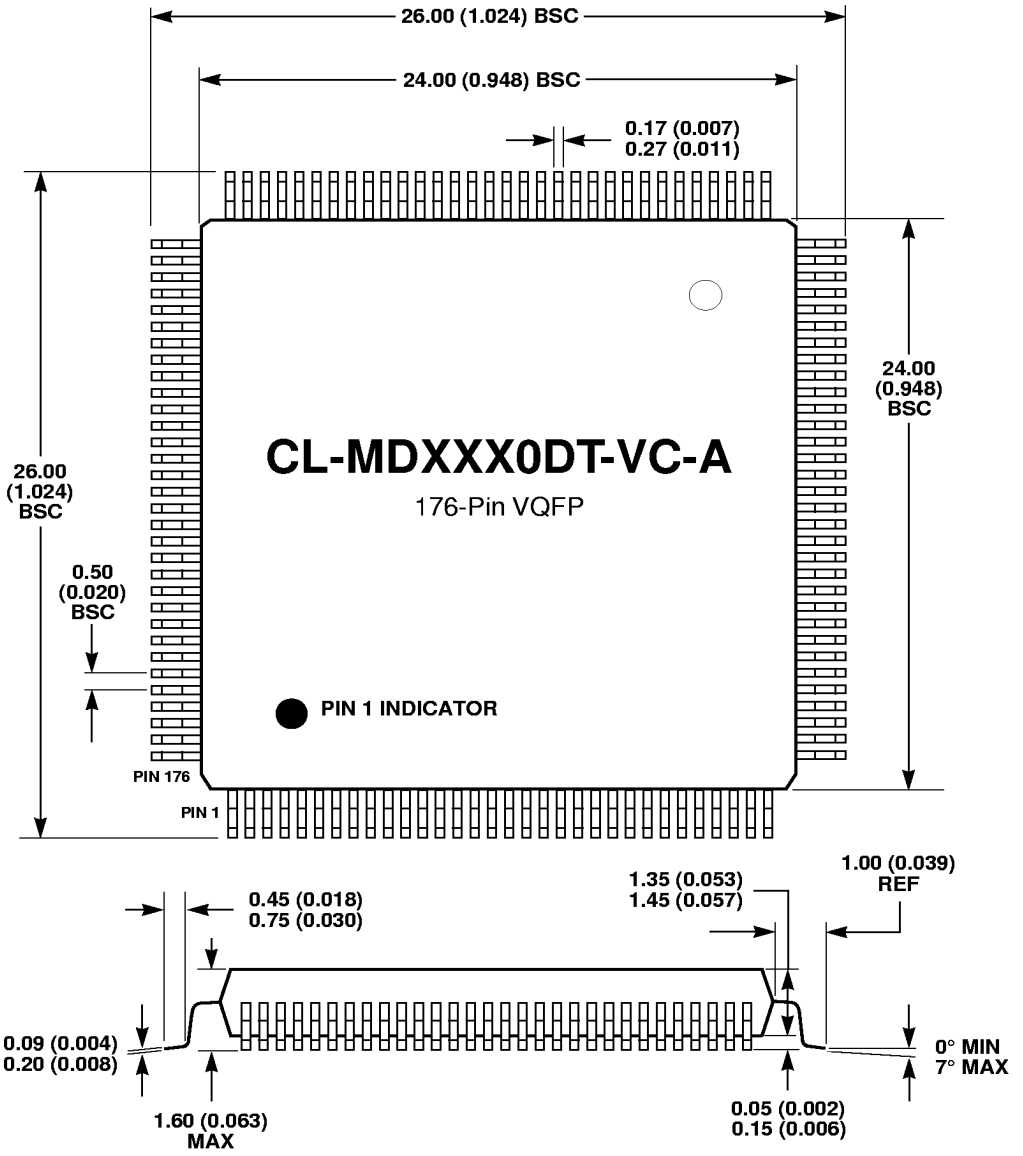
8.6 160-Pin PQFP Package Outline Drawing



NOTES:

1) Dimensions are in millimeters (inches); the controlling dimension is in millimeters.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

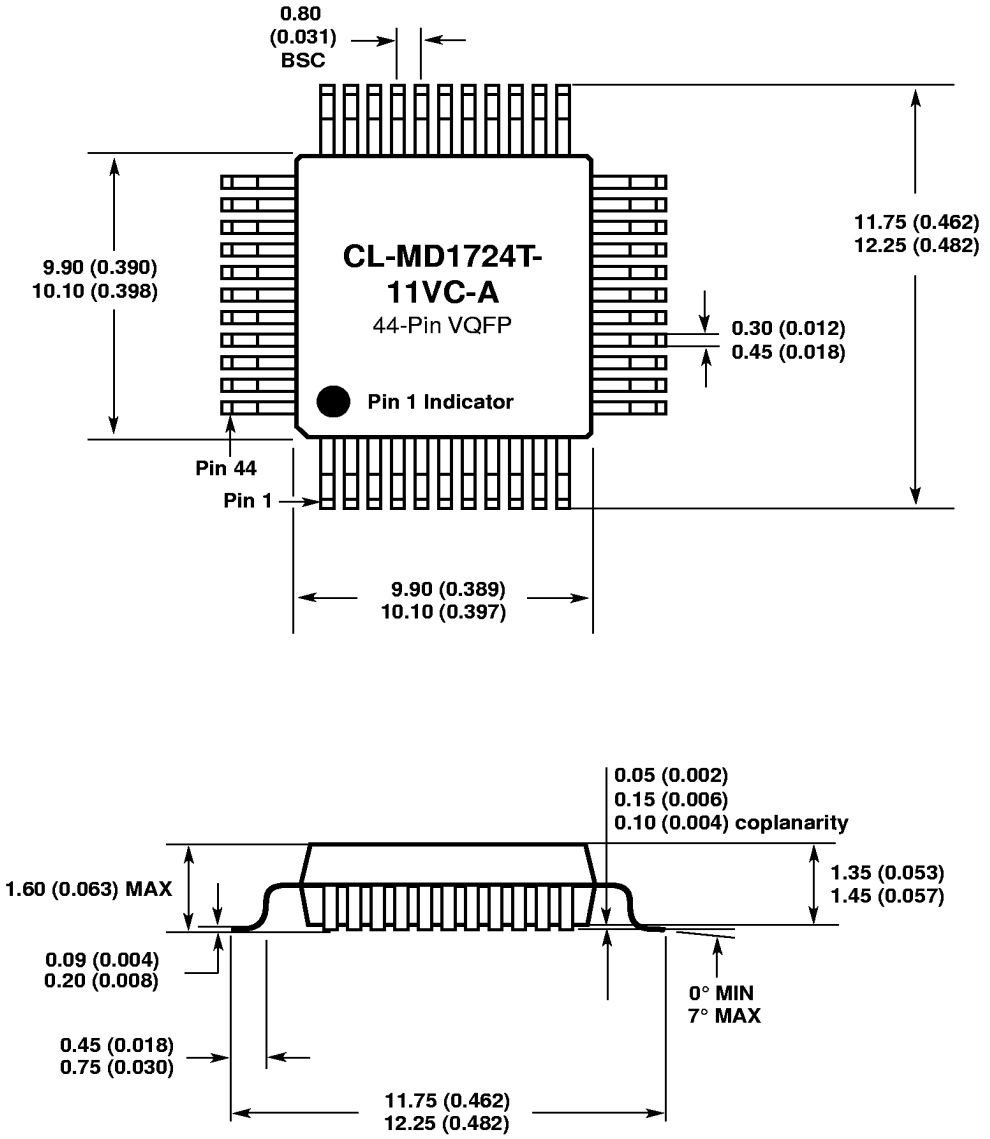
8.7 176-Pin VQFP Package Outline Drawing



NOTES:

1) Dimensions are in millimeters (inches); the controlling dimension is in millimeters.
2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

8.8 44-Pin VQFP Package Outline Drawing



NOTES:

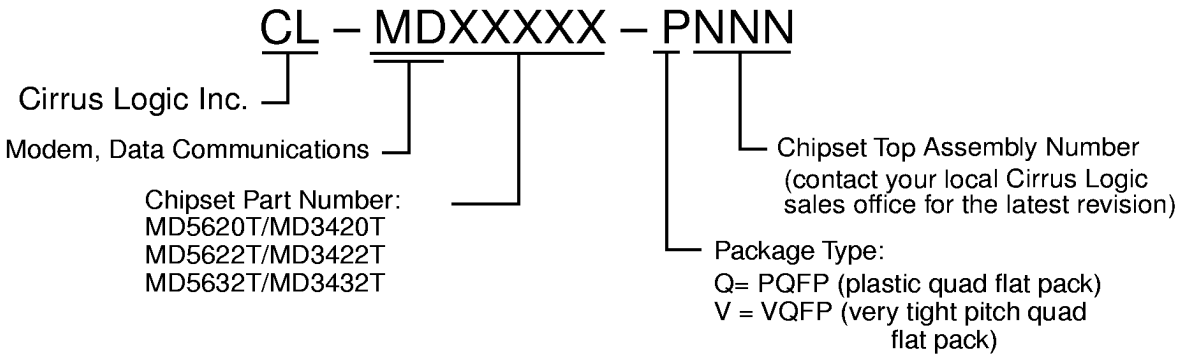
1) Dimensions are in millimeters (inches); the controlling dimension is in millimeters.
2) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

9. ORDERING INFORMATION

Chipset Composition

Features	CL-MD562X	CL-MD342X
Data/fax voice	**CL-MD5620T** **DSP** CL-MD5620DT **SAFE** CL-MD1724T	**CL-MD3420T** **DSP** CL-MD3420DT **SAFE** CL-MD1724T
Data/fax voice, full-duplex speakerphone	**CL-MD5622T** **DSP** CL-MD5620DT **SAFE** CL-MD1724T **SAFE** CL-MD1724T	**CL-MD3422T** **DSP** CL-MD3420DT **SAFE** CL-MD1724T **SAFE** CL-MD1724T
Data/fax voice, full-duplex speakerphone, future DSVD upgrade option	**CL-MD5632T** **DSP** CL-MD5630DT **SAFE** CL-MD1724T **SAFE** CL-MD1724T	**CL-MD3432T** **DSP** CL-MD3430DT **SAFE** CL-MD1724T **SAFE** CL-MD1724T

Chipset Information



Device Information

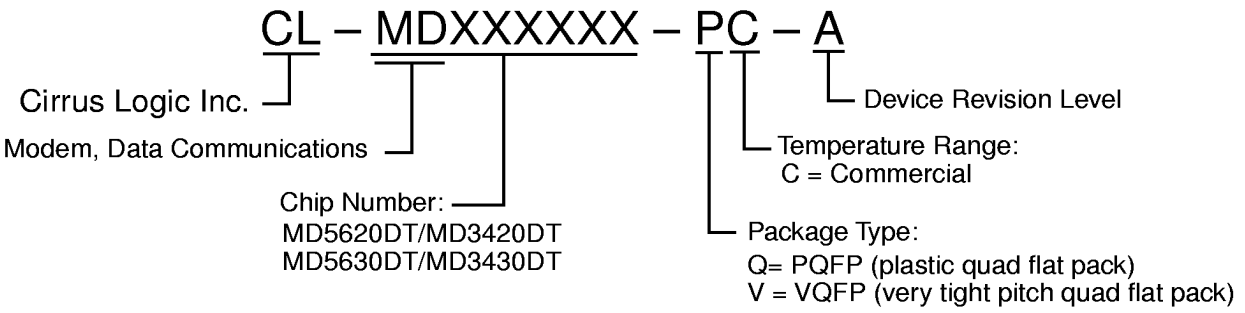


Table 9-1 briefly describes the controllerless modem chipsets. These chipsets are currently available except where indicated.

Table 9-1. Controllerless Modem Chipset Descriptions

Chipsets	Number of Devices	Features
CL-MD5620T/ CL-MD3420T	2	The CL-MD5620T sends data at 33.6 kbps and receives data at up to 56 kbps. The CL-MD3420T sends and receives data at 33.6 kbps. Both chipset types send and receive fax at 14.4 kbps. The chipsets also includs telephone answering machine functions, telephone emulation, and support for Caller ID. Future upgrade option of ITU-V.80 videoconferencing.
CL-MD5622T/ CL-MD3422T	3	Same features as the CL-MD5620T/CL-MD3420T, plus full-duplex Speakerphone mode with internal echo cancellation and an extra SAFE.
CL-MD5632T/ CL-MD3432T	3	Same features as the CL-MD5622T/CL-MD5632T, plus future upgrade of optional ITU-standard V.70 DSVD (digital simultaneous voice and data). These chipsets are currently not available.

10. DAA AND TELEPHONY INTERFACE DESIGN NOTES

DAA components and telephone interfaces are essential components of modem designs. Consider the following circuits and text carefully before designing a modem.

10.1 Data Access Arrangement (DAA) Design

The DAA is the link between the communication equipment and the PSTN (Public Switched Telephone Network). The DAA must perform four basic functions:

1) Provide a path for DC loop current.
2) Provide an AC signal path.
3) Protect the telephone network and the user.
4) Detect ring signals.

All of these functions must be performed within the framework of the *Code of Federal Regulations*, Title 47, Part 15 and Part 68, to obtain the FCC certification required to sell a product in the United States. Other countries have their corresponding requirements. Communications products that are intended for a country other than the United States or for the international market (several different countries) must have DAAs designed to meet the requirements of each country in which they will be sold.

The four DAA functions cannot be entirely separated because of the interdependence of requirements. For example: due to the interdependence of requirements, the AC signal path usually includes a transformer. The transient protection circuitry is limited since it must pass the 150-V_{rms} ring signal, which 'rides' on the 48-V central office battery voltage. Because of the 1500-V isolation barrier required between Tip and Ring (the PSTN) and the equipment, the DAA can be divided into the line (PSTN) side and the equipment side. Any device that crosses this barrier such as transformers, opto-isolators, solid-state switches, relays and the PC board must maintain the proper 1500-V isolation between the PSTN and the equipment.

The following sections provide several design examples and discussion of their design. First, the design of the protective circuitry is discussed. Next, the DC loop current and AC signal current paths are examined. And finally, several ring-detect circuits are illustrated. These sections are tailored to:

- Inform the modem designer about FCC requirements, which must be met by a certifiable design.
- Help develop a design approach.
- Provide usable design examples and parts lists.

10.2 Fault Protection

There are two types of fault protection:

- Components such as the transformer, relays, opto-isolator, and RJ-11 jack are designed to operate under normal circuit conditions and withstand the specified fault conditions without sustaining damage or exposing the user to dangerous voltages.
- Other components such as the MOV (metal-oxide varistor) are designed to remain passive until a fault condition occurs. The MOV is designed to protect the rest of the circuitry and its enclosing system from any harmful effects of the fault. The MOV might become damaged or destroyed in the process.

Two dangerous fault conditions can occur on the phone lines:

1) A lightning strike on or near a phone line. This can result in a large transient voltage between Tip and Ring, or between Tip and Ring and ground.
2) Telephone lines are often strung on power poles underneath power lines. Occurrences such as bad weather, automobile accidents, or earthquakes could cause the power lines to break and make contact with the phone lines, thus exposing telephone users to the second dangerous fault condition.

The *Code of Federal Regulations* Title 47, Part 68.302, specifies the following transient and leakage tests to simulate these potentially dangerous fault conditions:

10.2.1 Metallic Voltage Surge Test

The metallic voltage surge test specifies an 800-V, 10/560-µs pulse (of each polarity) current limited to no less than 100 A, to be applied between Tip and Ring. Protection against this fault is provided by the isolation of the transformer, relays, opto-isolator, and the RJ-11 jack and by the clamping action of the metal-oxide varistor.

10.2.2 Longitudinal Voltage Surge Test

The specification for the longitudinal-surge waveform is a 1500-V peak surge current (of each polarity) limited to not less than 200 A, with a maximum rise time-to-crest of 10 µs and a minimum decay time-to-half crest of 160 µs (for a 1500-V, 10/160-µs pulse). This surge is applied between Tip and Ring, connected to each other and grounded.

10.2.3 Leakage Test

For this test, a 1000-V_{rms} 60-Hz voltage is applied between Tip and Ring, connected to each other and grounded. This voltage is gradually increased from zero to full value over a 30-second period, then applied continuously for 60 seconds. During this test the current drawn from the source may not exceed 10 mA at any time.

After the surge and leakage tests, the modem should still meet the on-hook impedance limitations in the *Code of Federal Regulations*, Title 47, Part 68.312.

10.3 Radiated- and Conducted-Emissions Suppression

Radiated-emissions refers to the electromagnetic energy lost by radiation from the modem/computer combination and the necessary interconnection wiring, such as the modular lines connecting the modem to the wall jack and to the local telephone. *Conducted-emissions* refers to energy lost from the modem by conduction on the phone line or power lines.

The *Code of Federal Regulations,* Title 47, Part 15, places stringent limitations on the emission of radiation from electronic devices. Equipment for this purpose are divided into two broad categories: intentional radiators and unintentional radiators. This modem is considered an unintentional radiator since the radio frequency energy is generated from processing data and is not intended to be broadcast.

Two problems are associated with minimizing conducted and radiated energy:

- First, it is important not to generate any unnecessary radio energy. This is accomplished by keeping lead lengths short and as direct as possible. This minimizes ringing, the lengths of any potential antennas, and the capacitive and transformer coupling of unwanted signals outside the computer enclosure.
- Second, any radio frequency energy necessary for the modem to function or other radiation generated within the computer must be contained. The computer enclosure itself serves as a containment device. Also, the

bracket must be securely connected to both the PC board ground and the computer chassis. L_6–L_8 and L_{12} are intended to block and dissipate unwanted high-frequency signals, thus preventing them from radiating from the modular line connecting the modem to the wall jack, the local phone, the cable connector, or the external speaker. The computer power supply is relied upon to block any radiation appearing on the power lines in the modem.

10.4 Ring Detection

The ring signal for a 'B-type' ringer consists of a 15.3–68.0-Hz, 40–150-V_{rms} sine wave between Tip and Ring. This signal is on for 2 seconds and off for 4 seconds. The ring signal on/off pattern (cadence) repeats until the line is answered or the caller hangs up. This signal is applied between R_1 and C_1, as illustrated in Figure 10-1. On the positive half-cycle (R_1 positive with respect to C_1), D_1 is forward-biased, D_2 breaks down at 18 V, and D_3 is forward-biased. The LED in U_1 is reverse-biased and therefore does not conduct. On the negative half-cycle (R_1 negative with respect to C_1), D_3 is reverse-biased, D_2 is forward-biased, and D_1 breaks down at 18 V. Since D_3 is reverse-biased, the LED in U_1 is forward-biased and provides base current to the opto-isolator transistor. This causes RING* to go to the low or logic '0' state. R_2 serves as a pull-up for RING*. The signal at RING* is approximately a 0–5-V square wave (the saturation voltage of the opto-isolator transistor is approximately 0.2 V) at the ring signal frequency, as illustrated in Figure 10-2 on page 62.

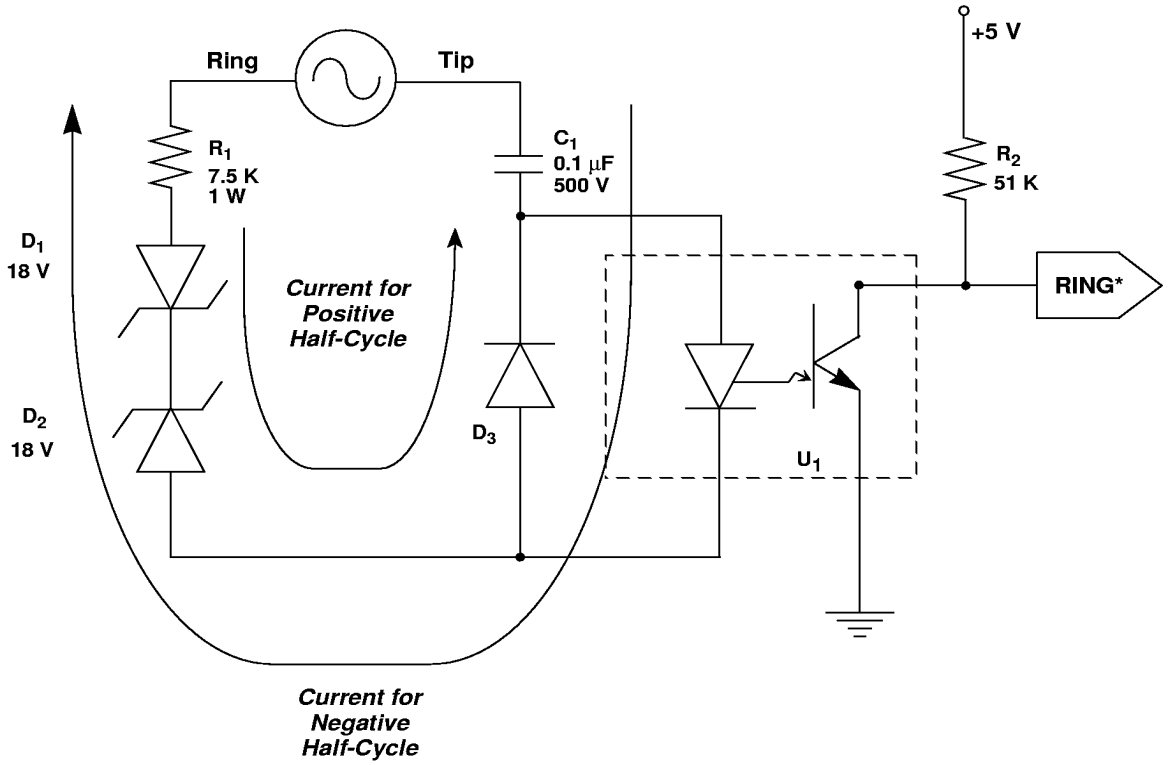


Figure 10-1. Ring Circuit

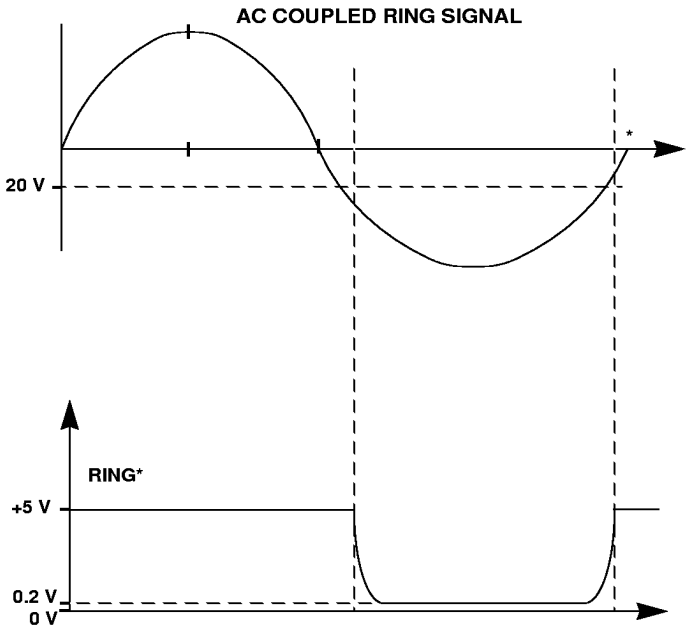


Figure 10-2. AC-Coupled Ring Signal and RING*

10.5 Special Features and Functions

10.5.1 Caller ID

Caller ID is a service that allows the called party to view a caller's phone number before answering the phone. The information transmitted to the called party by Caller ID includes the caller's name, call date, the call time and the calling number. This service is not available everywhere due to central office telephone equipment limitations and legal prohibition in some locations. The subscriber will have to invest in special equipment to receive the Caller ID message sent by the central office.

Caller ID data is sent as Frequency Shift Keying (FSK) data between the first and second ring burst. Since the called party does not want to answer the call until the caller has been identified, the data must be made available to the modem (or other device) without the modem going to the off-hook state. In other words, no DC loop current can be drawn until the called party chooses to answer the call. For this reason, Tip and Ring must be capacitively coupled to the modem during the interval between the first and second ring burst so the modem can decode the Caller ID signal without going off-hook.

A simplified circuit for implementing Caller ID is shown in Figure 10-3 on page 63. It functions as follows: After the first ring burst is decoded by the modem, the CIDREL* output is asserted low. This closes K_2, AC coupling tip to the transformer through C. The Caller ID data is presented to the modem, no DC current flows, and the line remains in the on-hook (unanswered) condition. First, a 250-µs burst of 600-Hz carrier

is sent by the central office followed by a 150-µs burst of 1200-Hz carrier to prepare the modem to receive the Caller-ID data. The 21 data words that comprise the Caller-ID message are transmitted according to the timing illustrated in Figure 10-4. Each word consists of a start bit, eight data bits, and a stop bit. The data must be received and K_2 opened prior to the start of the second ring burst. This is necessary to prevent the large-amplitude ring burst from being applied to the modem's receiver input. Once the data is received, it must be decoded and displayed for the called party to review. If the called party chooses to answer, K_1 closes, DC loop current flows, and the line goes to the off-hook state.

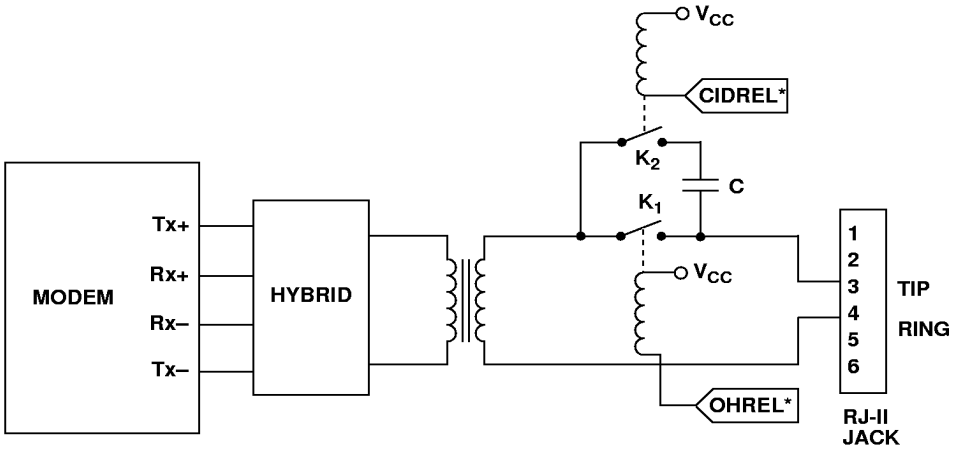


Figure 10-3. Caller ID Interface

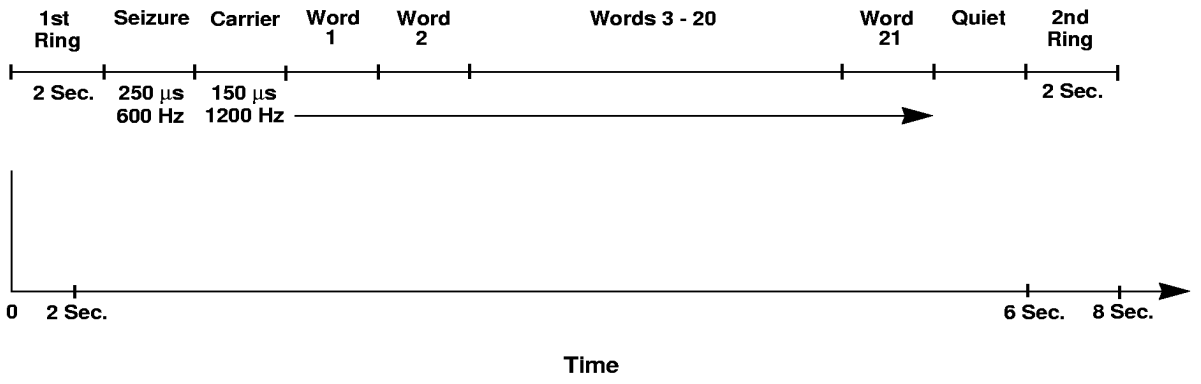


Figure 10-4. Caller ID Signal Timing

Table 10–1. Caller ID Message Transmission Order

Word Number	Word Description			Data Received 7	6	5	4	3	2	1	0
1	Message type — CND			0	0	0	0	0	1	0	0
2	Data words to follow — 18			0	0	0	1	0	0	1	0
3	Call Date	Month	0	0	0	0	0	0	0	0	0
4			2	0	0	0	0	0	0	1	0
5		Day	1	0	0	0	0	0	0	0	1
6			5	0	0	0	0	0	1	0	1
7	Call Time	Hour	1	0	0	0	0	0	0	0	1
8			0	0	0	0	0	0	0	0	0
9		Minute	1	0	0	0	0	0	0	0	1
10			5	0	0	0	0	0	1	0	1
11	Calling Number	Area Code	4	0	0	0	0	0	1	0	0
12			0	0	0	0	0	0	0	0	0
13			8	0	0	0	0	1	0	0	0
14		Number	9	0	0	0	0	1	0	0	1
15			4	0	0	0	0	0	1	0	0
16			5	0	0	0	0	0	1	0	1
17			0	0	0	0	0	1	0	0	0
18			8	0	0	0	0	0	0	1	1
19			3	0	0	0	0	0	0	0	0
20			0 0	0	0	0	0	0	0	0	0
21	Checksum			0	1	0	0	1	1	1	0

Several potentially useful options are possible in conjunction with Caller ID. The modem, computer, and application software can be configured to maintain a running log of numbers calling the modem and indicate whether the call was completed, whether a message was left, and how many times the phone rang. This information could be useful to determine peak hours of phone traffic, estimate staff efficiency, determine the desirability of an 800 number, or allowing missed calls to be answered. The computer could be set up to screen calls. The ringer could be deactivated if an incoming call is not on the approved list. For example, if an important call was expected from a client, all other calls could be screened.

10.6 Voice Interface

There are several methods to provide a voice interface to Cirrus Logic data/fax/voice modems. Many of these impact the DAA design. This section will present several alternative voice interfaces. These will include interfacing a handset/headset with a CL-MD1724T (which includes a microphone input), interfacing the local telephone, and options for Telephone Emulation mode. A remote voice connection using the CL-MD1724T (recording and playing back voice messages from a remote phone) requires no additional circuitry. Messages always can be played back through the speaker. The microphone pins on the CL-MD1724T can be connected directly to ground.

10.6.1 Local Phone Voice Interface

As illustrated in Figure 10-5, the local phone is biased when the modem is in the Local Voice mode. Current flows from the computer's +12 V power supply through the filter network consisting of L_3, R_{15}, C_{19}, and C_{20}, K_2 to the phone, T_1 and K_1 to ground. Most phones tested, including speakerphones, will function with a bias current of approximately 40 mA. At this current, 7–8 V will appear across the phone. The filter component values were chosen empirically to minimize the audible noise due to the electrical noise on the computer's +12-V power supply.

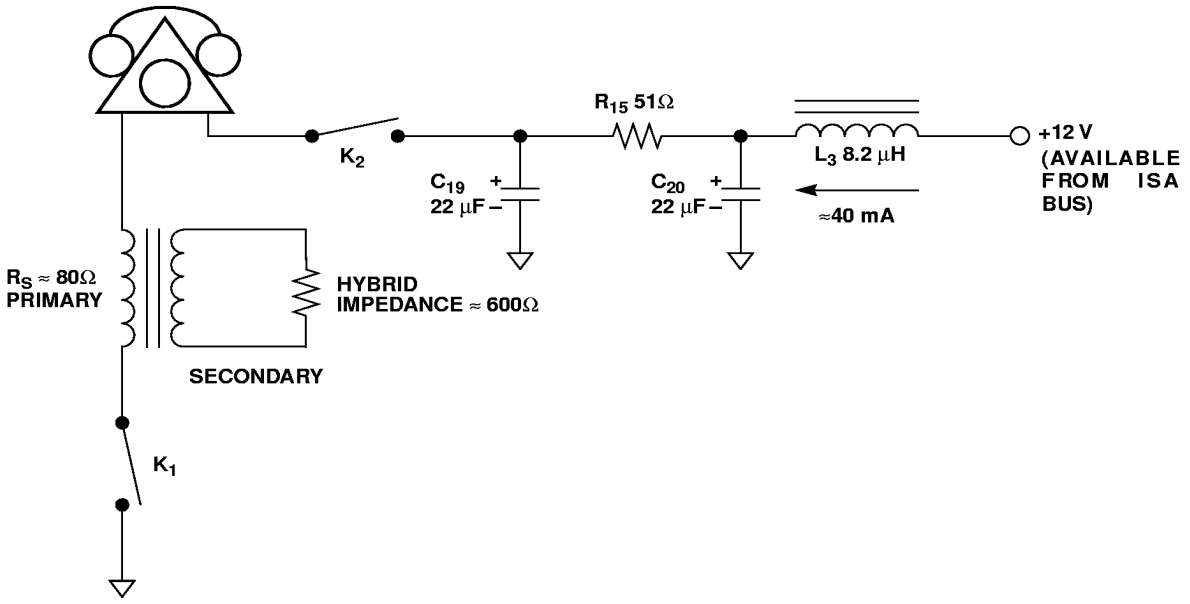
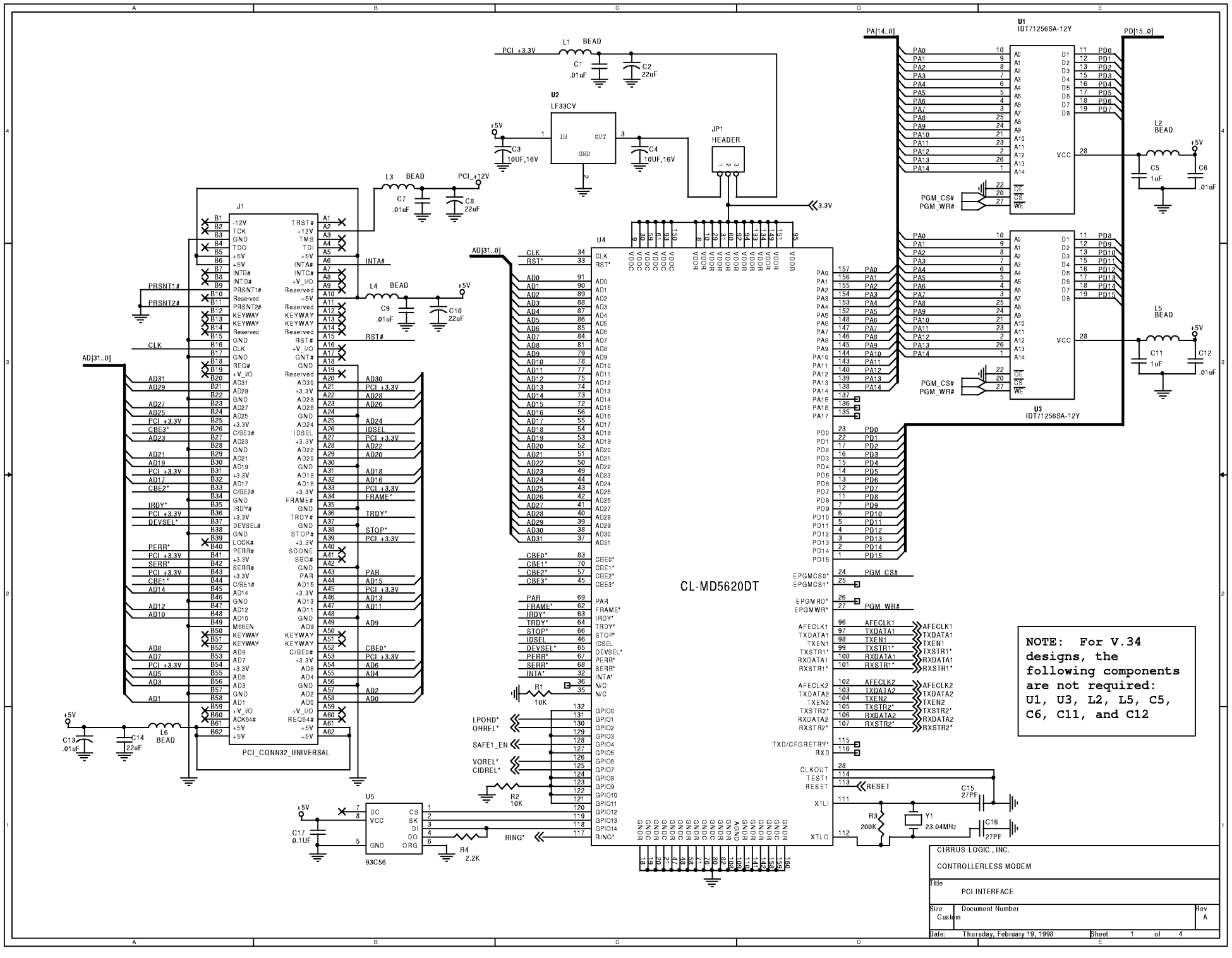


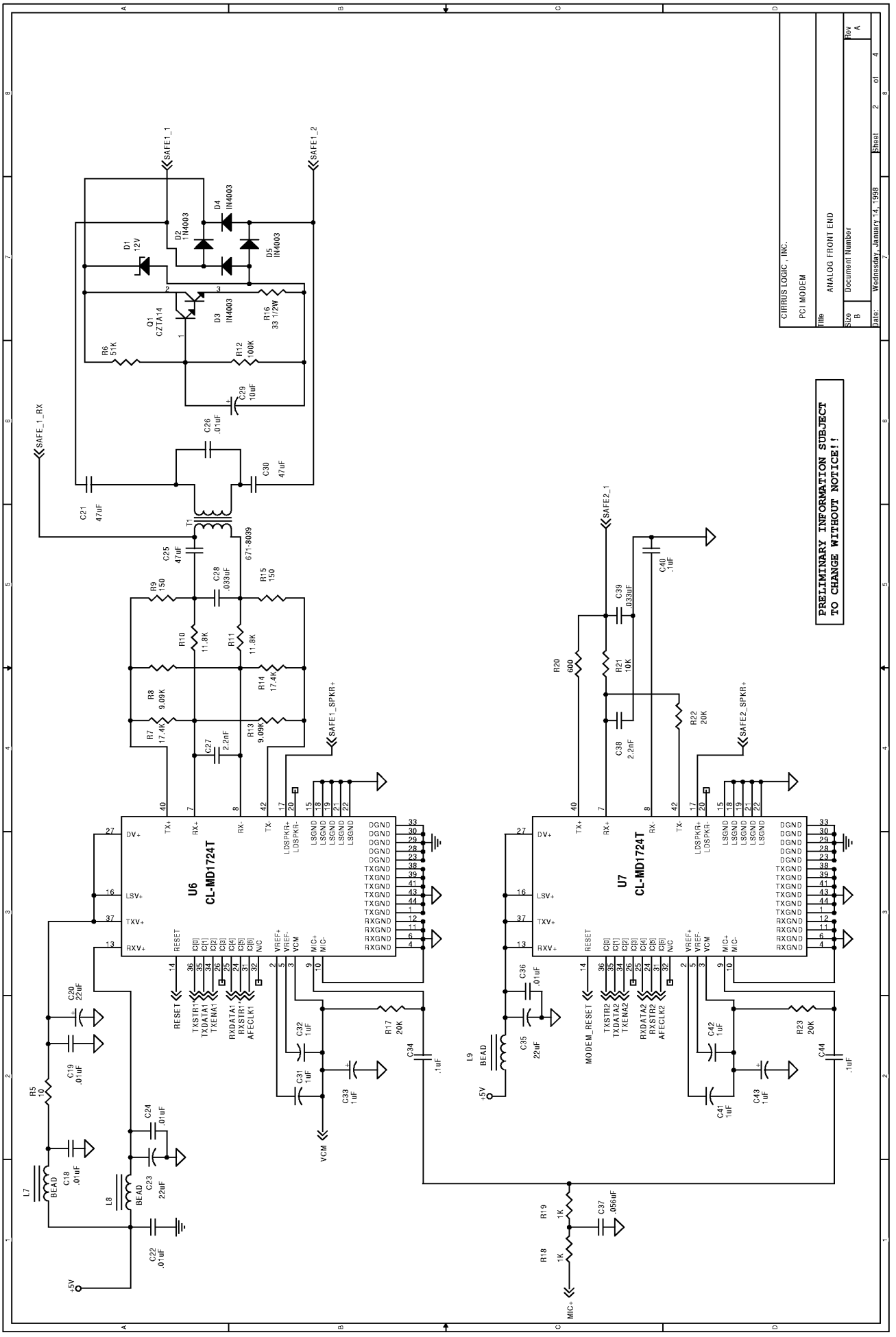
Figure 10-5. Local Phone in Voice Mode

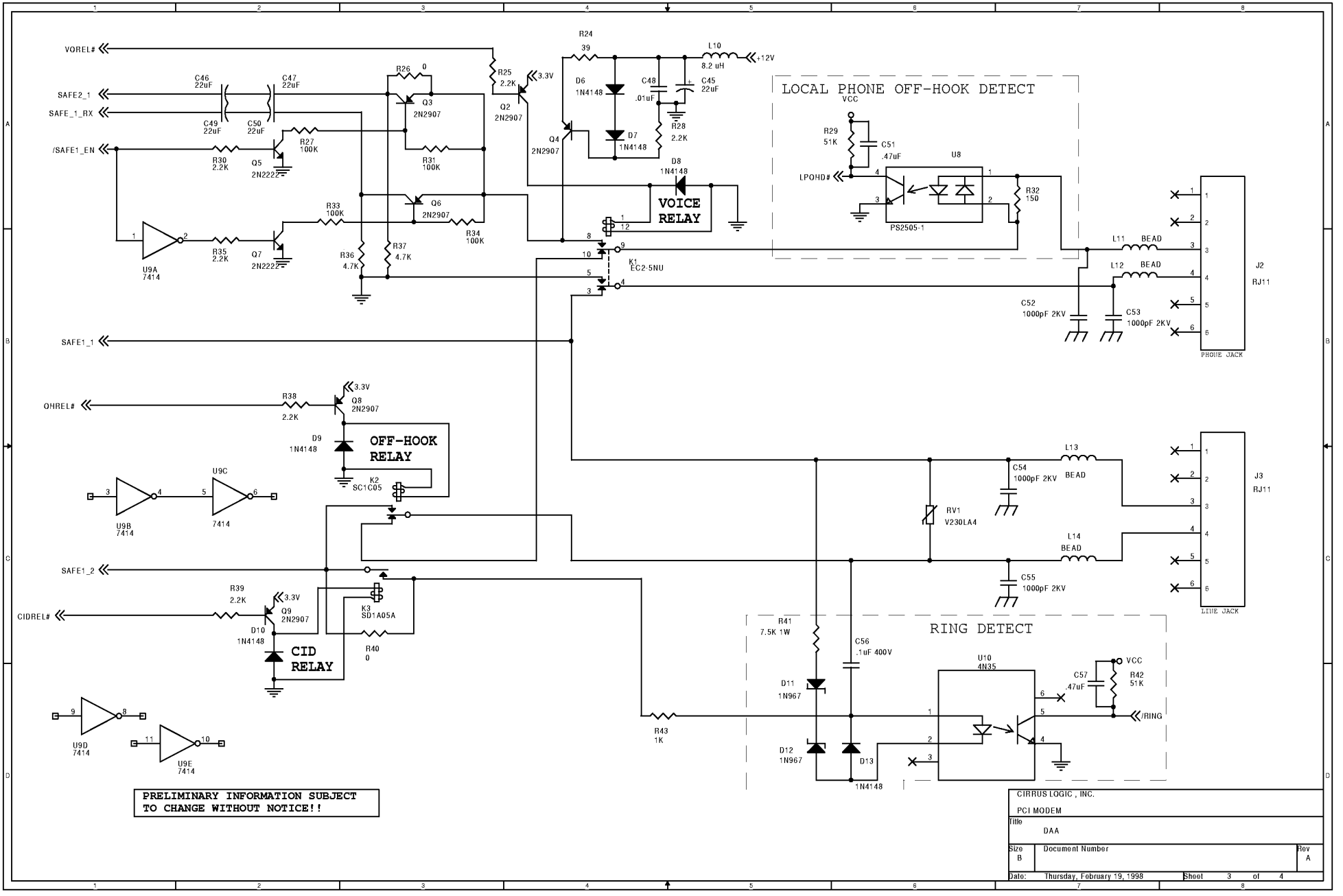
Mechanical relays are required in this application because the local phone and the primary side of the transformer are being switched between Tip and Ring and the +12 V and ground of the computer. 1500 V of isolation must be maintained between the computer ground (and +12 V) to pass the FCC's Part 68 leakage test. Therefore, the relay chosen for this application must have a minimum contact-to-contact breakdown of 1500 V. This requirement precludes the use of solid-state relays. Solid-state relays can be used in lineside applications only when switching Tip and Ring. In this case, the 1500 V appears as a common mode voltage simultaneously on both sides of the switch. The high-voltage isolation is then between both switch contacts and the LED, which is the mode in which solid-state relays were intended to be used.

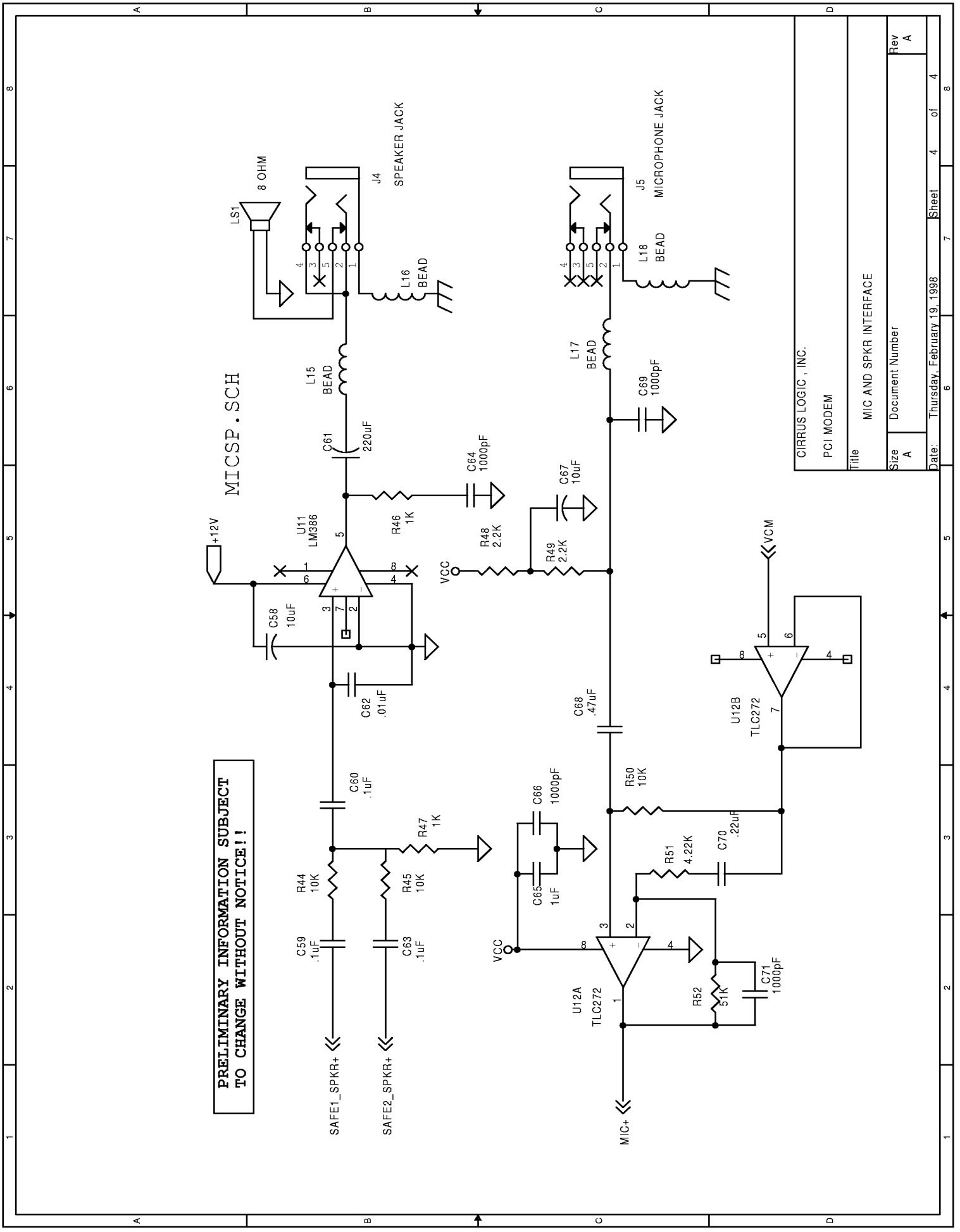
Appendix A

Schematics









Appendix B

Bill of Materials

Bill Of Materials

* For a V.34 design, Item #56 is not required.

Item	Quantity	Reference	Part
1	16	C1,C5,C6,C7,C9,C11,C12,	.01uF SMD 0805, 10 %
		C14,C18,C19,C22,C24,C26,	Vitramon VJ0805Y103KXXAR
		C36,C48,C62	
2	12	C2,C8,C10,C13,C20,C23,	22uF Thru Hole, Electrolytic 50V
		C35,C45,C46,C47,C49,C50	Panasonic ECE-A1HU220
3	2	C3,C4	10uF Thru Hole, Electrolytic 50V
			Panasonic ECE-A1HU100
4	2	C16,C15	27pF SMD 0805, 10 %
			Vitramon VJ0805A270KXAAR
5	3	C21,C25,C30	47uF Non Polar, 35V TH, .150”
			Panasonic ECE-A1VN470U
6	2	C27,C38	2200pF Thru Hole COG, .100"ls
			Panasonic ECU-S1J222JCB
7	2	C28,C39	0.033uF TH, 0.200" ls, Metalized Poly Film
			Panasonic ECQ-E1333KF
8	3	C29,C58,C67	10uF Thru Hole, Electrolytic 50V
			Panasonic ECE-A1HU100
9	7	C31,C32,C33,C41,C42,C43,	1uF Thru Hole, Electrolytic 50V
		C65	Panasonic ECE-A1HU010
10	7	C17,C34,C40,C44,C59,C60,C63	0.1uF, SMD 0805, 10%
			Vitramon VJ0805Y104KXXAR
11	1	C37	.056uF SMD 50V X7R, 0805
			Johanson Dielectric 500R15W563JV4E
12	3	C51,C57,C68	.47uF SMD 1206
			Vitramon VJ1206U474MXXAR
13	4	C52,C53,C54,C55	1000pF 2KV, Thru Hole 6.35mm LS
			NIC Component Corp. NCD103K2KVY5PC
14	1	C56	.1uF 400V, Thru Hole .400"ls
			Panasonic ECQ-E4104KF
15	1	C61	220uF, 16V, TH, ELT (6.3 X 11), 20%
			NIC COMPONENT CORP.NRSA221M16V
16	4	C64,C66,C69,C71	1000pF, SMD 0805, 10%
			Vitramon VJ0805Y102KXXAR

Bill Of Materials

Item	Quantity	Reference	Part
17	1	C70	.22uF,X7R, 25V, SMD 1206, 10%
			Vitramon VJ1206Y224KXXMR
18	1	D1	Zener Diode 12V, ThruHole
19	4	D2,D3,D4,D5	Bridge Diodes
			1N4004
20	6	D6,D7,D8,D9,D10,D13	Diode 1N4148, Thru-Hole
21	2	D12,D11	Zener Diode 18V, Thru-Hole
			LITEON, 1N5248BCT
22	1	JP1	HEADER 1 X 3, .100 ls
23	2	J3,J2	RJ11 Modular Jack
			Maxconn MJL-64
24	2	J4,J5	AUDIO JACKS
			Singatron SJ-372
25	1	K1	DPDT Single Coil Latch Relay
			NEC EC2-5NJ
26	1	K2	REED RELAY 1Form C, Thru-Hole
			EAC, SC1C05
27	1	K3	REED RELAY 1Form A, Thru-Hole
			EAC, SD1A05A
28	1	LS1	8 OHM
29	15	L1,L2,L3,L5,L7,L8,	0805 FERRITE BEAD
		L9,L11,L12,L13,L14,L15,	
		L16,L17,L18	
30	2	L4,L6	1210 FERRITE BEAD
31	1	L10	8.2 uH SMD, 1210
			KOA KL32TE8R2J
32	1	Q1	NPN Darlington SMD SOT-223
			Central Semiconductor CZTA14
33	6	Q2,Q3,Q4,Q6,Q8,Q9	PNP Transistor SMD, SOT-23
			Central Semiconductor CMPT2907A
34	2	Q5,Q7	NPN Transistor SMD, SOT-23
			Central Semiconductor CMPT2222A

Bill Of Materials

Item	Quantity	Reference	Part
35	1	RV1	Surge Protector, Thru-Hole
			Panasonic ERZ-V05D221
36	6	R1,R2,R21,R44,R45,R50	10K SMD 0805, 5%
			KOA Speer RK73H2AT1002F
37	1	R3	200K, SMD 0805, 5%
			KOA Speer RK73H2AT2003F
38	9	R4,R25,R28,R30,R35,R38,	2.2K SMD 0805, 5%
		R39,R48,R49	KOA Speer RK73H2AT2201F
39	1	R5	10 Ohms, SMD 0805, 5%
			KOA Speer RK73H2AT10R0F
40	4	R6,R29,R42,R52	51K, SMD 0805, 5%
			KOA Speer RK73H2AT5102F
41	2	R14,R7	17.4K, SMD 0805, 1%
			KOA Speer RK73H2AT1742F
42	2	R8,R13	9.09K, SMD 0805, 1%
			KOA Speer RK73H2AT9091F
43	3	R9,R15,R32	150 SMD 0805, 5%
			KOA Speer RK73H2AT1500F
44	2	R11,R10	11.8K, SMD 0805, 1%
			KOA Speer RK73H2AT1182F
45	5	R12,R27,R31,R33,R34	100K, SMD 0805, 5%
			KOA Speer RK73H2AT1003F
46	1	R16	33 Ohm 1/2W, SMD 2010, 1%
			KOA Speer RK73H2H33R0F
47	3	R17,R22,R23	20K SMD 0805, 5%
			KOA Speer RK73H2AT2002F
48	5	R18,R19,R43,R46,R47	1K SMD 0805, 5%
			KOA Speer RK73H2AT1001F
49	1	R20	600 SMD 0805, 5%
			KOA Speer RK73H2AT6000F
50	1	R24	39 Ohm, SMD 0805
51	2	R26,R40	0 Ohm, SMD 0805
52	2	R37,R36	4.7K SMD 0805, 5%
			KOA Speer RK73H2AT4701F

Bill Of Materials

Item	Quantity	Reference	Part
53	1	R41	7.5K 1/2W SMD 2010, 1 %
			KOA Speer RK73H2H7501F
54	1	R51	4.22K SMD 0805, 1%
			KOA SPEER RK73H2AT4221F
55	1	T1	Transformer Midcom 671-8039
56	2	U1,U3	32K X 16 12nS, SRAM, SMD SOJ-28 .300"
		Note: this item not required for	ISSI P/N#IS61C256AH-12
		V.34 designs	
57	1	U2	3.3 Voltage Regulator, TO-220
			SGS Thomson LF33CV
58	1	U4	Cirrus Logic DSP, CL-MD5620DT,
			160-pin SMD
59	1	U5	EEPROM,8-Pin SOIC
			ATMEL AT93C56-10SC
60	2	U6,U7	Cirrus Logic Analog Front End, 44 Pin VQFP
61	1	U8	AC OptoCoupler 4 Pin Thru Hole
			PS2505 NEC
62	1	U9	Hex Inverters 74HC14
			SMD 14 Pin SOIC
63	1	U10	Opto Coupler 6 Pin Thru Hole
			4N35 QT Optoelectronics
64	1	U11	Audio Power Amp, SOIC 8-pin
			National Semi. LM386M-1
65	1	U12	OP-AMP, SOIC 8 pin
			Texas Instruments TLC272CD
66	1	Y1	23.04MHz, CRYSTAL
			Abracon ABL-23.04MHz, AT-49/U (18pF)
			TOTAL TOLERANCE = +/- 50ppm

Notes

Notes

Direct Sales Offices

Domestic

N. CALIFORNIA
Fremont
TEL: 510/623-8300
FAX: 510/252-6020

S. CALIFORNIA
Westlake Village
TEL: 805/371-5860
FAX: 805/371-5861

NORTHWESTERN AREA
Portland, OR
TEL: 503/620-5547
FAX: 503/620-5665

SOUTH CENTRAL AREA
Austin, TX
TEL: 512/255-0080
FAX: 512/255-0733

Irving, TX
TEL: 972/252-6698
FAX: 972/252-5681

Houston, TX
TEL: 281/257-2525
FAX: 281/257-2555

NORTHEASTERN AREA
Andover, MA
TEL: 978/794-9992
FAX: 978/794-9998

SOUTHEASTERN AREA
Raleigh, NC
TEL: 919/859-5210
FAX: 919/859-5334

Boca Raton, FL
TEL: 561/241-2364
FAX: 561/241-7990

International

CHINA
Beijing
TEL: 86/10-6428-0783
FAX: 86/10-6428-0786

FRANCE
Paris
TEL: 33/1-48-12-2812
FAX: 33/1-48-12-2810

GERMANY
Herrsching
TEL: 49/81-52-92460
FAX: 49/81-52-924699

HONG KONG
Tsimshatsui
TEL: 852/2376-0801
FAX: 852/2375-1202

ITALY
Milan
TEL: 39/2-3360-5458
FAX: 39/2-3360-5426

JAPAN
Tokyo
TEL: 81/3-3340-9111
FAX: 81/3-3340-9120

KOREA
Seoul
TEL: 82/2-565-8561
FAX: 82/2-565-8565

SINGAPORE
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