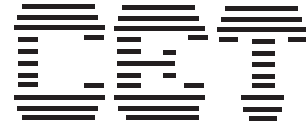


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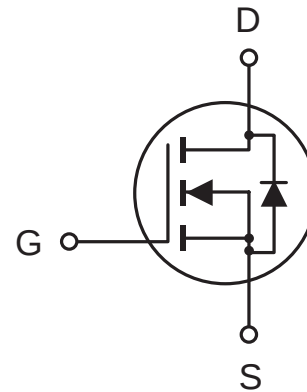
PRELIMINARY

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N-Channel Logic Level Enhancement Mode Field Effect Transistor

FEATURES

- 30V , 100A , $R_{DS(ON)} = 4.5m\Omega$ @ $V_{GS}=10V$.
 $R_{DS(ON)} = 6.0m\Omega$ @ $V_{GS}=4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous -Pulsed	I_D	100	A
	I_{DM}	300	A
Drain-Source Diode Forward Current	I_S	100	A
Maximum Power Dissipation @ $T_c=25^\circ\text{C}$ Derate above 25°C	P_D	107	W
		0.71	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.4	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

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ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
ON CHARACTERISTICS ^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1		3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 50A		3.9	4.5	mΩ
		V _{GS} = 4.5V, I _D = 40A		4.8	6.0	mΩ
On-State Drain Current	I _{D(ON)}	V _{GS} = 10V, V _{DS} = 10V	100			A
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D = 26A		32		S
DYNAMIC CHARACTERISTICS ^b						
Input Capacitance	C _{ISS}	V _{DS} =15V, V _{GS} = 0V f =1.0MHz		4800		pF
Output Capacitance	C _{OSS}			1480		pF
Reverse Transfer Capacitance	C _{RSS}			170		pF
SWITCHING CHARACTERISTICS ^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 15V, I _D =52A, V _{GS} = 10V R _{GEN} =24Ω		10	25	ns
Rise Time	t _r			100	150	ns
Turn-Off Delay Time	t _{D(OFF)}			100	140	ns
Fall Time	t _f			110	150	ns
Total Gate Charge	Q _g	V _{DS} =15V, I _D = 50A, V _{GS} =5V		50	70	nC
Gate-Source Charge	Q _{gs}			8		nC
Gate-Drain Charge	Q _{gd}			35		nC

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ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS^a						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 50A$			1.3	V

Notes

a. Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

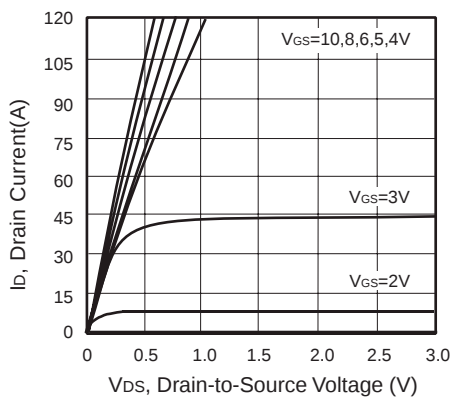


Figure 1. Output Characteristics

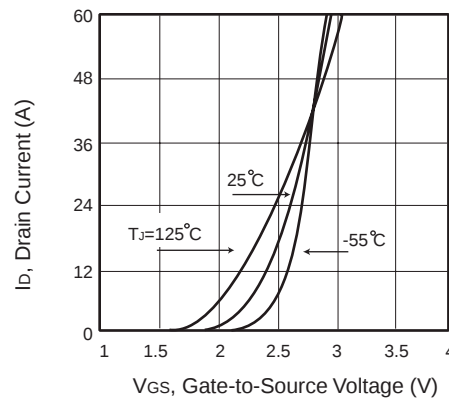


Figure 2. Transfer Characteristics

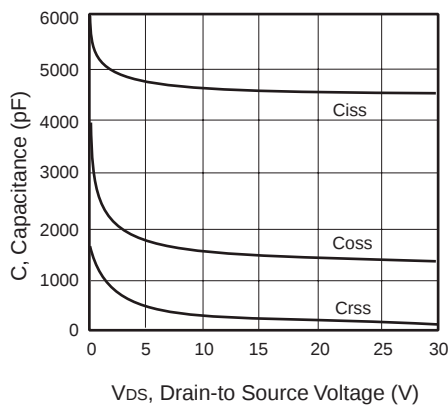


Figure 3. Capacitance

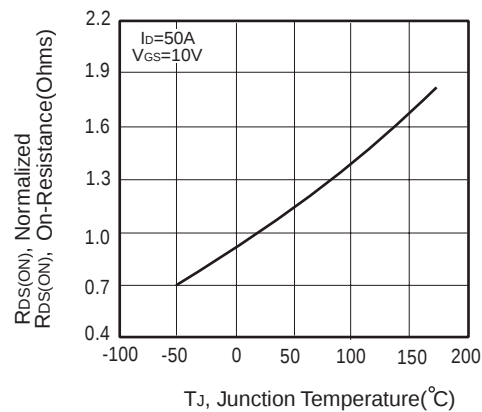
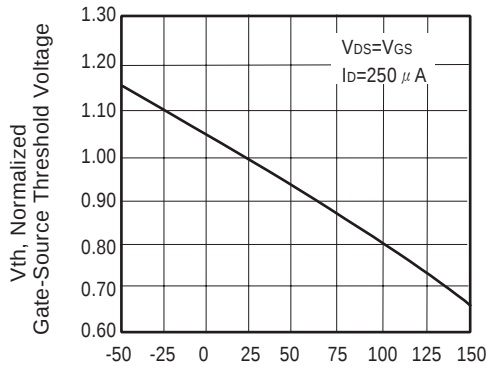


Figure 4. On-Resistance Variation with Temperature

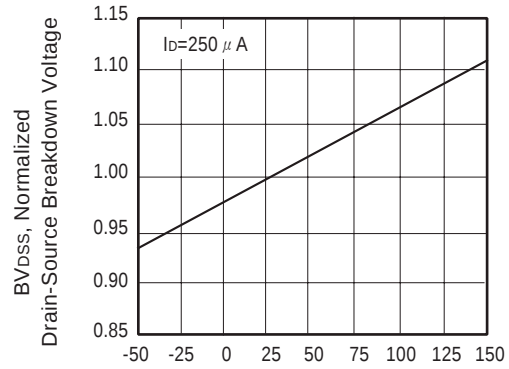
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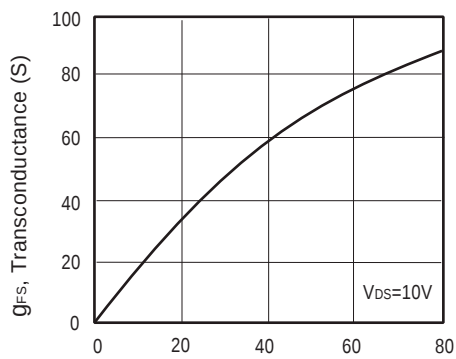
Tj, Junction Temperature (°C)

Figure 5. Gate Threshold Variation with Temperature



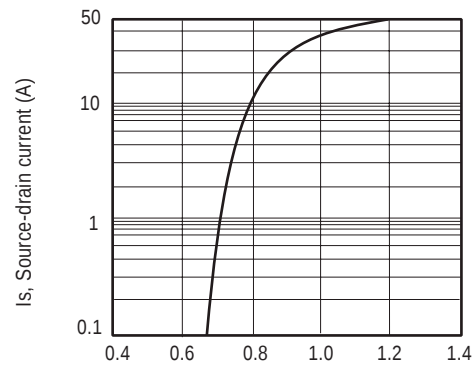
Tj, Junction Temperature (°C)

Figure 6. Breakdown Voltage Variation with Temperature



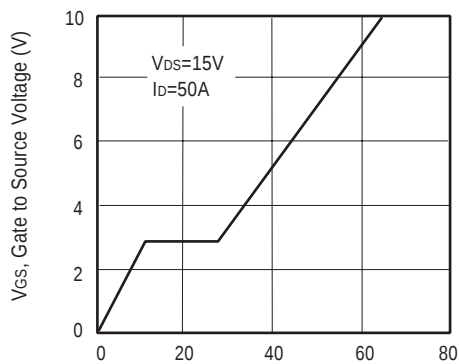
Ids, Drain-Source Current (A)

Figure 7. Transconductance Variation with Drain Current



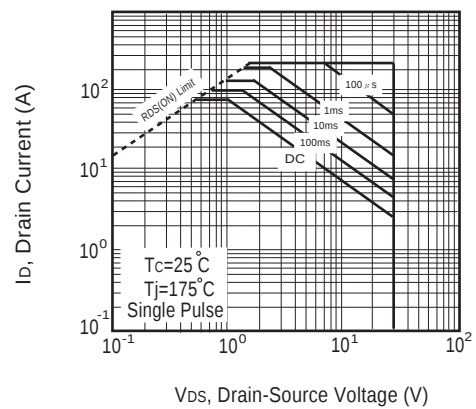
Vsd, Body Diode Forward Voltage (V)

Figure 8. Body Diode Forward Voltage Variation with Source Current



Qg, Total Gate Charge (nC)

Figure 9. Gate Charge



Vds, Drain-Source Voltage (V)

Figure 10. Maximum Safe Operating Area

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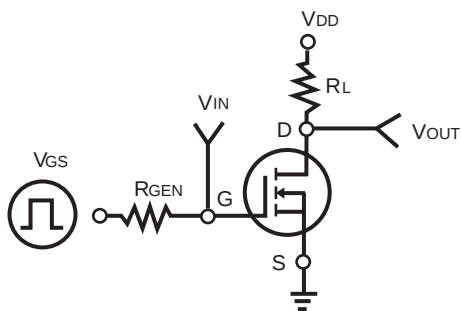


Figure 11. Switching Test Circuit

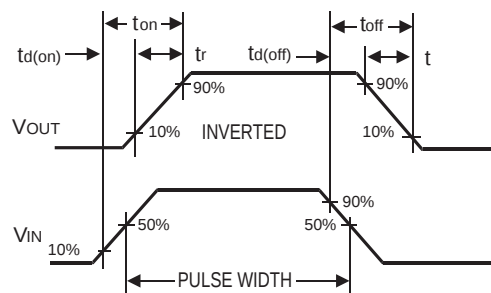


Figure 12. Switching Waveforms

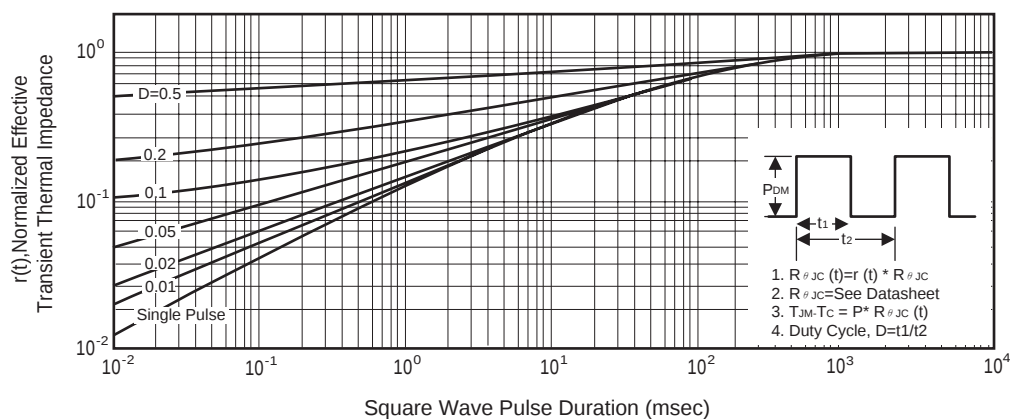


Figure 13. Normalized Thermal Transient Impedance Curve