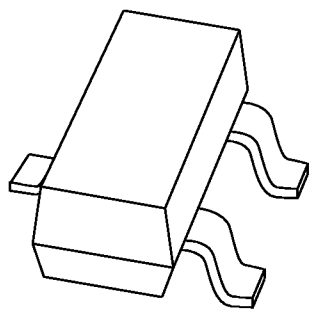
DATA SHEET



BSH204
P-channel enhancement mode MOS transistor

Objective specification
File under Discrete Semiconductors, SC13b

1997 Nov 26

Philips Semiconductors

PHILIPS

P-channel enhancement mode MOS transistor

BSH204

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Power management
- DC to DC converters
- General purpose switch
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

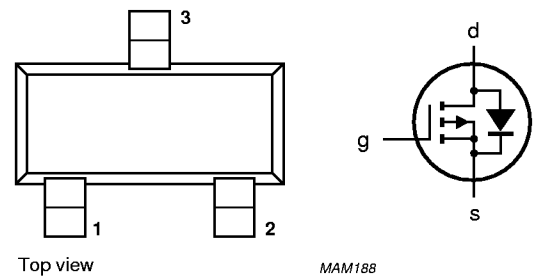


Fig.1 Simplified outline (SOT23) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.38 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–0.7	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –2.5 V; I_D = –0.4 A	–	0.75	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–0.7	A
I_{DM}	peak drain current	note 2	–	–2.8	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–0.38	A
I_{SM}	peak pulsed source current	note 2	–	–1.52	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 μA	–12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = –1 mA	–0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –9.6 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±8 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –4.5 V; I_D = –0.4 A	–	–	0.59	Ω
		V_{GS} = –2.5 V; I_D = –0.4 A	–	–	0.75	Ω
		V_{GS} = –1.8 V; I_D = –0.2 A	–	–	1	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = –6 V; V_{DD} = –6 V; I_D = –0.4 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = –6 V; I_D = –0.4 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = –6 V; I_D = –0.4 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to –6 V; V_{DD} = –6 V; I_D = –0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 0 to –6 V; V_{DD} = –6 V; I_D = –0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to –6 V; V_{DD} = –6 V; I_D = –0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = –6 to 0 V; V_{DD} = –6 V; I_D = –0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = –6 to 0 V; V_{DD} = –6 V; I_D = –0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = –6 to 0 V; V_{DD} = –6 V; I_D = –0.4 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.38 A	–	–	–1.3	V
t_{rr}	reverse recovery time	I_S = –0.5 A; di/dt = 100 A/μs	–	t.b.f.	–	ns

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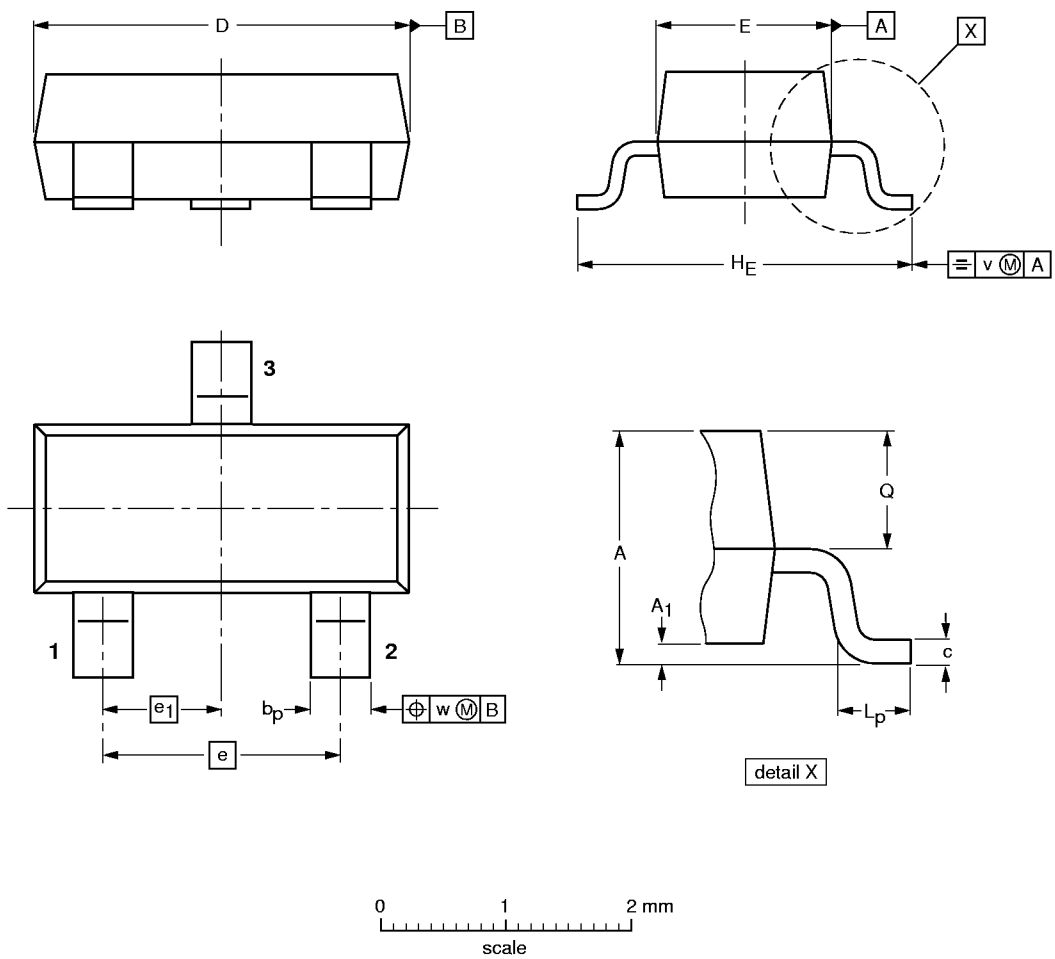
PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28