PRELIMINARY

Am27LV020

262,144 x 8-Bit CMOS Low Voltage, One Time Programmable Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **3.3 V ± 0.3 V V_{CC} read operation**
- **High performance at 3.3 V_{CC}**
  - 200 ns maximum access time
- **Low power consumption**
  - 90 µW maximum standby power
  - 25 µA maximum standby current
  - 54 mW maximum power at 5 MHz
  - 15 mA maximum current at 5 MHz
  - No data retention power
- **Industry standard packaging**
  - 32-pin PLCC
  - 32-pin Thin Small Outline Package
  - 32-pin Plastic DIP
- **Program voltage 12.75 ± .25 V**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Flashrite™ programming**
  - 10 µs typical byte-program
  - Less than 3 seconds typical chip program
- **Advanced CMOS memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am27LV020 device is a low voltage, low power, CMOS 256K x 8 One Time Programmable (OTP) non-volatile memory.

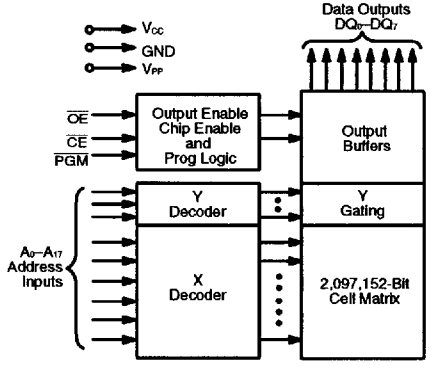
Maximum power consumption in standby mode is 90 µW. If the device is constantly accessed at 5 MHz, then maximum power consumption increases to 54 mW. These power ratings are significantly lower than typical EPROM devices. Since power consumption is proportional to voltage squared, 3.3 V devices typically consume at least 57% less power than 5.0 V devices.

The Am27LV020 typically draws 10 mA of current enabling 200 ns read operations. Typical power consumption under these conditions equals 33 mW. This "high performance", low voltage device is ideal for BIOS storage in portable computing applications and control code storage in portable digital cellular phone applications. Low voltage CMOS designs require less operating power and hence dramatically increases the usable operating life of battery powered systems.

The Am27LV020 is packaged in a 32-pin PLCC, Plastic DIP and Thin Small Outline Package (TSOP) versions. It is designed to be programmed in standard EPROM programmers.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC}+1 V.

BLOCK DIAGRAM



11507-001B

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

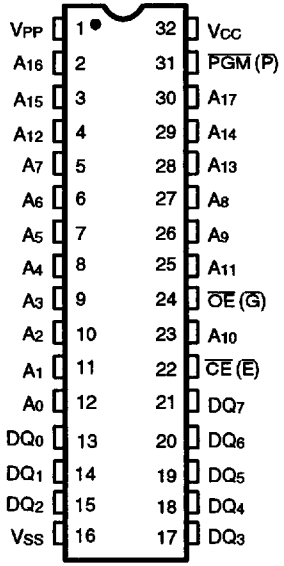
Publication #: 16357 Rev. A Amendment /0
Issue Date: July 1992

PRODUCT SELECTOR GUIDE

Family Part No.	Am27LV020		
Ordering Part No: ±0.3 V V_{CC} Tolerance	-200	-250	-300
Max Access Time (ns)	200	250	300
$\overline{CE}$ ($\overline{E}$) Access (ns)	200	250	300
$\overline{OE}$ ($\overline{G}$) Access (ns)	75	100	100

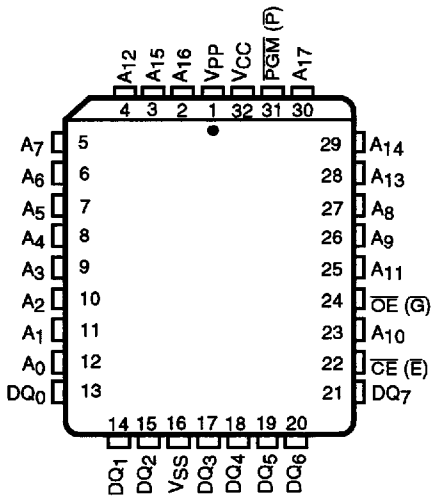
CONNECTION DIAGRAMS

DIP



14727-002B

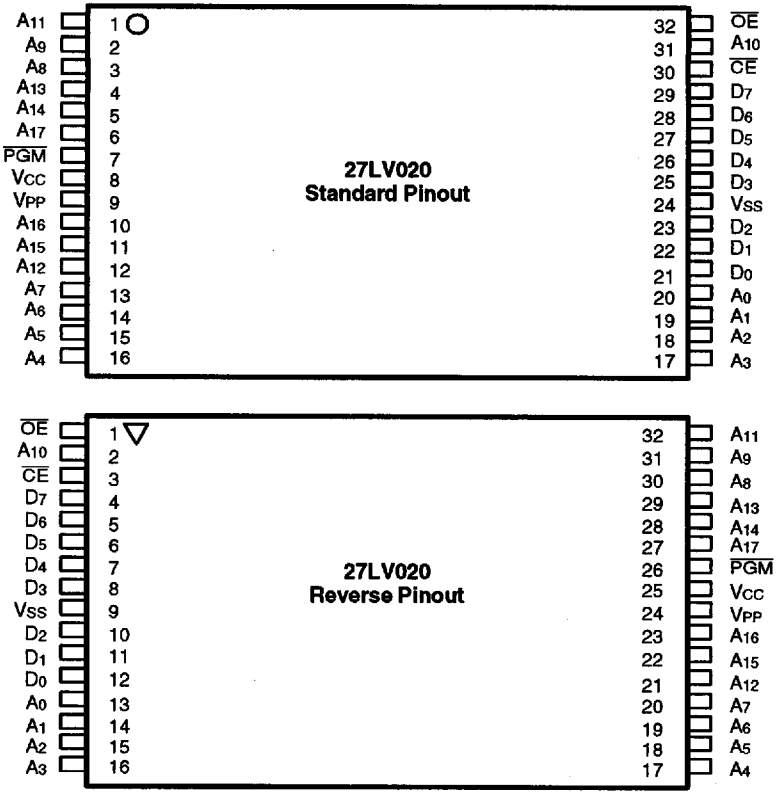
PLCC



14727-003B

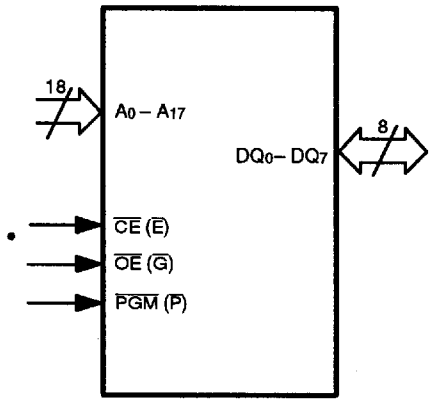
Note: Pin 1 is marked for orientation.

TSOP PACKAGES



27LV020 256K x 8 OTP in 32 Lead TSOP

LOGIC SYMBOL

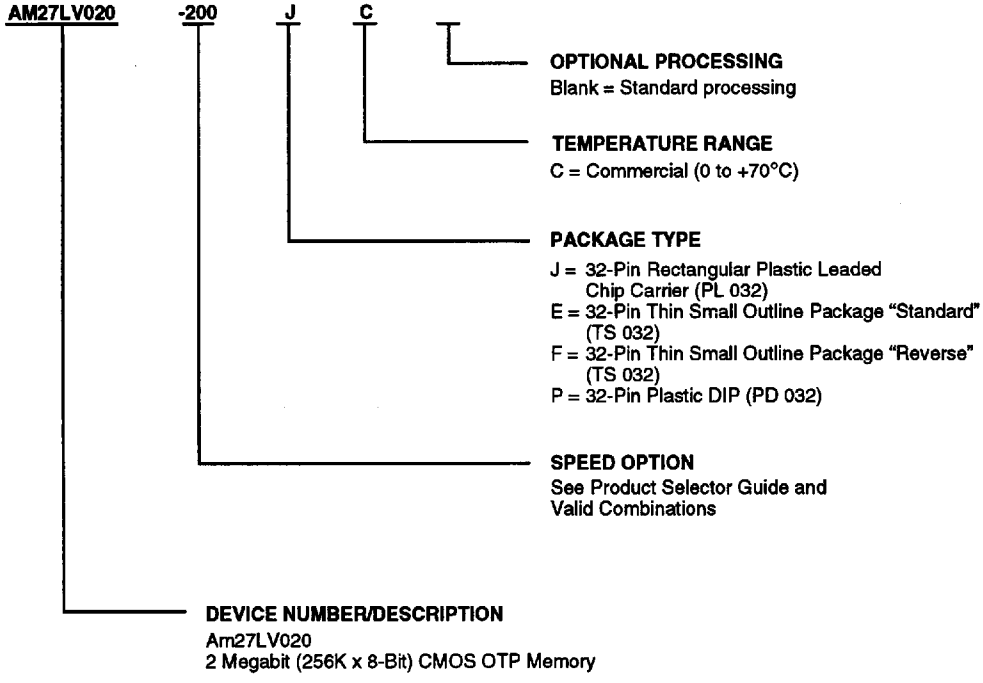


11559-004B

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of these elements:



Valid Combinations	
Am27LV020-200	JC, EC, FC, PC
Am27LV020-250	
Am27LV020-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

V_{PP}

Power supply for programming.

V_{CC}

Power supply for device operation. (Read: $V_{CC} = 3.3\,V \pm 0.3\,V$, Program: $V_{CC} = 5.0\,V \pm 10\%$)

V_{SS}

Ground

NC

No Connect-corresponding pin is not connected internally to the die.

$A_0 - A_{17}$

Address Inputs for memory locations.

$DQ_0 - DQ_7$

Data Inputs during memory program cycles. Internal latches hold data during program cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{PGM}$ ($\overline{P}$)

The Program Enable active low input controls the program function of the memory array.

BASIC PRINCIPLES

The Am27LV020 supports programming operations using a fixed 12.75 ± 0.25 V power supply.

Read Only Memory

Without high V_{PP} voltage, the Am27LV020 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Programming

These devices are programmable on standard PROM programmer equipment.

Please contact Advanced Micro Devices for PROM programmer information.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am27LV020 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 2)	CODE (01H)
	Auto-select Device Code	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 2)	CODE (2CH)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < An < V_{CC} + 2V$, (normal CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC} + 2.0$ V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written.
2. $11.5 \leq V_{ID} \leq 13.0$ V, $V_{CC} = 5.0\,V \pm 10\%$

READ ONLY MODE

V_{CC} = 3.3 V ± 0.3 V

Read

The Am27LV020 functions as a read only memory. The Am27LV020 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am27LV020 has one standby mode. The CMOS standby mode ($\overline{CE}$ input held at V_{CC} ± 0.5V), consumes less than 25 µA of current. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during programming, or program verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

The Am27LV020 can be programmed in a standard PROM programmer.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to V_{CC} + 2.0V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am27LV020 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

Table 2. Am27LV020 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	2C	0	0	1	0	1	1	0	0

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages ..... –65°C to +125°C

Ambient Temperature
with Power Applied ..... –55°C to + 125°C

Voltage with Respect To Ground. All pins
except A_9 and V_{PP} (Note 1) ..... –2.0 V to +7.0 V

V_{CC} (Note 1) ..... –2.0 V to +7.0 V

A_9 (Note 2) ..... –2.0 V to +14.0 V

V_{PP} (Note 2) ..... –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ..... 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

2. *During programming operations only. Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*

3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C) ..... 0°C to +70°C

V_{CC} Supply Voltages

V_{CC} for Am27LV020 ..... +3.0 V to +3.6 V

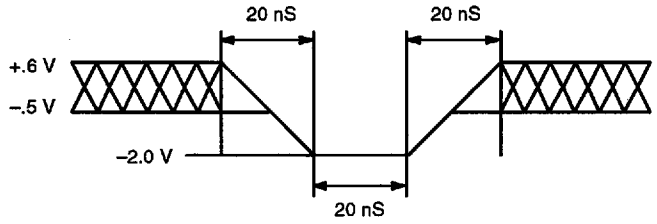
V_{PP} Supply Voltages

Program and Verify ..... +12.5 V to +13 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

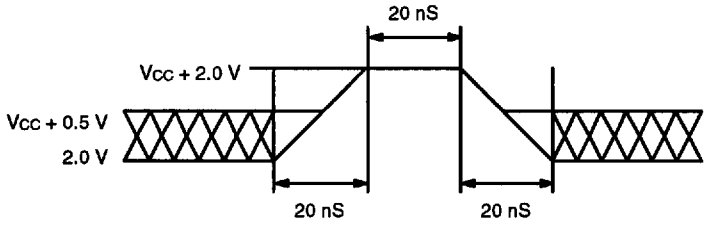
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



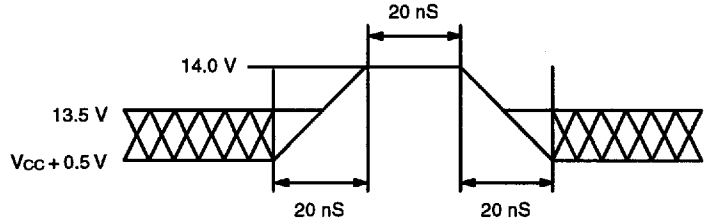
11561-009B

Maximum Positive Input Overshoot



11561-010A

Maximum V_{PP} Overshoot



11561-011A

DC CHARACTERISTICS-CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or V_{SS}		+1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{OUT} = V_{CC}$ or V_{SS}		+1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{CC} \pm 0.3$ V		25	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ I_{OUT} = 0 mA, at 5 MHz		15	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$		+1.0	µA
V_{IL}	Input Low Voltage		–0.5	0.6	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA $V_{CC} = V_{CC}$ Min.		0.3	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min.	V_{CC} –0.3		V
V_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	$A_9 = V_{ID}$ Max. $V_{CC} = V_{CC}$ Max.		35	µA
V_{PPL}	V_{PP} during Read-Only Operations		0.0	V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		12.5	13.0	V

Notes:

1. **Caution:** the Am27LV020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz.

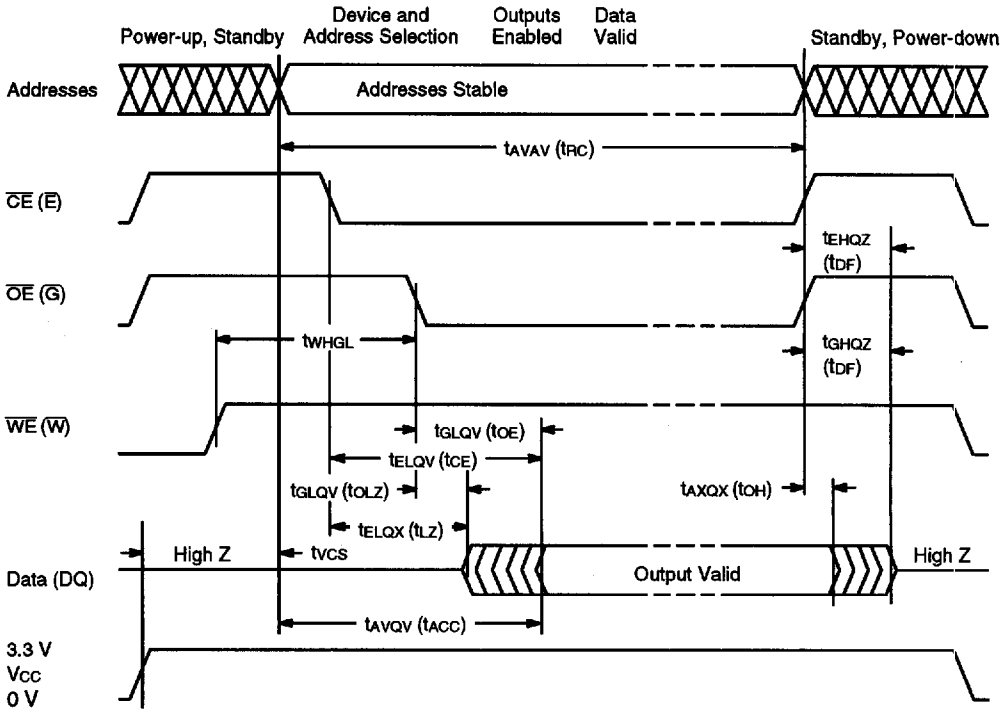
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Note 1)

Parameter Symbols				Am27LV020			
JEDEC	Standard	Parameter Description		-200	-250	-300	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	Min. Max.	200	250	300	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	200	250	300	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	200	250	300	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	75	100	100	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	Min. Max.	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	Min. Max.	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	Min. Max.	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	Min. Max.	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min. Max.	0	0	0	ns
t_{VCS}		V_{CC} Set-up Time to Valid Read	Min. Max.	50	50	50	µs

Notes:

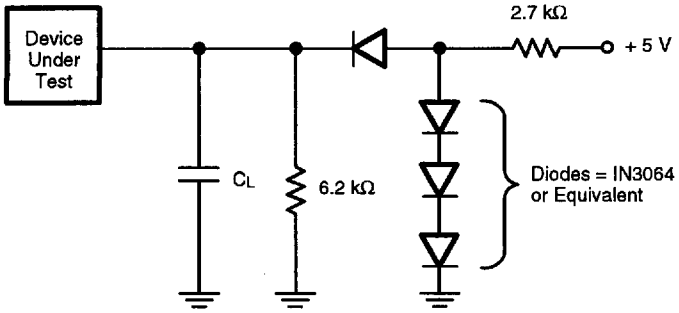
1. Output Load: 1 TTL gate and $C_L = 100$ pF, Input Rise and Fall Times: ≤ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.6 V and 2 V
   Outputs: 1.5 V
2. t_{VCS} is guaranteed by design not tested.



11561-013C

AC Waveforms for Read Operations

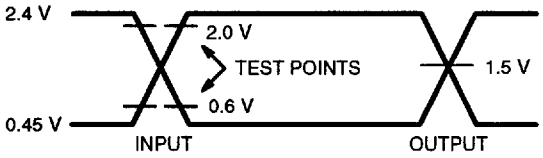
SWITCHING TEST CIRCUIT



11561-012A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

16357A-002B

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip Programming Time		4 (Note 1)	48	S	Excludes system-level overhead

Note:

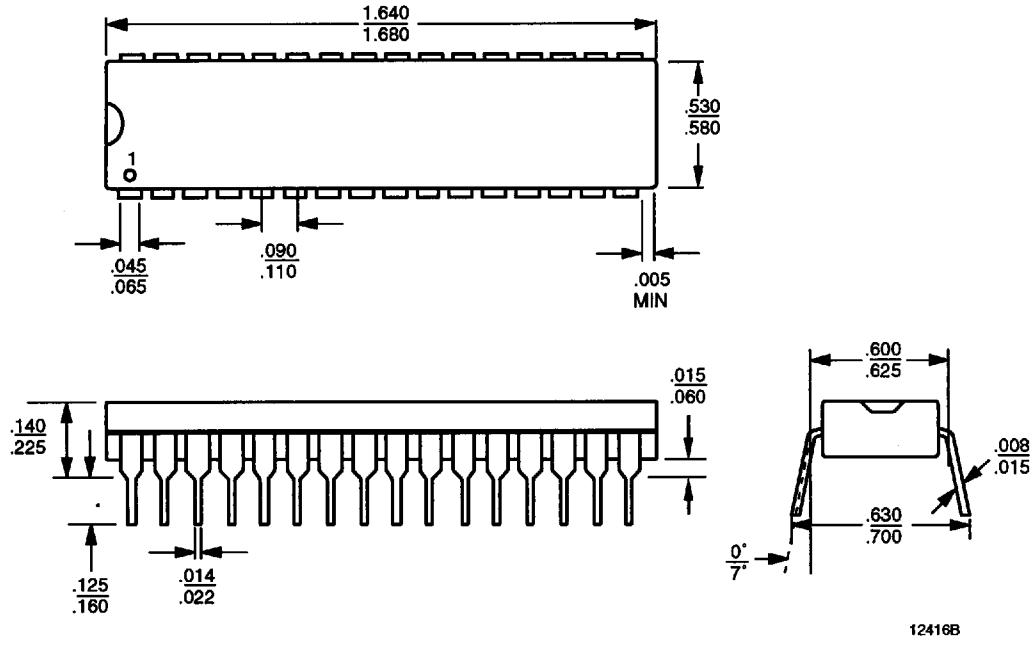
1. 25°C, 12.75 V V_{PP}.

LATCHUP CHARACTERISTICS

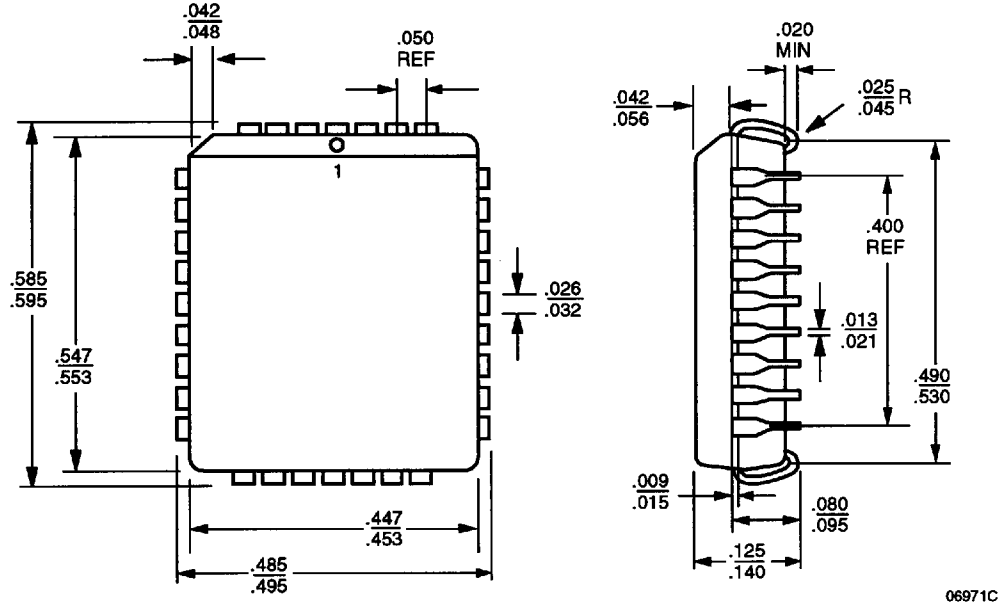
	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

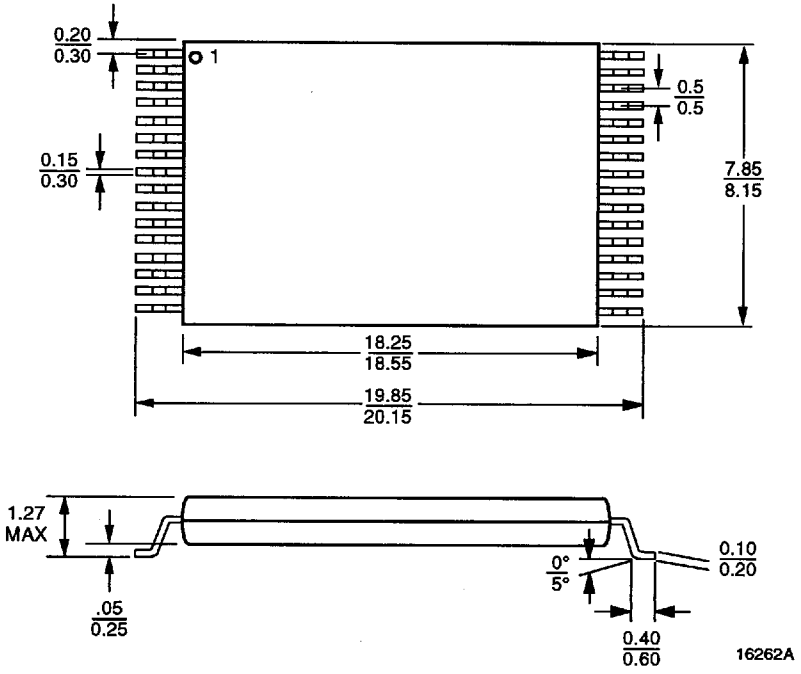
PHYSICAL DIMENSIONS*

PD 032



PL 032



*For reference only. All dimensions are measured in inches, unless otherwise noted. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS
TS 032