A66210/A66211

PROGRAMMABLE ARRAY CONTROLLER (PAC)

PRELIMINARY DATA SHEET - REVISION 2, SEPTEMBER, 1990

FEATURES:

- Full address generation capability for radix-2, radix-4, and mixed radix-2/radix-4 FFTs of up to 64K complex or 128K real points.
- Simultaneously generates up to five 16 bit addresses to both I/O buffer and data processing memories to permit full overlapping and synchronization of I/O transfers with data processing.
- Overlap/discard address generation for supporting real-time frequency domain FIR filtering.
- 32 word instruction store for holding DSP program.
- 144 and 180 pin PGA packages.
- 2-3W typical power dissipation.

APPLICATIONS:

- Radar
- Sonar
- EW/ECM
- Digital Radio
- Test Instruments
- Medical Instruments
- Spectrum Analyzers
- Transmultiplexing
- Image Processing
- Image Compression
- Image Reconstruction
- Spread Spectrum Communications

RELATED PRODUCTS:

Digital Array Signal Processor (DASP):
A66110/A66111

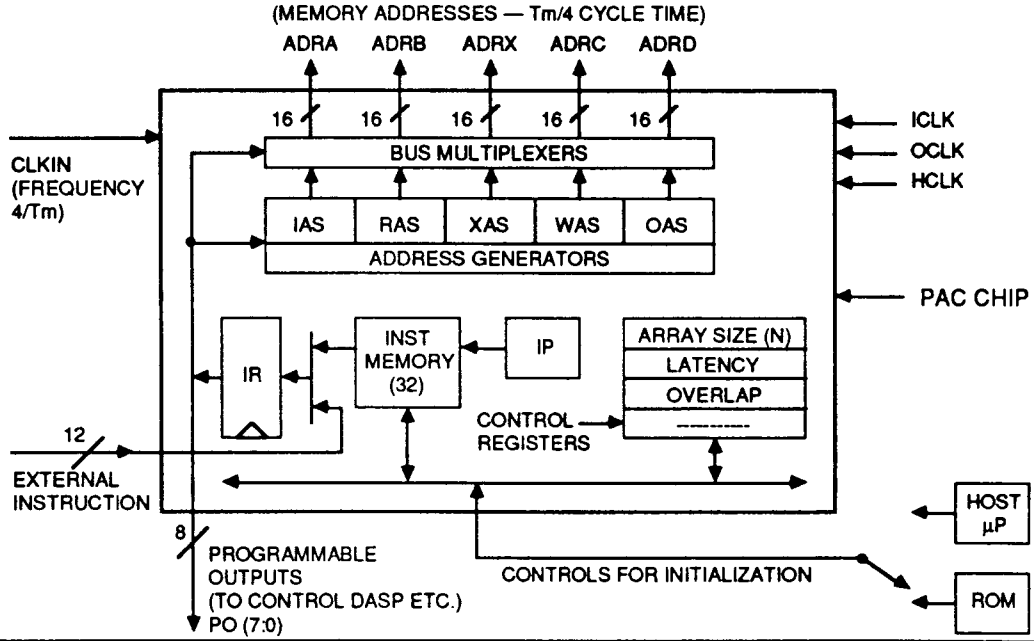
GENERAL DESCRIPTION:

The DASP/PAC chip set is the first chip set in the A66XXX family of array processing devices. It is specifically designed to fulfill the numerical processing, memory address generation, program sequencing and storage requirements of very high performance, real time DSP systems, especially those involving the computation of the Fast Fourier Transform (FFT). The PAC is used to generate memory addresses in such a DSP system and readily supports the overlapping of complex input/output data transfers with data processing.

The PAC also contains an instruction memory for holding the user's DSP program, and can either be hosted from a control processor or run in a stand-alone configuration.

Commercial temperature grade parts are available in 25 and 40 MHz speeds; military temperature range parts are available in 25 and 35 MHz speeds, with 25 MHz parts also available qualified to MIL-STD-883 levels. The A66210 is available in a 180 PGA, and the A66211 is available in a 144 PGA; the two versions are functionally identical.

BLOCK DIAGRAM



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FUNCTIONAL OVERVIEW

The Programmable Array Controller (PAC) is designed to be used with Array Microsystems' Digital Array Signal Processor (DASP) and off-the-shelf static RAMs to implement very high performance array processing systems for DSP applications. In such systems, the PAC typically satisfies all memory address generation and program storage requirements while the DASP performs all data processing. The DASP/PAC chip set can be used in a variety of system architectures which allow system throughput requirements to be traded-off against hardware constraints. A detailed functional description of both the PAC and these DASP/PAC-based system architectures appears in the **PAC User's Guide**.

Memory Address Sequences and Control

As shown in the block diagram on page 1, the core of the PAC consists of five address generators which are shown as IAS, OAS, RAS, WAS and XAS. IAS and OAS generate address sequences for data input and output, respectively, while RAS and WAS generate read and write addresses, respectively, to data processing memories. The XAS sequencer normally addresses an auxiliary or coefficient data memory. These address generators typically create all the addressing sequences required to implement various FFT-based DSP systems. Each address generator outputs a new address in response to a rising clock edge. IAS and OAS are clocked by ICLK and OCLK, respectively, while RAS, WAS, and XAS are clocked by CLKIN. ICLK, OCLK, and CLKIN can be completely asynchronous with respect to one another. As shown in the block diagram, the 16 bit outputs of these five address generators are routed through multiplexing logic to five external address buses labeled ADRA, ADRB, ADRC, ADRD and ADRX; memory write enable strobes are also routed to four control pins labeled AWE', BWE', CWE', and DWE'. These address buses and write enables can be used to control up to five distinct memories simultaneously.

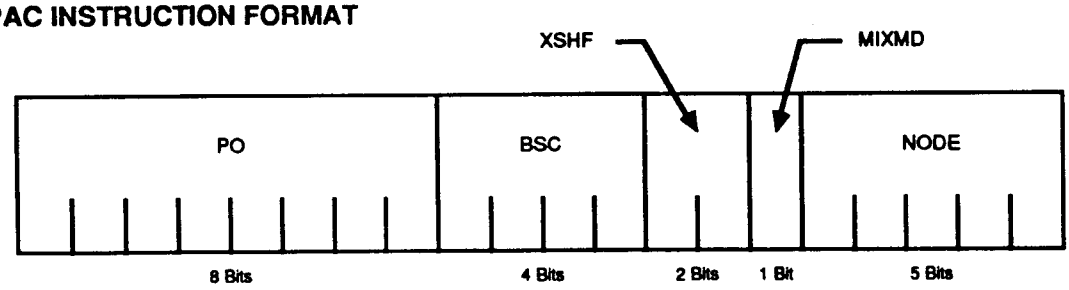
Typically, each PAC address bus addresses a memory containing complex (i.e. real and imaginary) data. The data port of each memory, in turn, is connected to one of the three I/O ports of the DASP, to an input data collection buffer, or to an output data buffer. When the PAC is used with the DASP running in the dual I/O mode, all of these memories can be single-ported, and only a minimum of glue logic is need to complete a system.

Normally, a DASP/PAC chip set is used in conjunction with a ping-pong memory architecture in which arrays of data are passed through the DASP between pairs of memories, with one memory supplying data to the DASP while the other receives output data from the DASP. In such a ping-pong memory system, it is necessary to be able to change the destinations of the PAC address generator outputs from one data pass to the next. This function is accomplished by the bus multiplexers shown in the block diagram, and these multiplexers are, in turn, controlled by the BSC ("bus switch code") field in the PAC instruction, which will be discussed later. Note that the output of the XAS generator is always routed to the XADR address bus.

The address sequences created by the five PAC address generators are selected by the 5 bit NODE field in the PAC instruction. The various address sequences supported by the PAC are as follows:

Mnemonic	Sequence Description
FFT0 to FFT15	Data and coefficient address sequences associated with an in-place, decimation-in-frequency (DIF) FFT algorithms. The sequences span from column 0 to column 15 of a radix-2, radix-4, or mixed radix-2/radix-4 FFT flowgraph, covering up to a 64K point complex data array. The radix base for the algorithm is defined by the PAC instruction and the RCONFIG control register. Digit reversed addresses can be optionally produced in the final FFT column.
SEQ	Sequential: A normal sequential binary sequence for the purpose of input, output, windowing etc.
SSEQ	Symmetric Sequential: A normal sequential binary sequence which is symmetrical in the middle to handle symmetric windows, etc.
FFT2N	Supports DASP's FFT2N function; generates addressing sequences to handle the data recombination associated with the implementation of a 2N real-point FFT using an N complex-point FFT.
FFTNN	Supports DASP's FFTNN function; generates addressing sequences to handle the data recombination associated with the implementation of two separate real N-point FFTs via a single N complex-point FFT.
FTRS	Filter Sequence: The overlap/save sequence to allow overlapping of input data frames during frequency domain FIR filtering of a continuous input sequence.

FIGURE 1 — PAC INSTRUCTION FORMAT



Control Registers

The PAC also contains several user-loadable control registers which add to the versatility of the PAC (see block diagram). These registers supply various parameters to the PAC describing the user's system configuration and are briefly described below:

Mnemonic	Register Description
N(15:0)	Specifies the size of the data array to be processed. It can range from 4 points to 64K complex points.
PLAT(3:0)	Processor latency; specifies the latency of the DASP in terms of machine cycles (user should always set to 4).
MLAT(5:0)	Memory latency; specifies the latencies through the external memories associated with the DASP. A latency in a memory path will be introduced if address and/or data of a memory are being latched for high performance applications. The PAC compensates for these latencies when generating the addresses and write strobes for corresponding memories.
K(15:0)	Specifies the size of the overlap in successive input data frames. The overlapping is normally used for frequency domain filtering. It can range from 0 to 50% of the array size.
RCONFIG(15:0)	Contains system configuration information such as cascaded system, single memory system, radix type.
PRGSZ(5:0)	Program size; length of user's PAC program.
PSLEN(7:0)	Pause length; used to enforce delays between data passes.
M(4:0)	Base-2 or base-4 logarithm of N (i.e array length) as required.
M4(4:0)	Holds value of (M-1)/2 for use during mixed-radix FFTs.
LFND(5:0)	Left neighbor node field; contains the value of the NODE instruction field of the current PAC's left neighbor in full column-pipelined cascaded systems.
RFND(5:0)	Right neighbor node field; contains the value of the NODE instruction field of the current PAC's right neighbor in full column-pipelined cascaded systems.
TCNT(15:0)	Test count; a diagnostic register no intended for general usage which should normally be ignored.
STAD(15:0)	Starting address; specifies the page offset to be applied to addresses output on the ADRA, ADRB, ADRC, and ADRD buses.

Instruction Memory

The PAC contains a 32 word by 20-bit instruction RAM whic holds the user's DSP program. The PAC instruction layo appears in Figure 1 above. The concept of a PAC instructic is somewhat different from that of a typical microprocessc In microprocessors, an instruction typically manipulates ju

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a few data values. A PAC instruction controls a full pass of an N-point data array through the DASP, where N is defined by the similarly named PAC control register. During the pass, the DASP function programmed into the PO(7:0) field of the PAC instruction will be applied to successive sets of data values from the N-point data array. DASP functions and data sets are defined in the **DASP Data Sheet** and **DASP User's Guide**. Since one PAC instruction controls a complete pass of the data array through the DASP, a 1024 point FFT using a radix-4 algorithm, for example, basically takes only 5 instructions since the corresponding FFT flowgraph consists of five FFT columns. If additional passes such as windowing or magnitude-squared are desired, one instruction will be needed for each such pass. The on-chip 32 word program memory suffices for most applications; however, external program memory may also be used if necessary (see the **PAC User's Guide** for further details).

The various fields of the PAC instruction as displayed in Figure 1 are briefly described below:

PO(7:0) Programmable outputs. The user-defined 8 bit value in this field is directly fed to the PO pins of PAC; normally, 6 of these bits are used to hold the 6 bit DASP function code.

BSC(3:0) Bus switch code. This field controls the bus multiplexers of the PAC to assign the appropriate address generators to the ADRA, ADRB, ADRC and ADRD address buses. The BSC field is also output directly to the BSC pins where it can be accessed for the purpose of controlling the data buffers in the user's system. The legal BSC encodings are shown in Table 1.

XSHF(1:0) This field defines the number of bit positions to left-shift the XAS address generator output prior to outputting it on the XADR bus. This feature permits coefficient table decimation which is useful for sharing coefficient memories between different sized FFTs.

MIXMD This bit indicates if a mixed-radix FFT (radix-4/radix-2) is being performed; it should be set in the PAC instructions comprising the radix-4 passes. By using the mixed-radix mode, it is possible to transform a data array in which the number of points is an odd power of 2 at almost the speed of an even power of 2 (i.e. radix-4) array.

NODE(4:0) This field selects the addressing sequences produced by the five address generators of the PAC during the current data pass. These sequences were briefly described earlier. The legal encodings of this field are listed in Table 2.

Host Interface and PAC Initialization

All the control registers and the instruction memory of the PAC are memory mapped for ease of initialization; this memory map appears in Figure 2. The PAC can be initialized by a host processor or it can autoboot itself from an external ROM. The initialization option is determined by the AUTO-BOOT pin. Control register and instruction memory data are transferred to the PAC via the ADRA and ADRB buses; for this purpose, ADRA serves as an input address bus, while ADRB serves as a data bus. After initialization, processing is started by activating the GO pin, after which the PAC manages the complete system. The SYNC pins on both the DASP and the PAC should also be activated at this time to synchronize PAC address generation with DASP data processing. The PAC executes the DSP algorithm by either continuously looping through the PAC program or executing it one instruction at a time in single-step fashion, as determined by the ASTRT bit in the RCONFIG control register.

Clocks

The PAC is operated by using a system clock (CLKIN) at a frequency of 4/Tm, where Tm is the machine cycle time of the DASP (100 nsec minimum). However, additional clock inputs ICLK, OCLK and HCLK are also provided. ICLK and OCLK manage input data collection and output data dumping, respectively, at the desired rate. HCLK is used to clock data and addresses into the PAC during PAC initialization. CLKIN, ICLK, OCLK, and HCLK can all be asynchronous with respect to one another.

TABLE 1 - PAC INSTRUCTION BSC FIELD ENCODINGS

FOR RECURSIVE OPERATION:

BSC	ADRA	ADRB	ADRC	ADRD
0	IAS	***	WAS	OAS
1	IAS	WAS	RAS	OAS
2	OAS	IAS	RAS	WAS
3	RAS	IAS	OAS	WAS
4	WAS	IAS	OAS	RAS
5	***	OAS	WAS	IAS
6	WAS	OAS	RAS	IAS
7	OAS	IAS	WAS	***
8	OAS	RAS	IAS	WAS
9	OAS	WAS	IAS	RAS
A	OAS	WAS	RAS	IAS
C	WAS	OAS	IAS	RAS

*** RAS if MUXRW = 0
RAS/WAS if MUXRW = 1

FOR CASCADED OPERATION:

BSC	ADRA	ADRB	ADRC	ADRD
0	IAS	RAS	WAS	OAS
1	RAS	IAS	WAS(1)	OAS
2	T.S.	WAS(2)	RAS (3)	T.S.
3	T.S.	RAS(4)	OAS	WAS

Notes for cascaded operation:

1. The write address generator is used to generate the read address sequence for the PAC's right neighbor.
2. The write address generator is used to generate the write address sequence for the PAC's left neighbor.
3. The read address generator is used to generate the read address sequence for the PAC's right neighbor.
4. The read address generator is used to generate the write address sequence for the PAC's left neighbor.

T.S. - Tri-state

TABLE 2 - PAC INSTRUCTION NODE FIELD ENCODINGS

Hex Code	Mnemonic	Description
00	FFT0	FFT Column 0
01	FFT1	FFT Column 1
02	FFT2	FFT Column 2
03	FFT3	FFT Column 3
04	FFT4	FFT Column 4
05	FFT5	FFT Column 5
06	FFT6	FFT Column 6
07	FFT7	FFT Column 7
08	FFT8	FFT Column 8
09	FFT9	FFT Column 9
0A	FFT10	FFT Column 10
0B	FFT11	FFT Column 11
0C	FFT12	FFT Column 12
0D	FFT13	FFT Column 13
0E	FFT14	FFT Column 14
0F	FFT15	FFT Column 15
10	SEQ	Sequential
11	SSEQ	Symmetric Sequential
12	FFT2N	Double-Length Real FFT
13	FFTNN	Dual Real FFT
14	FTRS	Filter Sequence
15-1E	Reserved	
1F	EOPM	End of Process Marker

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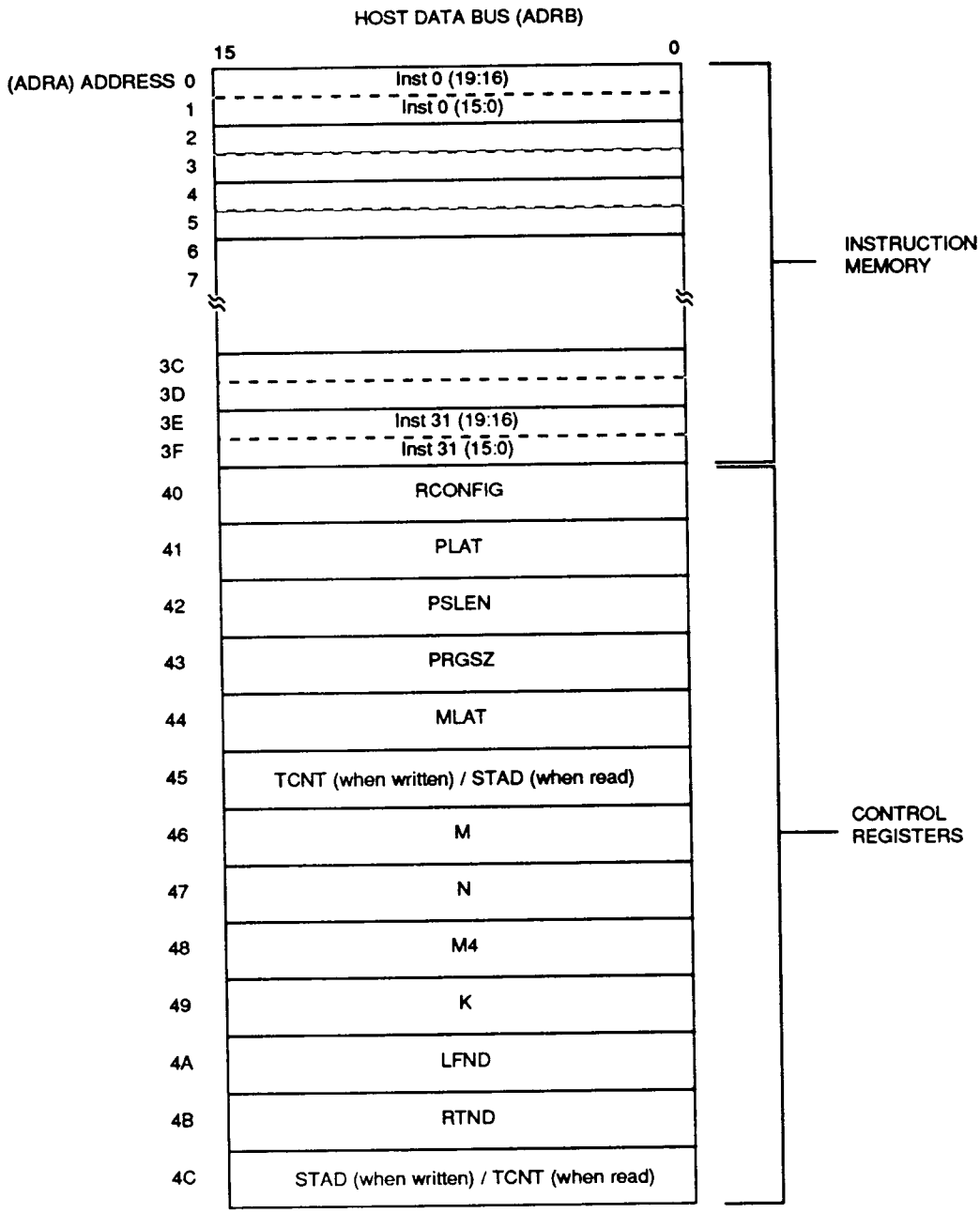
FIGURE 2 - MEMORY MAP OF PAC CONTROL AND INSTRUCTION REGISTERS



ABSOLUTE MAXIMUM RATINGS (BEYOND WHICH DAMAGE MAY OCCUR)

Positive Supply Voltage .....-0.5V to 7.0V
DC Input Voltage .....-0.5V to 7.0V
DC Output Voltage (Applied in Hi-Z State) ..-0.5V to 7.0V
Low Level Output Current .....20 mA
Operating Case Temperature .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C

Note:
Operation at any Absolute Maximum Rating is not implied. Ratings are provided for guidance purposes only and are not tested. Exposure to absolute maximum rating conditions over extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

(See page 14 for switching waveforms; test levels are defined on page 10.)

MILITARY TEMPERATURE RANGE

Test Conditions:

T_C=-55°C to +125°C, V_{CC} = 5V ± 5%, output load capacitance = 50 pF unless otherwise specified (T_C = case temperature).

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	A66210B A66211B MIN	TYP	MAX	A66210A A66211A MIN	TYP	MAX	UNITS
			ADVANCED INFORMATION(1)			ADVANCED INFORMATION(1)			
Input High Voltage(V_{IH})		I	2.5		5.25	2.5		5.25	V
Input Low Voltage(V_{IL})		I			0.6			0.6	V
Output High Voltage(V_{OH})	Vcc Min	I	3.7			3.7			V
Output Low Voltage(V_{OL})	Vcc Min	I			0.6			0.6	V
Input High Leakage Current	Vcc Max	I			120			120	µA
Input Low Leakage Current	Vcc Max	I			-40			-40	µA
High Level Output Current(I_{OH})		I			-4.0			-4.0	mA
Low Level Output Current(I_{OL})		I			4.0			4.0	mA
Hi-Z Output Leakage Current (I_{OZ})	Vcc Max, .6V <V_{OUT}<2.7V	I	-20		20	-20		20	µA
Operating Supply Current(I_{CC})	Vcc, f_a Max	I			375			475	mA
CAPACITANCE									
Input Capacitance(C_{IN})	V_{CC} = 5V, T_C=25°C	V		10			10		pF
Output Capacitance(C_{OUT})	V_{CC} = 5V, T_C=25°C	V		10			10		pF

NOTES:

1. Parameter values are subject to change based on final device characterization.

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MILITARY TEMPERATURE RANGE

Test Conditions:

T_C = -55°C to +125°C, V_{CC} = 5V ± 5%, output load capacitance = 50 pF unless otherwise specified (T_C = case temperature).

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	AP66210B AP66211B MIN	TYP	MAX	A66210A A66211A MIN	TYP	MAX	UNITS
PROCESSOR CLOCKS (2)			ADVANCED INFORMATION(1)			ADVANCED INFORMATION(1)			
CLKIN Frequency (f_{ci})		I	3		25	3		35	MHz
CLKIN Period (t_{ci})		I	40			28.5			nS
CLKIN Rise and Fall Time (t_{ri})		IV			10			10	nS
CLKIN Low Level Pulse Width (t_{pwl})		I	15			11			nS
CLKIN High Level Pulse Width (t_{pwh})		I	15			12			nS
CLKIN to CLKOUT Delay (t_{cd})		V		7			7		nS
CLKIN to MCLKOUT Delay (t_{md})		V		7			7		nS
CLKOUT Period (t_{co})			40			28.5			nS
MCLKOUT Period (t_m)			160			114			nS
INPUT / OUTPUT CLOCKS (3)									
ICLK / OCLK Frequency (f_{ic},f_{oc})		I			25			35	MHz
ICLK / OCLK Period (t_{ic},t_{oc})		I	40			28.5			nS
ICLK / OCLK Rise and Fall Time (t_{ri})		IV			10			10	nS
ICLK / OCLK Hi or Low Pulse Width (t_{pw})		IV	12			12			nS
ADDRESS, WRITE ENABLE, AND CHIP SELECT OUTPUT DELAYS									
CLKIN to Any Address (t_{ad}) (2)		I	10		18	10		18	nS
ICLK / OCLK to Any Address (t_{ad}) (3)		I	11		15	11		15	nS
CLKIN / ICLK / OCLK to Any Write Enable or Chip Select (t_{wd}) (4)		I	11		14	11		14	nS
OE' to Any Address, PO(7:0), or IP(4:0) Either Active or Inactive (t_{zd}) (2)		I							nS
INPUT / OUTPUT STATUS DELAYS (3)									
ICLK / OCLK to IBUSY, OBUSY, IFULL, or OEMPTY Output (t_{sd})		I	11		18	11		18	nS
DATA PASS AND PROCESS SYNCHRONIZATION (2)									
CLKIN to INITPR,BOP,EOP,EOPR (t_{pd})		I	15		30	15		30	nS
SYNC/NFTS Setup to CLKIN (t_{ssu})		I	13			13			nS
SYNC/NFTS Hold Time from CLKIN (t_{sh})		I	0			0			nS

NOTES:
1. Parameter values are subject to change based on final device characterization.
2. See Figure 3.
3. See Figure 4.
4. See either Figure 3 or Figure 4.

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MILITARY TEMPERATURE RANGE

Test Conditions:

T_c = -55°C to +125°C, V_{CC} = 5V ± 5%, output load capacitance = 50 pF unless otherwise specified (T_c = case temperature).

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	A66210B A66211B MIN	TYP	MAX	A66210A A66211A MIN	TYP	MAX	UNITS
INSTRUCTION FIELD AND INSTRUCTION POINTER OUTPUTS (2)			ADVANCED INFORMATION(1)			ADVANCED INFORMATION(1)			
CLKIN to PO(7:0),BSC(3:0), IP(4:0) (t_{pd})		I		15	24		15	24	nS
EXTERNAL INSTRUCTION INPUT (2)									
PO(7:0), IP(4:0) Setup to CLKIN (t_{isu})		I	8			8			nS
PO(7:0), IP(4:0) Hold from CLKIN (t_{ih})		I	0			0			nS
HOST INTERFACE (3)									
HCLK Frequency (f_{hc})		I			10			10	MHz
HCLK Period (t_{hc})		I	100			100			nS
HCLK Rise and Fall Time (t_{rf})		IV			10			10	nS
HCLK High or Low Pulse Width (t_{pw})		I	15			15			nS
ADRA (Address) Setup to HCLK (t_{asu}) (4)		I	15			15			nS
ADRA Hold Time after HCLK (t_{ah})		I	0			0			nS
ADRB (Data) Setup to HCLK (t_{dsu})		I	18			18			nS
ADRB Hold Time after next HCLK (t_{dh})		I	0			0			nS
WR', CS' Setup to HCLK (t_{wsu})		I	25			25			nS
WR', CS' Hold Time after HCLK (t_{wh})		I	0			0			nS
ADRA (Address) to ADRB (Data) (t_{ra}) (Read Access Time)		I			50			50	nS
HCLK to CS' (AUTOBOOT=1) (t_{cd})		I			25			25	nS
HCLK to BOOTDONE (t_{bd})		I			30			30	nS
BOOTDONE output pulse width (t_{bpw})		I	$2*t_{hc}$			$2*t_{hc}$			nS
GO Setup to CLKIN (t_{gsu})		I	9			9			nS
GO input pulse width (t_{gpw})		I	NOTE 5			NOTE 5			nS
RST' input pulse width (t_{rpw})		I	NOTE 6			NOTE 6			nS
CS' to ADRA/ADRB Active or Inact (t_{zd})		I			25			25	nS
QUAD MODE CONTROL OUTPUTS(2)									
CLKIN to QAS0,QAS1,QAS2,QAS3 (t_{qd})		IV			25			25	nS

NOTES:

1. Parameter values are subject to change based on final device characterization.
2. See Figure 3.
3. See Figure 5.
4. Setup is relative to HCLK falling edge
5. In AUTOBOOT mode, the first GO signal following initialization must be the largest of: $2*t_{hc}$, t_m. In HOSTBOOT mode and f all other GO pulses after initialization, the minimum GO pulse width is: t_m.
6. Largest of: t_{ic}, t_{oc}, t_{hc}, t_m

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TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are performed after device case reaches operating temperature.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_C = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

COMMERCIAL TEMPERATURE RANGE

Test Conditions:

T_C = 0°C to +70°C, V_{CC} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_C = case temperature).

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	A66210B A66211B MIN	TYP	MAX	A66210A A66211A MIN	TYP	MAX	UNITS
Input High Voltage(V_{IH})	V_{cc} Max	I	2.4		Vcc	2.4		Vcc	V
Input Low Voltage(V_{IL})	V_{cc} Max	I			0.6			0.6	V
Output High Voltage(V_{OH})	I_{OH}=-4.0mA	I	3.75			3.75			V
Output Low Voltage(V_{OL})	I_{OL}=4.0mA	I			0.6			0.6	V
Input High Leakage Current (I_{LH})	V_{cc} Max	I			120			120	µA
Input Low Leakage Current (I_{LL})	V_{cc} Max	I			-40			-40	µA
Hi-Z Output Leakage Current (I_{OZ})	Vcc Max, .6V <V_{OUT}<2.7V	I	-20		20	-20		20	µA
Operating Supply Current(I_{CC})	Vcc Max, f_{ci} Max	I			375			650	mA
CAPACITANCE									
Input Capacitance(C_{IN})	V_{CC} = 5V,T_C=25°C	V		10			10		pF
Output Capacitance(C_{OUT})	V_{CC} = 5V,T_C=25°C	V		10			10		pF

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Test Conditions:

T_c = 0°C to +70°C, V_{cc} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature) MUXRW=low, NFT=low.

AC ELECTRICAL PARAMETERS[1]	TEST CONDITIONS	TEST LEVEL	A66210B A66211B MIN	TYP	MAX	A66210A A66211A MIN	TYP	MAX	UNITS
PROCESSOR CLOCKS									
CLKIN Frequency (f_{ci})		I[3]	3		25	3		40	MHz
CLKIN Period (t_{ci})		I	40			25			nS
CLKIN Rise and Fall Time (t_{rf})		IV			10			10	nS
CLKIN Low Level Pulse Width (t_{pwl})		I	16			12			nS
CLKIN High Level Pulse Width (t_{pwh})		I	16			10			nS
CLKIN to CLKOUT Delay (t_{cd})		I	3		20	3		14	nS
CLKIN to MCLKOUT Delay (t_{md})		I	3		20	3		14	nS
CLKOUT Period (t_{co})		IV	40			25			nS
MCLKOUT Period (t_m)		IV	160			100			nS
INPUT / OUTPUT CLOCKS									
ICLK / OCLK Frequency (f_{ic},f_{oc})		I	3		25			40	MHz
ICLK / OCLK Period (t_{ic},t_{oc})		I	40			25			nS
ICLK / OCLK Rise and Fall Time (t_{irf})		IV			10			10	nS
ICLK / OCLK Hi or Low Pulse Width (t_{pw})		IV	16			12			nS
ADDRESS, WRITE ENABLE, AND CHIP SELECT OUTPUT DELAYS									
CLKIN/ICLK/OCLK to ADRA/ADRB/ ADRC/ADRD (t_{ad})		I	5		26	5		19	nS
CLKIN to ADRX (t_{xd})		I	7		29	7		22	nS
CLKIN / ICLK to Any Write Enable or Chip Select (t_{wed})[2]		I	5		22	5		18	nS
OE' to Any Address, PO(7:0), or IP(4:0) Either Active or Inactive (t_{ozd})		IV			40			30	nS
INPUT / OUTPUT STATUS DELAYS									
ICLK / OCLK to IBUSY, OBUSY, IFULL, or OEMPTY Output (t_{sd})		I	5		22	5		18	nS
DATA PASS AND PROCESS SYNCHRONIZATION									
CLKIN to INITPR,BOP,EOP,EOPR (t_{pd})		I	8		33	8		26	nS
SYNC Setup to CLKIN (t_{ssu})		I	20			16			nS
SYNC Hold Time from CLKIN (t_{sh})		I	0			0			nS

NOTES:

1. For all output delay times, MIN values refer to the minimum time old outputs are valid after the clock edge triggering the change before the new outputs are valid (see switching waveforms).
2. Signals include: AWE', BWE', CWE', DWE', OVAWE', OVBWE', OVACS', OVBCS'.
3. MAX is fully tested; MIN is guaranteed by design.

Test Conditions:

T_c = 0°C to +70°C, V_{cc} = 5V ± 5%, output load capacitance = 35 pF unless otherwise specified (T_c = case temperature) MUXRW=low, NFT=low.

AC ELECTRICAL PARAMETERS [6]	TEST CONDITIONS	TEST LEVEL	A66210B A66211B MIN	TYP	MAX	A66210A A66211A MIN	TYP	MAX	UNITS
INSTRUCTION FIELD AND INSTRUCTION POINTER OUTPUTS									
CLKIN to PO(7:0),BSC(3:0), IP(4:0) (t_{id})		I	8		30	8		22	nS
EXTERNAL INSTRUCTION INPUT									
PO(7:0), IP(4:0) Setup to CLKIN (t_{isu})		I	13			13			nS
PO(7:0), IP(4:0) Hold from CLKIN (t_{ih})		I	0			0			nS
HOST INTERFACE [1]									
HCLK Frequency (f_{hc})		I			6.25			10	MHz
HCLK Period (t_{hc})		I	160			100			nS
HCLK Rise and Fall Time (t_{hrf})		IV			10			10	nS
HCLK High or Low Pulse Width (t_{hpw})		IV	30			30			nS
ADRA (Address) Setup to HCLK (t_{asu})[2]	AUTOBOOT=low	I	18			17			nS
ADRA Hold Time after HCLK (t_{ah})	AUTOBOOT=low	I	0			0			nS
ADRB (Data) Setup to HCLK (t_{dsu})		I	23			22			nS
ADRB Hold Time after HCLK (t_{dh})		I	0			0			nS
CS' Setup to HCLK (t_{csu})	AUTOBOOT=low	I	50			50			nS
CS' Hold Time after HCLK (t_{ch})	AUTOBOOT=low	I	0			0			nS
WR' Setup to HCLK (t_{wsu})[2]	AUTOBOOT=low	I	20			17			nS
WR' Hold Time after HCLK (t_{wh})	AUTOBOOT=low	I	0			0			nS
ADRA (Address) to ADRB (Data) (t_{ra}) (Read Access Time)	AUTOBOOT=low	I	13		59	13		45	nS
HCLK to CS', BOOTDONE (t_{hcd})	AUTOBOOT=high	I	5		20	5		17	nS
HCLK to ADRA (Address) (t_{had})	AUTOBOOT=high	I	6		20	6		18	nS
BOOTDONE output pulse width (t_{bpw})	AUTOBOOT=high	IV	$2*t_{hc}$		NOTE 3	$2*t_{hc}$		NOTE 3	nS
GO Setup to CLKIN (t_{gsu})		I	25			22			nS
GO input pulse width (t_{gpw})		I	NOTE 4			NOTE 4			nS
RST' Setup to CLKIN (t_{rsu})		I	28			23			nS
RST' input pulse width (t_{rpw})		I	NOTE 5			NOTE 5			nS
CS' to ADRA/ADRB Active or Inact (t_{czd})	AUTOBOOT=low	IV			45			35	nS
QUAD MODE CONTROL OUTPUTS									
CLKIN to QAS0,QAS1,QAS2,QAS3 (t_{qd})		I	5		28	5		23	nS

NOTES: (See next page).

NOTES (for Page 12):

1. Unless otherwise noted: All set-up, hold and output delay times with respect to HCLK are relative to HCLK low-to-high transition.
2. With respect to HCLK high-to-low transition.
3. At a maximum, BOOTDONE will remain high until low-to-high transition on GO.
4. Min pulse width when AUTOBOOT=high is the largest of t_{hc} and t_m; min pulse width when AUTOBOOT=low is t_m.

   Futhermore, when AUTOBOOT=high, ICLK must undergo a low-to-high transition while BOOTDONE=high to ensure proper address sequencing.
5. Min pulse width is largest of t_{ic}, t_{oc}, t_{hc}, and t_m.
6. For all output delay times, MIN values refer to the minimum time old outputs are valid after the clock edge triggering the change before the new outputs are valid (see switching waveforms).

FIGURE 3 - SWITCHING WAVEFORMS

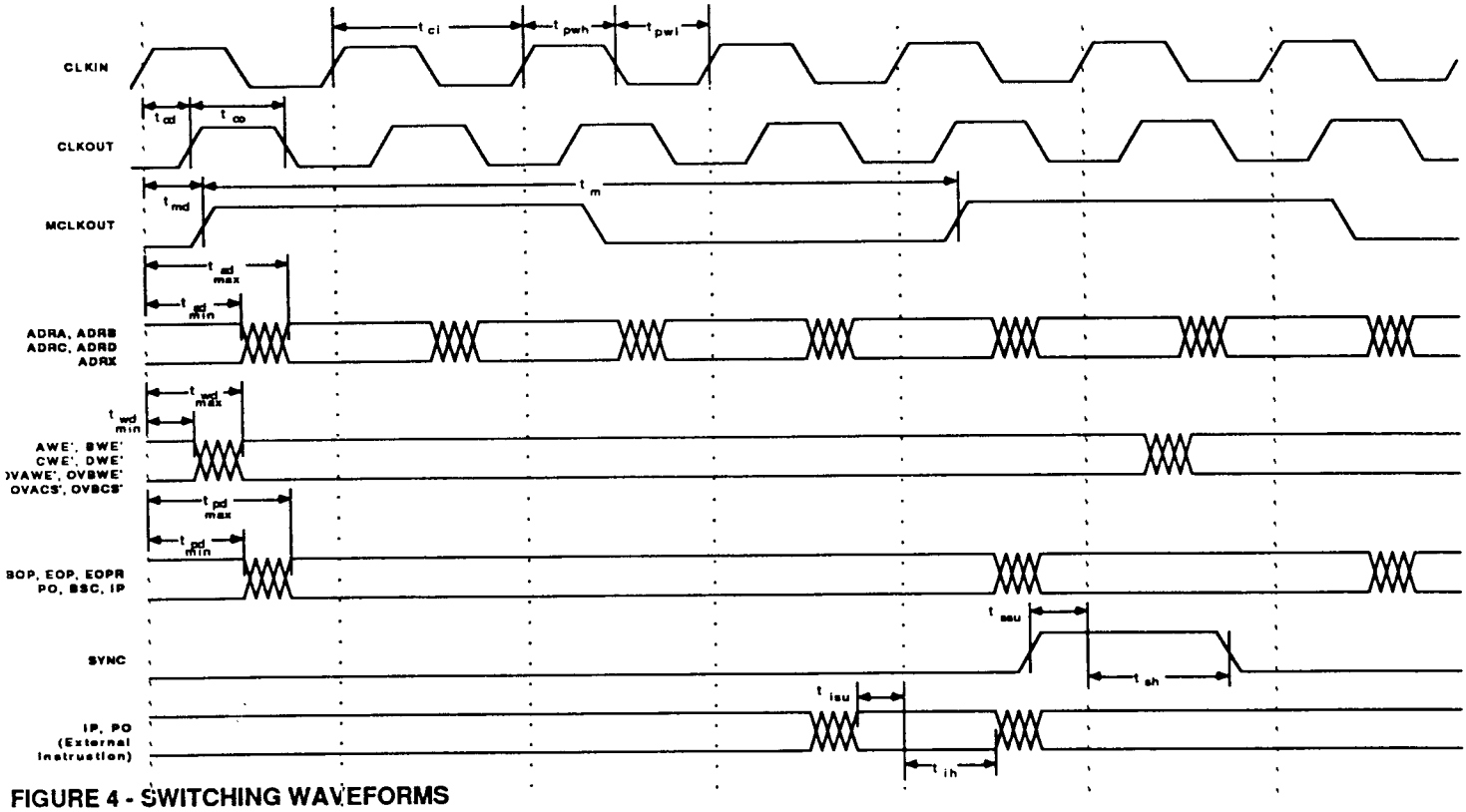


FIGURE 4 - SWITCHING WAVEFORMS

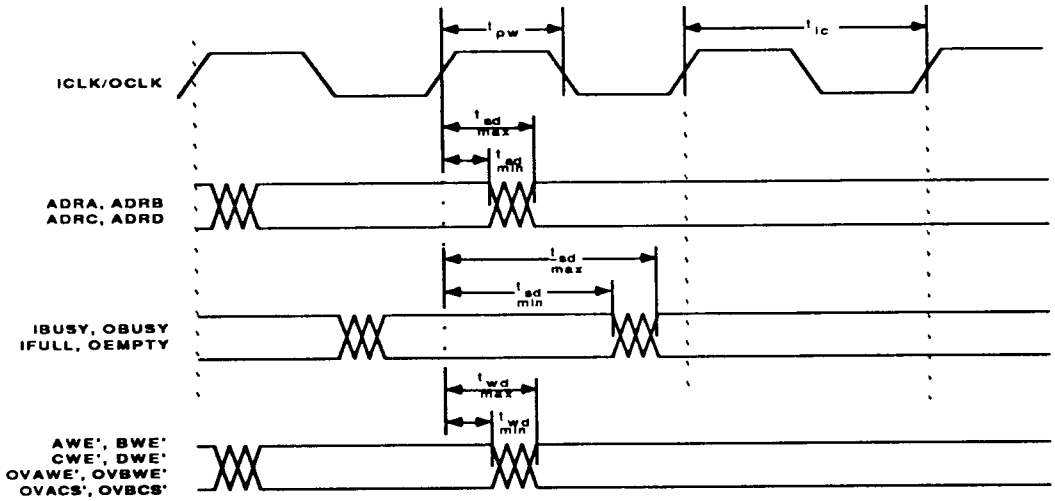
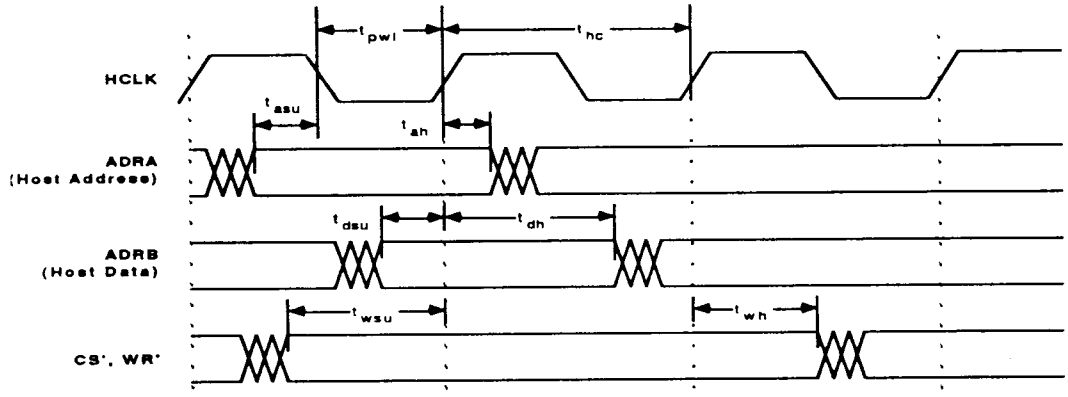


FIGURE 5 - SWITCHING WAVEFORMS



Telephone: (719) 540-7900 FAX (719) 540-7950

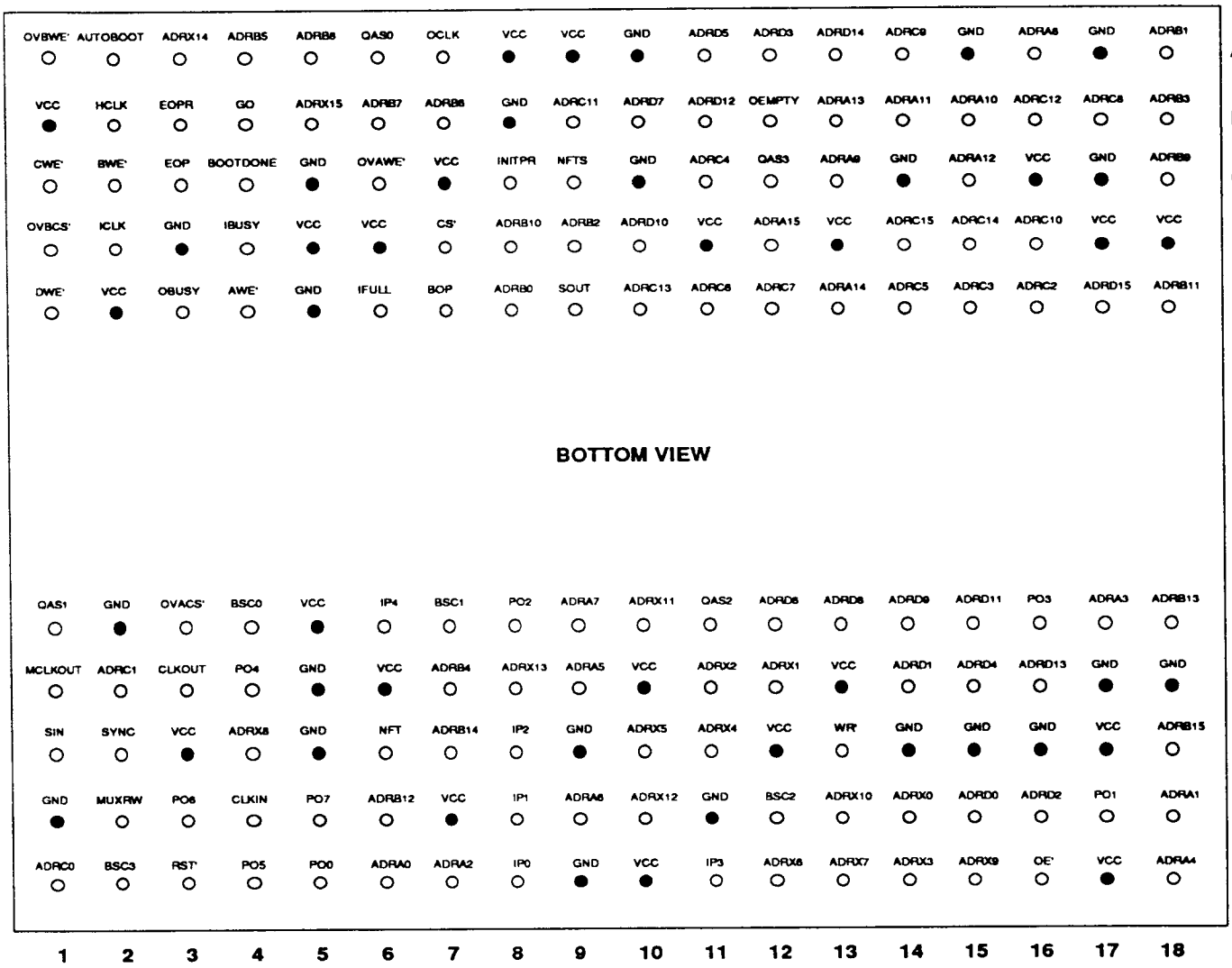
PACKAGING INFORMATION

A66210 Pin Definitions

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED
ADDRESS BUSES			
ADRA (15:0)	I/O	(Output) Address Bus for Memory A/(Input) Host Address Bus	16
ADRB (15:0)	I/O	(Output) Address Bus for Memory B/(Input) Host Data Bus	16
ADRC (15:0)	O	Address Bus for Memory C	16
ADRD (15:0)	O	Address Bus for Memocy D	16
ADRX (15:0)	O	Address Bus for Auxiliary Memory X	16
OE'	I	Output Enable: Tristates Address Buses, PO(7:0), IP(4:0) if High	1
MEMORY CONTROLS			
AWE'	O	Memory A Write Strobe	1
BWE'	O	Memory B Write Strobe	1
CWE'	O	Memory C Write Strobe	1
DWE'	O	Memory D Write Strobe	1
OVAWE'	O	Filter Overlap Memory A Write Strobe	1
OVBWE'	O	Filter Overlap Memory B Write Strobe	1
OVACS'	O	Filter Overlap Memory A Chip Select	1
OVBCS'	O	Filter Overlap Memory B Chip Select	1
PASS EXECUTION CONTROLS			
BOP	O	Beginning of Pass Signal	1
EOP	O	End of Pass Signal	1
EOPR	O	End of Process Signal	1
IBUSY	O	Input Data Collection in Progress	1
OBUSY	O	Output Data Dump in Progress	1
IFULL	O	Input Memory Full	1
OEMPTY	O	Output Memory Empty	1
HOST INTERFACE/INITIALIZATION CONTROLS			
AUTOBOOT	I	Autoboot from a Memory	1
BOOTDONE	O	PAC Autoboot Complete	1
CS'	I/O	(Input) PAC Chip Select from Host/(Output) Autoboot Memory Select	1
WR'	I	Write Strobe from Host	1
RST'	I	Reset Input	1
INITPR	O	Initializes External Processor	1
GO	I	Start Instruction Execution	1

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED
GENERAL COMMUNICATION SIGNALS			
PO (7:0)	I/O	(Output) Programmable Outputs from Internal Instruction/(Input) External Instruction Fields XSHF (1:0), MIXMD, NODE (4:0)	8
IP (4:0)	I/O	(Output) Internal Instruction Memory Pointer/ (Input) External PAC Instruction Field BSC (3:0)	5
BSC (3:0)	O	Bus Switch Code: Controls Internal Bus Multiplexers	4
MUXRW	O	Multiplexed Read Write (Single Memory System)	1
QUAD-MODE CONTROLS			
QAS0	O	Quad-Mode Address Strobe 0	1
QAS1	O	Quad-Mode Address Strobe 1	1
QAS2	O	Quad-Mode Address Strobe 2	1
QAS3	O	Quad-Mode Address Strobe 3	1
CLOCK SIGNALS			
CLKIN	I	System Clock Input (Frequency 4/Tm)	1
ICLK	I	Input Data Collection Clock	1
OCLK	I	Output Data Dump Clock	1
HCLK	I	Host Interface Clock	1
SYNC	I	System Clock Synchronization Signal	1
CLKOUT	O	Delayed System Clock Output (Frequency 4/Tm)	1
MCLKOUT	O	Machine-Cycle Clock Output (Frequency 1/Tm)	1
SERIAL SCAN FOR NON-FUNCTIONAL-TEST (NFT)			
NFT	I	NFT Testing in Progress	1
NFTS	I	NFT Scan In Progress	1
SIN	I	NFT Serial Scan Input	1
SOUT	I	NFT Serial Scan Output	1
SUPPLY			
VCC	I	Voltage Supply	22
GND	I	Ground	22
TOTAL PACKAGE PINS USED			180

A66210 Pinout

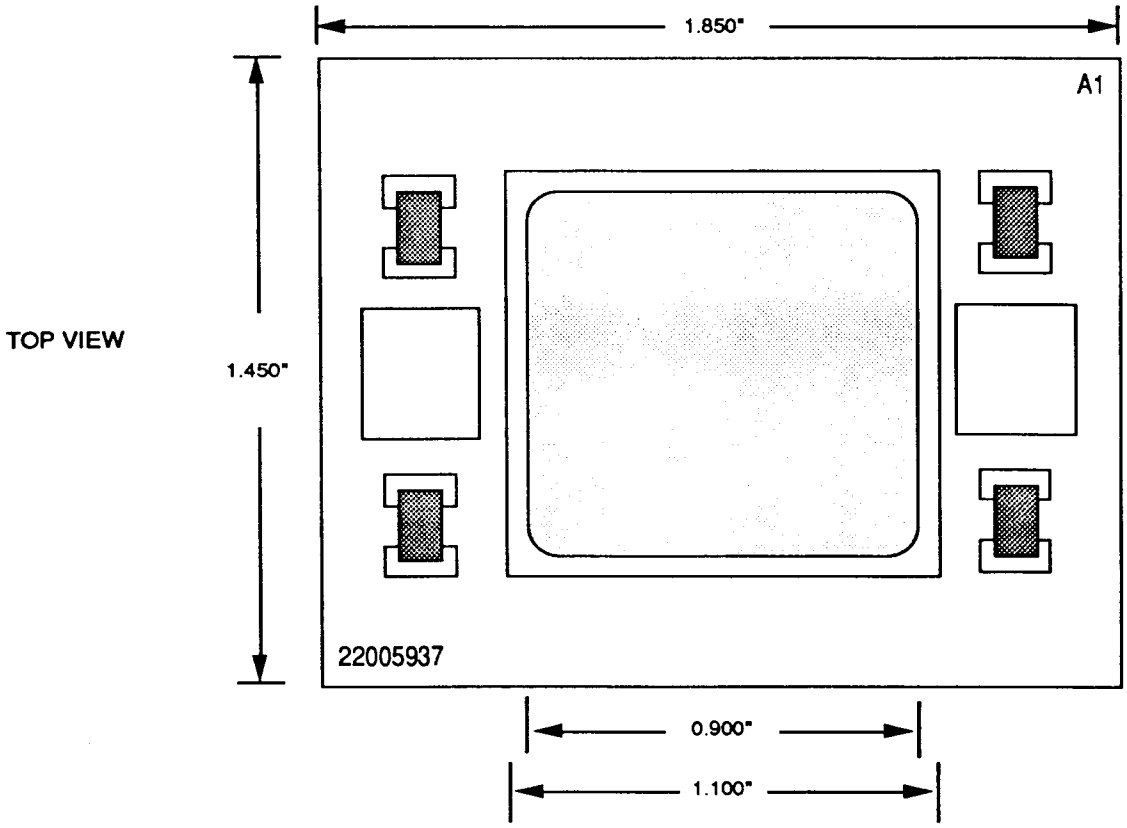


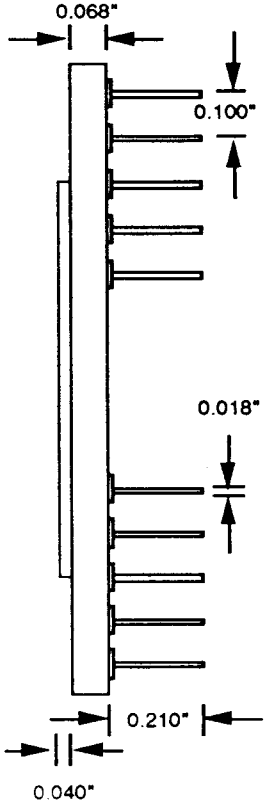
PAC Commerce Ltd

A66210 Pin Assignments

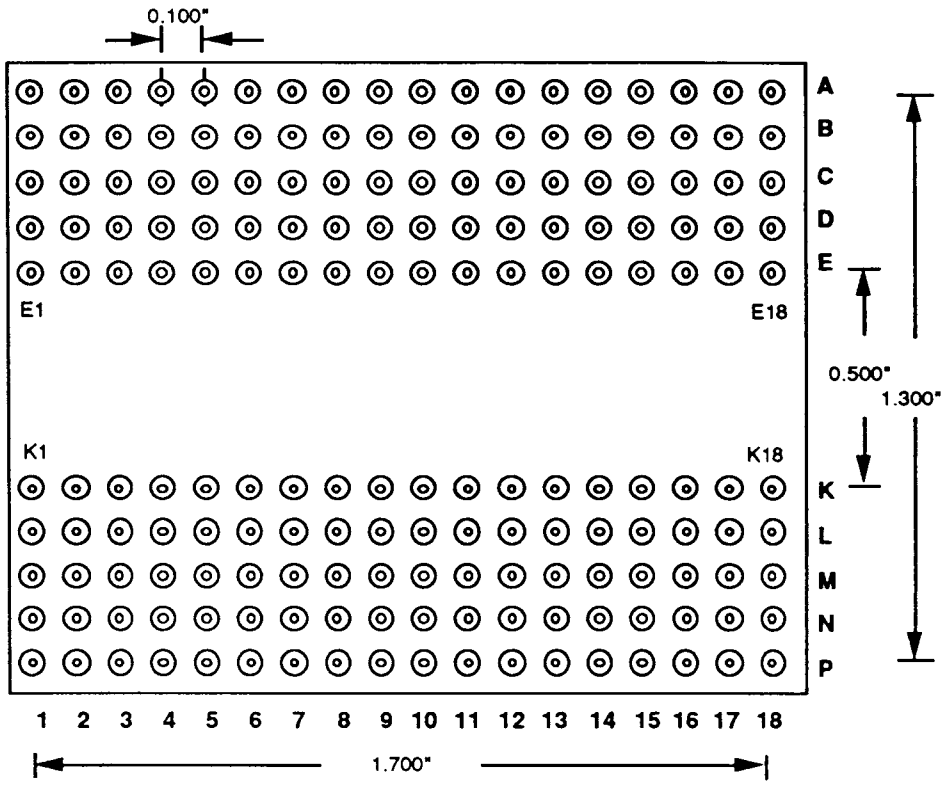
SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
ADRA(0)	P6	ADRB(8)	A5	ADRD(0)	N15	ADRX(8)	M4
ADRA(1)	N18	ADRB(9)	C18	ADRD(1)	L14	ADRX(9)	P15
ADRA(2)	P7	ADRB(10)	D8	ADRD(2)	N16	ADRX(10)	N13
ADRA(3)	K17	ADRB(11)	E18	ADRD(3)	A12	ADRX(11)	K10
ADRA(4)	P18	ADRB(12)	N6	ADRD(4)	L15	ADRX(12)	N10
ADRA(5)	L9	ADRB(13)	K18	ADRD(5)	A11	ADRX(13)	L8
ADRA(6)	N9	ADRB(14)	M7	ADRD(6)	K12	ADRX(14)	A3
ADRA(7)	K9	ADRB(15)	M18	ADRD(7)	B10	ADRX(15)	B5
ADRA(8)	A16	ADRC(0)	P1	ADRD(8)	K13	BSC(0)	K4
ADRA(9)	C13	ADRC(1)	L2	ADRD(9)	K14	BSC(1)	K7
ADRA(10)	B15	ADRC(2)	E16	ADRD(10)	D10	BSC(2)	N12
ADRA(11)	B14	ADRC(3)	E15	ADRD(11)	K15	BSC(3)	P2
ADRA(12)	C15	ADRC(4)	C11	ADRD(12)	B11	IP(0)	P8
ADRA(13)	B13	ADRC(5)	E14	ADRD(13)	L16	IP(1)	N8
ADRA(14)	E13	ADRC(6)	E11	ADRD(14)	A13	IP(2)	M8
ADRA(15)	D12	ADRC(7)	E12	ADRD(15)	E17	IP(3)	P11
ADRB(0)	E8	ADRC(8)	B17	ADRX(0)	N14	IP(4)	K6
ADRB(1)	A18	ADRC(9)	A14	ADRX(1)	L12	QAS0	A6
ADRB(2)	D9	ADRC(10)	D16	ADRX(2)	L11	QAS1	K1
ADRB(3)	B18	ADRC(11)	B9	ADRX(3)	P14	QAS2	K11
ADRB(4)	L7	ADRC(12)	B16	ADRX(4)	M11	QAS3	C12
ADRB(5)	A4	ADRC(13)	E10	ADRX(5)	M10	AUTOBOOT	A2
ADRB(6)	B7	ADRC(14)	D15	ADRX(6)	P12	BOOTDONE	C4
ADRB(7)	B6	ADRC(15)	D14	ADRX(7)	P13	GND	A17
PO(0)	P5	IBUSY	D4	VCC	A9	GND	A15
PO(1)	N17	ICLK	D2	VCC	B1	GND	B8
PO(2)	K8	IFULL	E6	VCC	C7	GND	C14
PO(3)	K16	INITPR	C8	VCC	D5	GND	C17
PO(4)	L4	MUXRW	N2	VCC	D6	GND	C10
PO(5)	P4	NFT	M6	VCC	D11	GND	C5
PO(6)	N3	NFTS	C9	VCC	D13	GND	D3
PO(7)	N5	OBUSY	E3	VCC	D17	GND	K2
BOP	E7	OCLK	A7	VCC	D18	GND	L5
EOP	C3	OE'	P16	VCC	E2	GND	L17
CLKIN	N4	OEMPTY	B12	VCC	K5	GND	L18
CLKOUT	L3	OVACS'	K3	VCC	L6	GND	M16
MCLKOUT	L1	OVAWE'	C6	VCC	L10	GND	M15
AWE'	E4	OVBCS'	D1	VCC	L13	GND	M14
BWE'	C2	OVBWE'	A1	VCC	M3	GND	M9
CWE'	C1	RST'	P3	VCC	M12	GND	M5
DWE'	E1	SIN	M1	VCC	M17	GND	N1
CS'	D7	SOUT	E9	VCC	N7	GND	N11
EOPR	B3	WR'	M13	VCC	P10	GND	P9
HCLK	B2	SYNC	M2	VCC	P17	GND	A10
GO	B4	VCC	A8	VCC	C16	GND	E5

A66210 Package Drawing





SIDE V IEW



BOTTOM VIEW

Colorado Springs, CO 80906 Telephone: (719) 540-7900 FAX (719) 540-7950

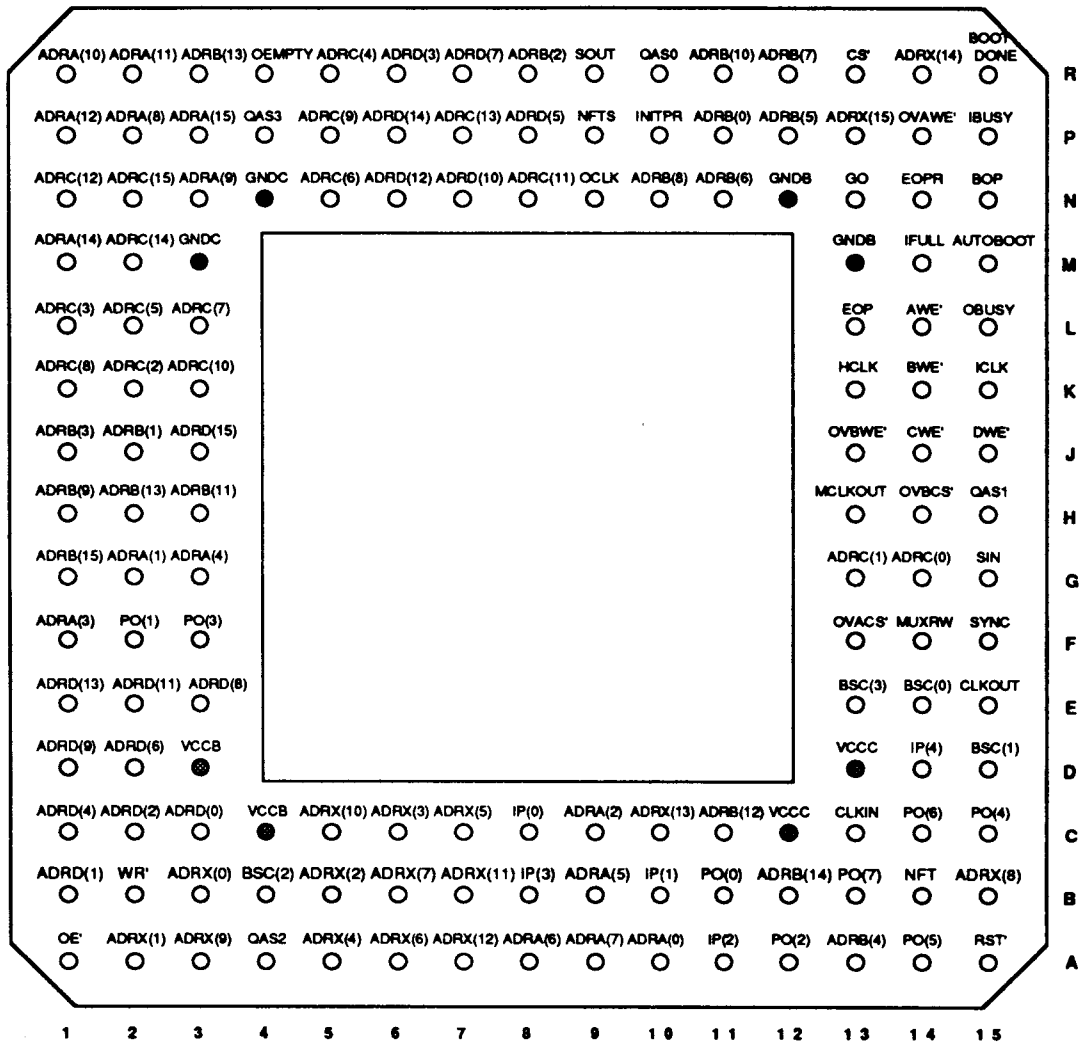
PACKAGING INFORMATION

A66211 Pin Descriptions

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED
ADDRESS BUSES			
ADRA (15:0)	I/O	(Output) Address Bus for Memory A/(Input) Host Address Bus	16
ADRB (15:0)	I/O	(Output) Address Bus for Memory B/(Input) Host Data Bus	16
ADRC (15:0)	O	Address Bus for Memory C	16
ADRD (15:0)	O	Address Bus for Memocy D	16
ADRX (15:0)	O	Address Bus for Auxiliary Memory X	16
OE'	I	Output Enable: Tristates Address Buses, PO(7:0), IP(4:0) If High	1
MEMORY CONTROLS			
AWE'	O	Memory A Write Strobe	1
BWE'	O	Memory B Write Strobe	1
CWE'	O	Memory C Write Strobe	1
DWE'	O	Memory D Write Strobe	1
OVAWE'	O	Filter Overlap Memory A Write Strobe	1
OVBWE'	O	Filter Overlap Memory B Write Strobe	1
OVACS'	O	Filter Overlap Memory A Chip Select	1
OVBCS'	O	Filter Overlap Memory B Chip Select	1
PASS EXECUTION CONTROLS			
BOP	O	Beginning of Pass Signal	1
EOP	O	End of Pass Signal	1
EOPR	O	End of Process Signal	1
IBUSY	O	Input Data Collection in Progress	1
OBUSY	O	Output Data Dump in Progress	1
IFULL	O	Input Memory Full	1
OEMPTY	O	Output Memory Empty	1
HOST INTERFACE/INITIALIZATION CONTROLS			
AUTOBOOT	I	Autoboot from a Memory	1
BOOTDONE	O	PAC Autoboot Complete	1
CS'	I/O	(Input) PAC Chip Select from Host/(Output) Autoboot Memory Select	1
WR'	I	Write Strobe from Host	1
RST'	I	Reset Input	1
INITPR	O	Initializes External Processor	1
GO	I	Start Instruction Execution	1

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED
GENERAL COMMUNICATION SIGNALS			
PO (7:0)	I/O	(Output) Programmable Outputs from Internal Instruction/(Input) External Instruction Fields XSHF (1:0), MIXMD, NODE (4:0)	8
IP (4:0)	I/O	(Output) Internal Instruction Memory Pointer/ (Input) External PAC Instruction Field BSC (3:0)	5
BSC (3:0)	O	Bus Switch Code: Controls Internal Bus Multiplexers	4
MUXRW	O	Multiplexed Read Write (Single Memory System)	1
QUAD-MODE CONTROLS			
QAS0	O	Quad-Mode Address Strobe 0	1
QAS1	O	Quad-Mode Address Strobe 1	1
QAS2	O	Quad-Mode Address Strobe 2	1
QAS3	O	Quad-Mode Address Strobe 3	1
CLOCK SIGNALS			
CLKIN	I	System Clock Input (Frequency 4/Tm)	1
ICLK	I	Input Data Collection Clock	1
OCLK	I	Output Data Dump Clock	1
HCLK	I	Host Interface Clock	1
SYNC	I	System Clock Synchronization Signal	1
CLKOUT	O	Delayed System Clock Output (Frequency 4/Tm)	1
MCLKOUT	O	Machine-Cycle Clock Output (Frequency 1/Tm)	1
SERIAL SCAN FOR NON-FUNCTIONAL-TEST (NFT)			
NFT	I	NFT Testing in Progress	1
NFTS	I	NFT Scan in Progress	1
SIN	I	NFT Serial Scan Input	1
SOUT	I	NFT Serial Scan Output	1
SUPPLY			
VCC	I	Voltage Supply	4
GND	I	Ground	4
TOTAL PACKAGE PINS USED			144

A66211 Pinout

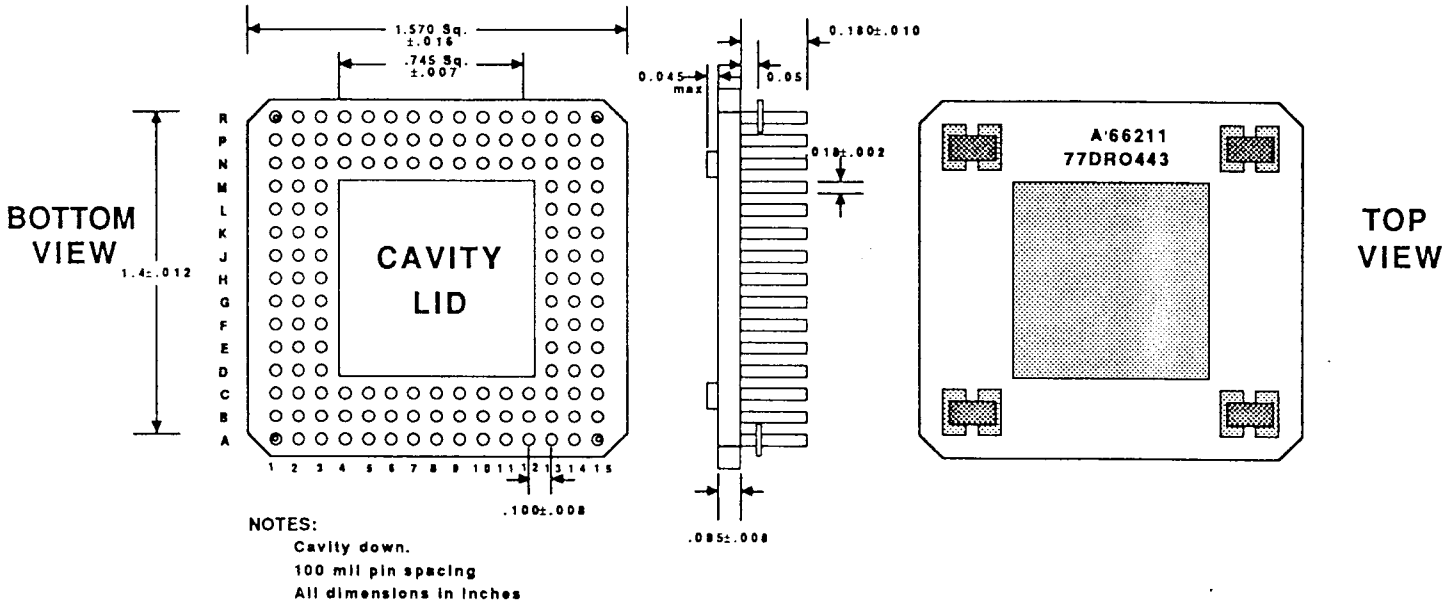


BOTTOM VIEW

A66211 Pin Assignments

SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
ADRA(0)	A10	ADRB(8)	N10	ADRD(0)	C3	ADRX(8)	B15
ADRA(1)	G2	ADRB(9)	H1	ADRD(1)	B1	ADRX(9)	A3
ADRA(2)	C9	ADRB(10)	R11	ADRD(2)	C2	ADRX(10)	C5
ADRA(3)	F1	ADRB(11)	H3	ADRD(3)	R6	ADRX(11)	B7
ADRA(4)	G3	ADRB(12)	C11	ADRD(4)	C1	ADRX(12)	A7
ADRA(5)	B9	ADRB(13)	H2	ADRD(5)	P8	ADRX(13)	C10
ADRA(6)	A8	ADRB(14)	B12	ADRD(6)	D2	ADRX(14)	R14
ADRA(7)	A9	ADRB(15)	G1	ADRD(7)	R7	ADRX(15)	P13
ADRA(8)	P2	ADRC(0)	G14	ADRD(8)	E3	BSC(0)	E14
ADRA(9)	N3	ADRC(1)	G13	ADRD(9)	D1	BSC(1)	D15
ADRA(10)	R1	ADRC(2)	K2	ADRD(10)	N7	BSC(2)	B4
ADRA(11)	R2	ADRC(3)	L1	ADRD(11)	E2	BSC(3)	E13
ADRA(12)	P1	ADRC(4)	R5	ADRD(12)	N6	IP(0)	C8
ADRA(13)	R3	ADRC(5)	L2	ADRD(13)	E1	IP(1)	B10
ADRA(14)	M1	ADRC(6)	N5	ADRD(14)	P6	IP(2)	A11
ADRA(15)	P3	ADRC(7)	L3	ADRD(15)	J3	IP(3)	B8
ADRB(0)	P11	ADRC(8)	K1	ADRX(0)	B3	IP(4)	D14
ADRB(1)	J2	ADRC(9)	P5	ADRX(1)	A2	QAS0	R10
ADRB(2)	R8	ADRC(10)	K3	ADRX(2)	B5	QAS1	H15
ADRB(3)	J1	ADRC(11)	N8	ADRX(3)	C6	QAS2	A4
ADRB(4)	A13	ADRC(12)	N1	ADRX(4)	A5	QAS3	P4
ADRB(5)	P12	ADRC(13)	P7	ADRX(5)	C7	AUTOBOOT	M15
ADRB(6)	N11	ADRC(14)	M2	ADRX(6)	A6	BOOTDONE	R15
ADRB(7)	R12	ADRC(15)	N2	ADRX(7)	B6	GO	N13
PO(0)	B11	MCLKOUT	H13	MUXRW	F14	SIN	G15
PO(1)	F2	AWE'	L14	NFT	B14	SOUT	R9
PO(2)	A12	BWE'	K14	NFTS	P9	WR'	B2
PO(3)	F3	CWE'	J14	OBUSY	L15	SYNC	F15
PO(4)	C15	DWE'	J15	OCLK	N9	VCCB	C4
PO(5)	A14	CS'	R13	OE'	A1	VCCB	D3
PO(6)	C14	EOPR	N14	OEMPTY	R4	VCCC	C12
PO(7)	B13	HCLK	K13	OVACS'	F13	VCCC	D13
BOP	N15	IBUSY	P15	OVAWE'	P14	GNDB	M13
EOP	L13	ICLK	K15	OVBCS'	H14	GNDB	N12
CLKIN	C13	IFULL	M14	OVBWE'	J13	GNDC	M3
CLKOUT	E15	INITPR	P10	RST'	A15	GNDC	N4

A66211 Package Drawing



NOTES:
Cavity down.
100 mil pin spacing
All dimensions in inches

Ordering Information

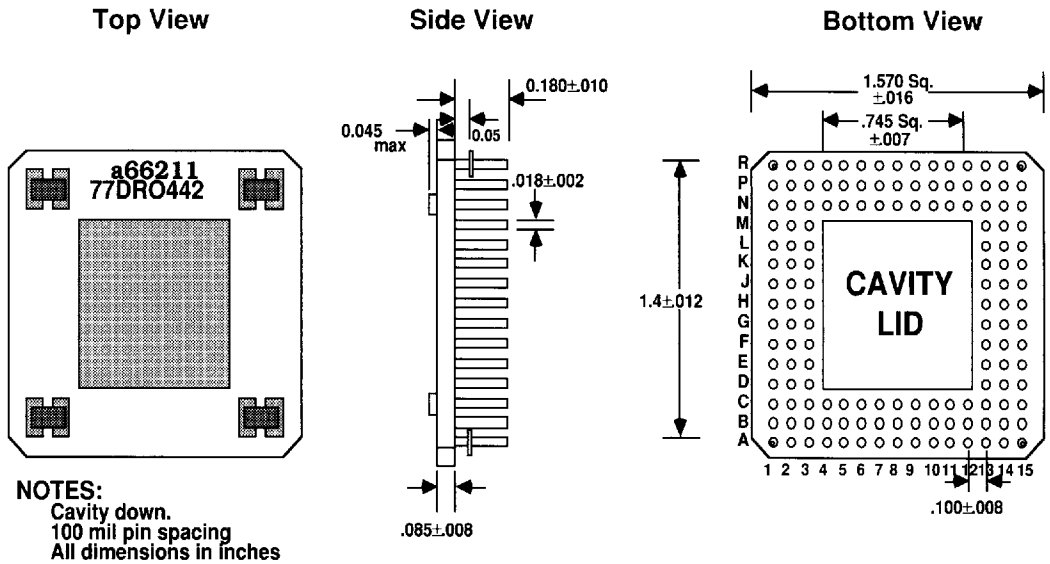
Product Number	Speed	Temperature Range(Case)	Voltage Range	Number of Pins	Package Type
A66210BCG	25 MHz	0 °C to +70 ° C	4.75V - 5.25V	180	Pin Grid Array
A66210BMG/H	25 MHz	-55 °C to +125 ° C	4.75V - 5.25V	180	Pin Grid Array
A66210ACG	40 MHz	0 °C to +70 ° C	4.75V - 5.25V	180	Pin Grid Array
A66210AMG/H	35 MHz	-55 °C to +125 ° C	4.75V - 5.25V	180	Pin Grid Array
A66211BCG	25 MHz	0 °C to +70 ° C	4.75V - 5.25V	144	Pin Grid Array
A66211BMG/883	25 MHz	-55 °C to +125 ° C	4.75V - 5.25V	144	Pin Grid Array
A66211ACG	40 MHz	0 °C to +70 ° C	4.75V - 5.25V	144	Pin Grid Array
A66211AMG/H	35 MHz	-55 °C to +125 ° C	4.75V - 5.25V	144	Pin Grid Array

Array Microsystems, Inc. 1420 Quail Lake Loop Colorado Springs, CO 80906 Telephone: (719) 540-7900 FAX (719) 540-7950

T-90-20

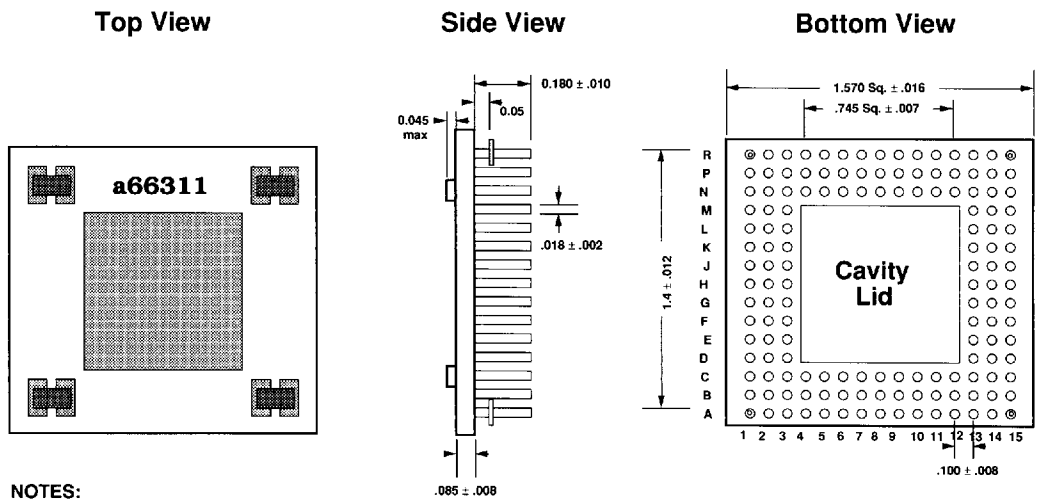
Package Drawings (cont.)

a66211 PaC (144 PGA)



NOTES:
Cavity down.
100 mil pin spacing
All dimensions in inches

a66311 RaS (144 PGA)



NOTES:
Cavity down.
100 mil pin spacing
All dimensions in inches