Chapter 18

Electrical Specifications and Timings

This chapter contains electrical and timing information for the TMS370 family devices. This information is presented according to device category.

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18.1 Timing Parameter Symbols

Timing parameter symbols occur throughout this chapter. They were created in accordance with JEDEC standard 100A. To keep the symbols short, some of the signal names and other operational terms were abbreviated as follows:

A	Address	RXD	SCIRXD
AR	Array mode	S	Slave mode
B	Byte mode	SC	SYSCLK
CI	XTAL2/CLKIN	SCC	SCICLK
D	Data	SIMO	SPISIMO
E	$\overline{\text{EDS}}$	SOMI	SPISOMI
FE	Final	SPC	SPICLK
IE	Initial	TXD	SCITXD
M	Master mode	W	Write
PGM	Programming	WT	$\overline{\text{WAIT}}$
R	Read		

Lowercase subscripts and their meanings are:

c	Cycle time (period)	r	Rise time
d	Delay time	su	Setup time
f	Fall time	v	Valid time
h	Hold time	w	Pulse duration (width)

The following additional letters are used with these meanings:

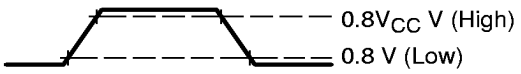
H	High	V	Valid
L	Low	Z	High impedance

18.2 Parameter Measurements

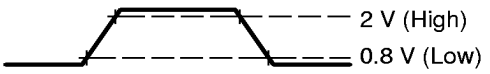
All timings are calculated between high and low measurement points as indicated in Figure 18–1.

Figure 18–1. Measurement Points for Timings

(a) XTAL2/CLKIN measurement points



(b) General measurement points



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18.3 Absolute Maximum Ratings for All TMS370 Devices

For all TMS370 devices, Table 18–1 provides the absolute maximum ratings over the operating free-air temperature range. This operating free-air temperature range is specified for your device in its respective section of this chapter.

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions for the specific device is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 18–1. Absolute Maximum Ratings Over Operating Free-Air Temperature Range (See Note 1)

Parameter		Maximum Rating
Supply voltage range, V_{CC} (see Note 1)		–0.6 V to 7 V
Input voltage range	All pins except MC	–0.6 V to 7 V
	MC	–0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ V or $V_I > V_{CC}$)		±20 mA
Output clamp current, I_{OK} ($V_O < 0$ V or $V_O > V_{CC}$)		±20 mA
Continuous output current per buffer, I_O (V_O = 0 V to V_{CC}) (see Note 2)		±10 mA
Maximum supply current, I_{CC}		170 mA
Maximum supply current, I_{SS}		–170 mA
Continuous power dissipation	TMS370Cx0xA, TMS370Cx0x, TMS370Cx1xA, TMS370Cx1xB, TMS370CxCxA	500 mW
	TMS370Cx32A	800 mW
	TMS370Cx2xA, TMS370Cx2x, TMS370Cx36A, TMS370Cx4xA, TMS370Cx5xA, TMS370Cx5xB, TMS370Cx6xA, TMS370Cx7xA, TMS370Cx8xA, TMS370Cx9xA, TMS370CxAxA, TMS370CxBxA	1 W
Storage temperature range, T_{stg}		–65°C to 150°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS} (ground).

2) Electrical characteristics are specified with all output buffers loaded with the specified I_O. Exceeding the specified I_O in any buffer may affect the levels on other buffers.

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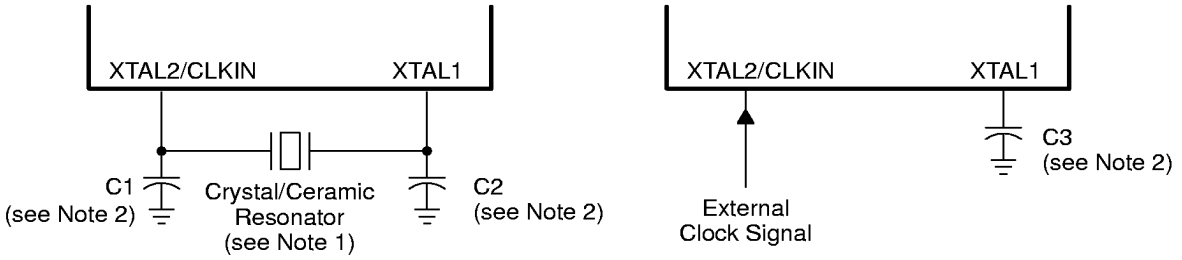
18.4 External Crystal/Clock Connections and Typical Circuits for Loads and Buffers

Figure 18–2 illustrates how to connect the crystal/ceramic resonator and the external clock signal. This figure is valid for all TMS370 family devices.

Figure 18–2. Recommended Crystal/Clock Connections

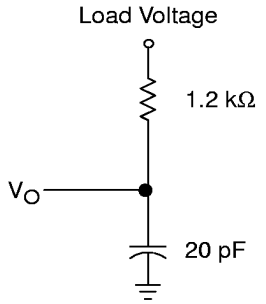


Notes: 1) The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.

2) The values of C1 and C2 are typically 15 pF and the value of C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 18–3 is an output load circuit that you can use for any TMS370 device.

Figure 18–3. Typical Output Load Circuit



Case 1: $V_O = V_{OH} = 2.4$ V; Load Voltage = 0 V
Case 2: $V_O = V_{OL} = 0.4$ V; Load Voltage = 2.1 V

Note: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

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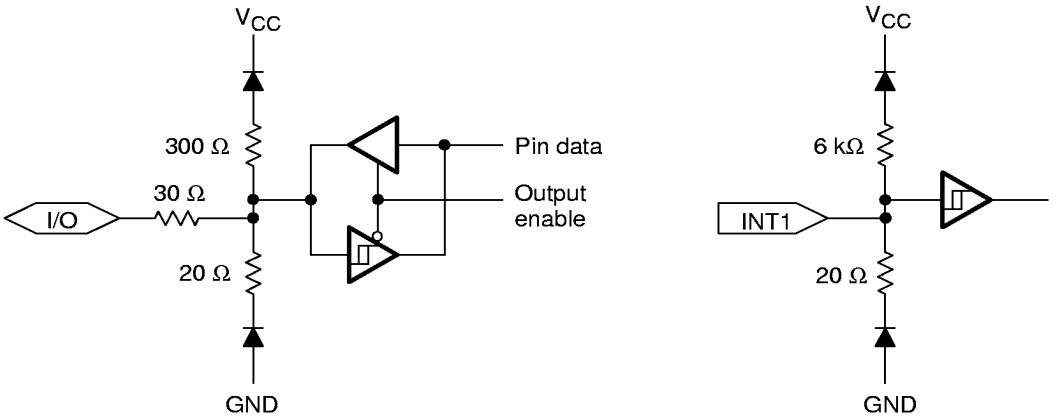
Figure 18–4. Typical Buffer Circuitry



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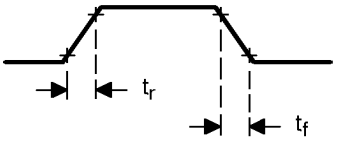
18.5 General-Purpose Output Signal Timings

Refer to Sections 18.1 and 18.2 for timing symbol definitions and parameter measurement points. The timings shown in this section are valid for all TMS370 family devices.

Table 18–2. General-Purpose Output Signal Timing Requirements

Parameter		Min	Nom	Max	Unit
t_r	Rise time		30		ns
t_f	Fall time		30		ns

Figure 18–5. Switching Time Measurement Points



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18.6 EPROM/EEPROM Specifications

Refer to Sections 18.1 and 18.2 for timing symbol definitions and parameter measurement points. The timings shown in this section are valid for all ’C702, ’C722, ’CxxxA, and ’CxxxB family devices except the ’C3xxA device.

Table 18–3. EEPROM Timing Requirements for Programming

Parameter		Min	Max	Unit
$t_{w(PGM)B}$	Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$	Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

Table 18–4. Recommended EPROM Operating Conditions for Programming

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage		4.75	5.5	6	V
V_{PP}	Supply voltage at MC pin		13	13.2	13.5	V
I_{PP}	Supply current at MC pin during programming (V_{PP} = 13 V)			30	50	mA
SYSCLK	System clock operating frequency	Divide-by-4 clock	0.5		5	MHz
		Divide-by-1 clock	2		5	MHz

Table 18–5. EPROM Timing Requirements for Programming

Parameter		Min	Nom	Max	Unit
$t_{w(EPGM)}$	Pulse duration, programming signal (see Note)	0.40	0.50	3	ms

Note: Programming pulse is active when both EXE (EPCTL.0) and VPPS (EPCTL.6) are set.

Note:

The parameters V_{PP} and $t_{w(EPGM)}$ for EPROM are different for the TMS370Cxxx devices (vs. the TMS370CxxxA or TMS370CxxxB devices). Refer to subsection A.9.3, *Differences in EPROM Specifications,* on page A-10.

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18.7 TMS370Cx0xA and TMS370Cx0x Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx0xA and TMS370Cx0x categories. These devices include the TMS370C002A, TMS370C302A, TMS370C702, and SE370C702.

18.7.1 TMS370Cx0xA and TMS370Cx0x Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–6 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 18–6. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage (see Note 1)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	$0.8V_{CC}$		V_{CC}	V
		$\overline{\text{RESET}}$	$0.7V_{CC}$		V_{CC}	V
V_{MC}	MC (mode control) voltage	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microcomputer mode	V_{SS}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS} (ground).
2) $\overline{\text{RESET}}$ must be activated externally when V_{CC} or SYSCLK is out of the recommended operating range.

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Table 18–7. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V ≤ V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 1)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC}			±10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 4)		See Notes 2 and 3 SYSCLK = 5 MHz		20	36	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		13	25	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		5	11	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 5)		See Notes 2 and 3 SYSCLK = 5 MHz		10	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		6.5	11	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.5	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 6)		See Notes 2 and 3 SYSCLK = 3 MHz		4.5	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		1.5	3.0	mA
I_{CC}	Supply current (HALT mode)		See Note 2 XTAL2/CLKIN < 0.2 V		1	30	µA

Notes: 1) Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.
2) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2 V.
3) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
4) Maximum operating current = 5.6 (SYSCLK) + 8 mA.
5) Maximum standby current = 3 (SYSCLK) + 2 mA (OSC POWER bit = 0).
6) Maximum standby current = 2.24 (SYSCLK) + 1.9 mA (OSC POWER bit = 1, only valid up to 3 MHz of SYSCLK).

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18.7.2 TMS370Cx0xA and TMS370Cx0x Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–8. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–6.

2) This pulse can be either a high pulse, as illustrated in Figure 18–6, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–6. External Clock Timing for Divide-by-4 Clock

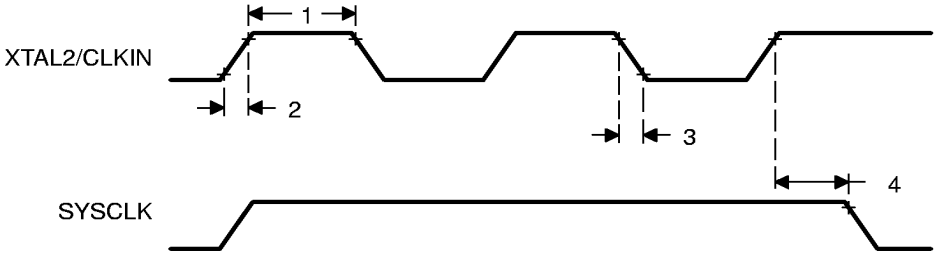

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Table 18–9. External Clocking Requirements for Divide-by-1 Clock (PLL) (see Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–6.

2) This pulse can be either a high pulse, as illustrated in Figure 18–7, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–7. External Clock Timing for Divide-by-1 Clock

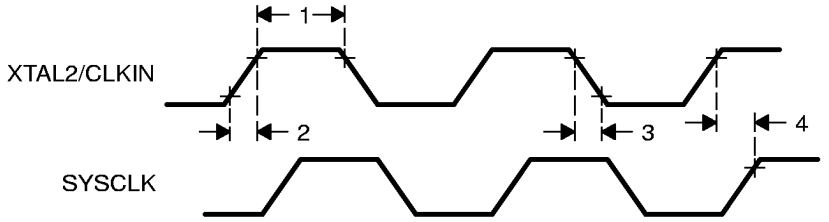
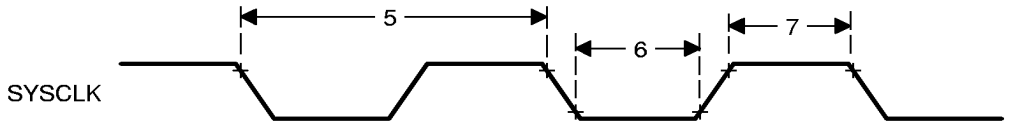


Table 18–10. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system clock cycle time = 1 / SYSCLK

Figure 18–8. SYSCLK TIming



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18.8 TMS370Cx1xA and TMS370Cx1xB Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx1xA and the TMS370Cx1xB categories. These devices include the TMS370C010A, TMS370C012A, TMS370C310A, TMS370C311A, TMS370C312A, TMS370C712A, TMS370C712B, SE370C712A, and SE370C712B.

18.8.1 TMS370Cx1xA and TMS370Cx1xB Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–11 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 18–11. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage (see Note 1)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	$0.8V_{CC}$		V_{CC}	V
		$\overline{\text{RESET}}$	$0.7V_{CC}$		V_{CC}	V
V_{MC}	MC (mode control) voltage	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microcomputer mode	V_{SS}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS} (ground).
2) $\overline{\text{RESET}}$ must be externally activated when V_{CC} or SYSCLK is not within the recommended operating range.

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Table 18–12. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V ≤ V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 1)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC}			± 10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 4)		See Notes 2 and 3 SYSCLK = 5 MHz		20	36	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		13	25	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		5	11	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 5)		See Notes 2 and 3 SYSCLK = 5 MHz		10	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		6.5	11	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.5	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 6)		See Notes 2 and 3 SYSCLK = 3 MHz		4.5	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		1.5	3.0	mA
I_{CC}	Supply current (HALT mode)		See Note 2 XTAL2/CLKIN < 0.2 V		1	30	µA

Notes: 1) Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.
2) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2 V.
3) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).
4) Maximum operating current = 5.6(SYSCLK) + 8 mA.
5) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).
6) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit = 1; valid only up to 3-MHz SYSCLK).

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18.8.2 TMS370Cx1xA and TMS370Cx1xB Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–13. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–11.

2) This pulse may be either a high pulse, as illustrated in Figure 18–9, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–9. External Clock Timing for Divide-by-4 Clock

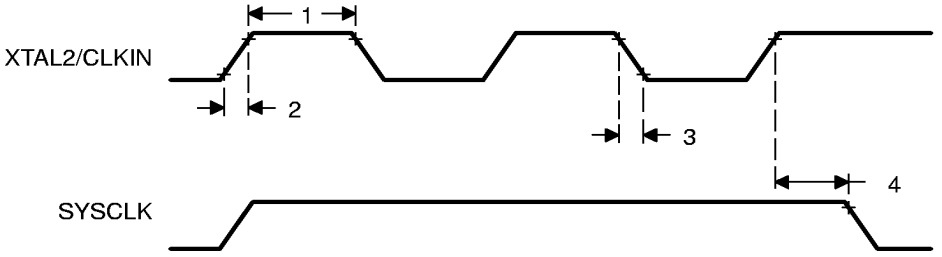

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Table 18–14. External Clocking Requirements for Divide-by-1 Clock (PLL) (see Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–11.

2) This pulse may be either a high pulse, as illustrated in Figure 18–10, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–10. External Clock Timing for Divide-by-1 Clock

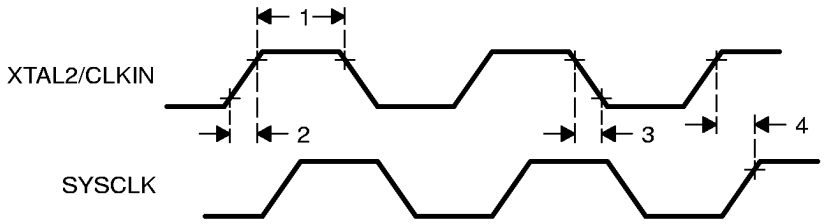
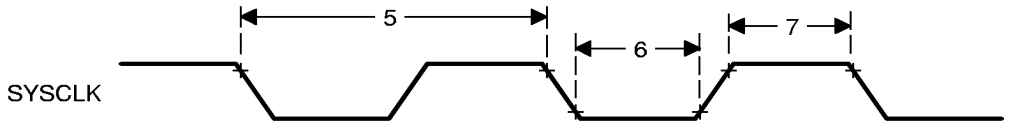


Table 18–15. Switching Characteristics and Timing Requirements (see Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system clock cycle time = 1 / SYSCLK

Figure 18–11. SYSCLK Timing



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18.9 TMS370Cx2xA and TMS370Cx2x Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx2xA TMS370Cx2x categories. These devices include the TMS370C020A, TMS370C022A, TMS370C320A, TMS370C322A, TMS370C722, and SE370C722.

18.9.1 TMS370Cx2xA and TMS370Cx2x Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–16 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 18–16. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	$0.8V_{CC}$		V_{CC}	V
		$\overline{\text{RESET}}$	$0.7V_{CC}$		V_{CC}	V
V_{MC}	MC (mode control) voltage	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microcomputer mode	V_{SS}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltages are with respect to V_{SS} (ground).
2) $\overline{\text{RESET}}$ must be externally activated when V_{CC} or SYSCLK is out of the recommended operating range.

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Table 18–17. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 1)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC}			±10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 4)		See Notes 2 and 3 SYSCLK = 5 MHz		30	45	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		20	30	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		7	11	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 5)		See Notes 2 and 3 SYSCLK = 5 MHz		10	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		8	11	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.5	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 6)		See Notes 2 and 3 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.0	mA
I_{CC}	Supply current (HALT mode)		See Note 2 XTAL2/CLKIN < 0.2 V		2	30	µA

Notes: 1) Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.

2) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} − 0.2 V.

3) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).

4) Maximum operating current = 7.6(SYSCLK) + 7 mA.

5) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).

6) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit = 1; valid only up to 3-MHz SYSCLK).

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18.9.2 TMS370Cx2xA and TMS370Cx2x Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–18. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–16.

2) This pulse may be either a high pulse, as illustrated in Figure 18–12, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–12. External Clock Timing for Divide-by-4 Clock

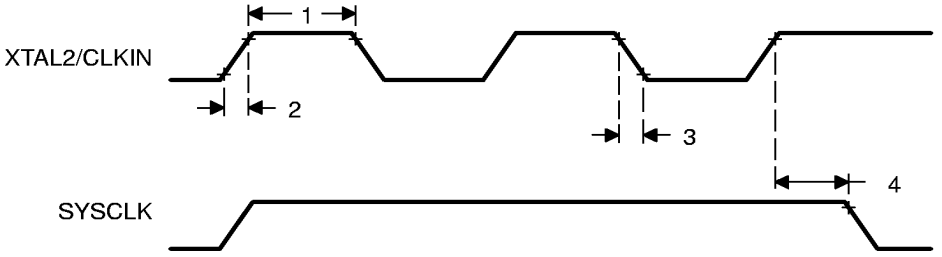

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Table 18–19. External Clocking Requirements for Divide-by-1 Clock (PLL) (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–16.
2) This pulse can be either a high pulse, as illustrated in Figure 18–13, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.
3) SYSCLK = CLKIN/1

Figure 18–13. External Clock Timing for Divide-by-1 Clock

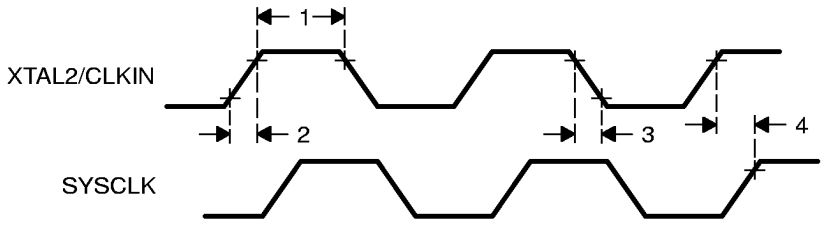
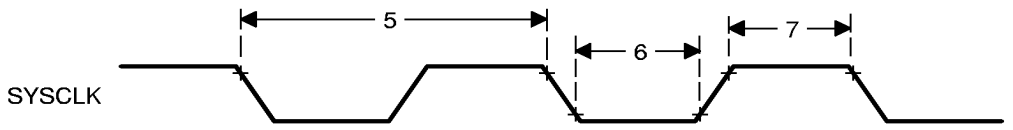


Table 18–20. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock	200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system-clock cycle time = 1/SYSCLK

Figure 18–14. SYSCLK Timing



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18.10 TMS370Cx32A Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx32A category. These devices include the TMS370C032A, TMS370C332A, TMS370C732A, and SE370C732A.

18.10.1 TMS370Cx32A Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–21 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 18–21. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC1}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{CC3}	Analog supply voltage		4.5	5	5.5	V
V_{SS3}	Analog supply ground		–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS1}		0.8	V
		MC, normal operation	V_{SS1}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC1}	V
		XTAL2/CLKIN	$0.8V_{CC1}$		V_{CC1}	V
		$\overline{\text{RESET}}$	$0.7V_{CC1}$		V_{CC1}	V
V_{MC}	MC (mode control) voltage	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microcomputer mode	V_{SS1}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS1}.
2) $\overline{\text{RESET}}$ must be externally activated when V_{CC1} or SYSCLK is not within the recommended operating range.

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Table 18–22. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V ≤ V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 1)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC1}			± 10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC1}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC1}	Supply current (operating mode) OSC POWER bit = 0		See Notes 2 and 3 SYSCLK = 5 MHz		35	45	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		25	35	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		10	14	mA
I_{CC1}	Supply current (STANDBY mode) OSC POWER bit = 0		See Notes 2 and 3 SYSCLK = 5 MHz		12	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		8	13	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		3	4	mA
I_{CC1}	Supply current (STANDBY mode) OSC POWER bit = 1		See Notes 2 and 3 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.0	mA
I_{CC1}	Supply current (HALT mode)		See Note 2 XTAL2/CLKIN < 0.2 V		15	40	µA

Notes: 1) Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.
2) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} – 0.2 V.
3) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).

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18.10.2 TMS370Cx32A Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–23. External Clocking Requirements For Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–21.

2) This pulse may be either a high pulse, as illustrated in Figure 18–15, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–15. External Clock Timing for Divide-by-4 Clock

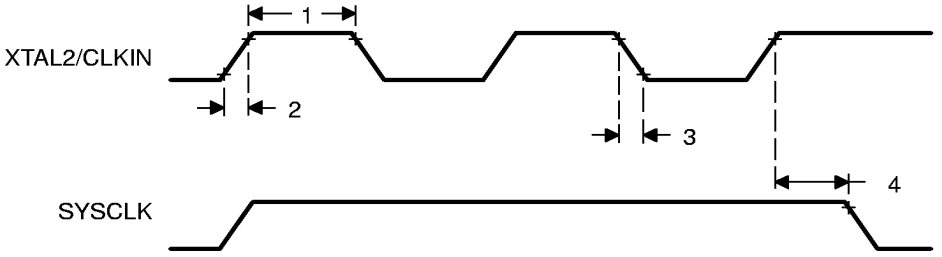

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Table 18–24. External Clocking Requirements for Divide-by-1 Clock (PLL) (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–21.

2) This pulse can be either a high pulse, as illustrated in Figure 18–16, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–16. External Clock Timing for Divide-by-1 Clock

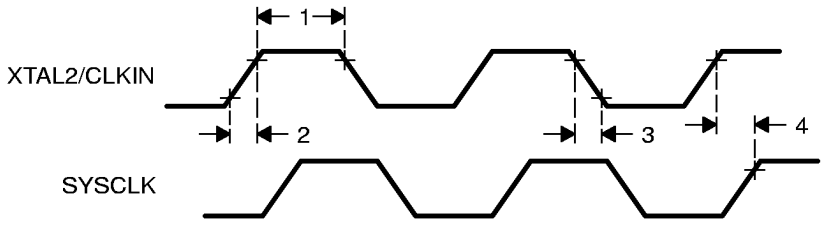
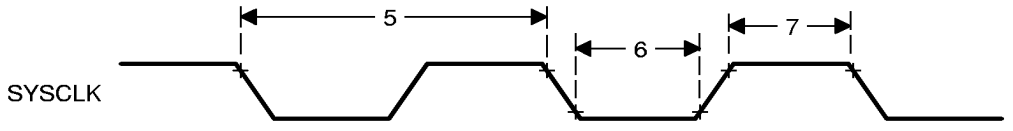


Table 18–25. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock	200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c$–20	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c$ + 20	ns

Note: t_c = system clock cycle time = 1 / SYSCLK

Figure 18–17. SYSCLK Timing



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18.11 TMS370Cx36A Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx36A category. These devices include the TMS370C036A, TMS370C736A, and SE370C736A.

18.11.1 TMS370Cx36A Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–26 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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Table 18–26. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC1}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{CCSTBY}	Standby RAM supply voltage		4.5	5	5.5	V
V_{CCSTBY}	Standby RAM data retention supply voltage (see Note 2)		3		5.5	V
V_{CC3}	Analog supply voltage		4.5	5	5.5	V
V_{SS3}	Analog supply ground		–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS1}		0.8	V
		MC, normal operation	V_{SS1}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC1}	V
		XTAL2/CLKIN	$0.8V_{CC1}$		V_{CC1}	V
		$\overline{\text{RESET}}$	$0.7V_{CC1}$		V_{CC1}	V
V_{MC}	MC (mode control) voltage	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microcomputer mode	V_{SS1}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS1}.

2) $\overline{\text{RESET}}$ must be externally activated when V_{CC1} or SYSCLK is not within the recommended operating range.

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Table 18–27. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage, all outputs		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage	All outputs except PACT outputs	I_{OH} = −50 µA	$0.9V_{CC1}$			V
		PACT outputs	I_{OH} = −50 µA	$0.7V_{CC1}$			V
		All outputs	I_{OH} = −2 mA	2.4			V
I_I	Input current	MC pin	0 V < V_I < 0.3 V			10	µA
			0.3 V < V_I < V_{CC1} − 0.3 V			50	µA
			V_{CC1} − 0.3 < V_I < V_{CC1} + 0.3 V			10	µA
			V_{CC1} + 0.3 V < V_I < 13 V			650	µA
		I/O pins	0 V < V_I < V_{CC1}			±10	µA
I_{OL}	Low-level output current, all outputs		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current, all outputs		V_{OH} = 0.9 V_{CC1}	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC1}	Supply current (operating mode) OSC POWER bit = 0		See Notes 1 and 2 SYSCLK = 5 MHz		36	45	mA
	Supply current (STANDBY mode) OSC POWER bit = 0		See Notes 1 and 2 SYSCLK = 5 MHz		7	12	mA
	Supply current (HALT mode)		See Notes 1 and 2 XTAL2/CLKIN < 0.2 V		5	30	µA
I_{CCSTBY}	Standby RAM supply current (operating mode) OSC POWER bit = 0		SYSCLK = 5 MHz V_{CCSTBY} = 4.5 V		1	1.5	mA

Notes: 1) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} − 0.2 V.

2) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).

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18.11.2 TMS370Cx36A Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–28. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–26.

2) This pulse may be either a high pulse, as illustrated in Figure 18–18, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–18. External Clock Timing for Divide-by-4 Clock

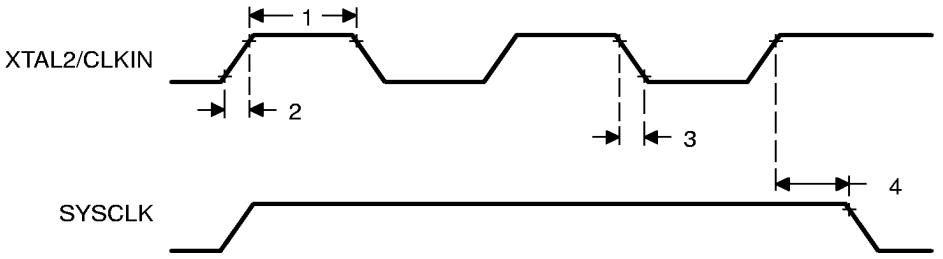

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Table 18–29. External Clocking Requirements For Divide-by-1 Clock (PLL) (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–26.

2) This pulse can be either a high pulse, as illustrated in Figure 18–19, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–19. External Clock Timing for Divide-by-1 Clock

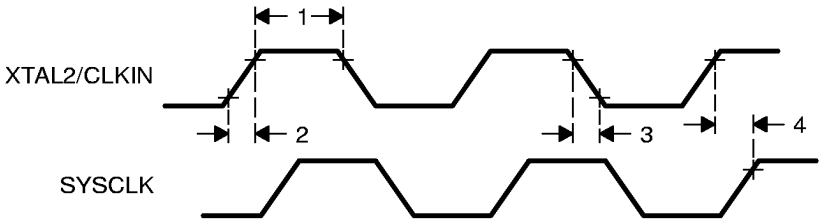
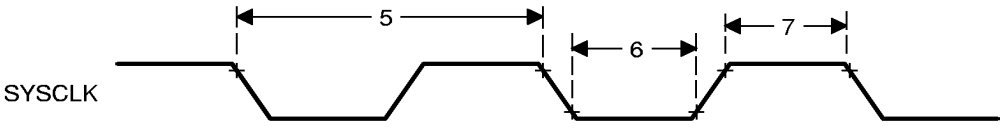


Table 18–30. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c$–20	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c$ + 20	ns

Note: t_c = system clock cycle time = 1/SYSCLK

Figure 18–20. SYSCLK Timing



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18.12 TMS370Cx4xA Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx4xA category. These devices include the TMS370C040A, TMS370C042A, TMS370C340A, TMS370C342A, TMS370C742A, and SE370C742A.

18.12.1 TMS370Cx4xA Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–31 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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Table 18–31. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{CC3}	Analog supply voltage		4.5	5	5.5	V
V_{SS3}	Analog supply ground		–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	$0.8V_{CC}$		V_{CC}	V
		$\overline{\text{RESET}}$	$0.7V_{CC}$		V_{CC}	V
V_{MC}	MC (mode control) voltage	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		Microcomputer mode	V_{SS}		0.3	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS} (ground).

2) $\overline{\text{RESET}}$ must be externally activated when V_{CC} or SYSCLK is out of the recommended operating range.

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Table 18–32. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level digital output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 6)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC}			±10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 3)		See Notes 1 and 2 SYSCLK = 5 MHz		30	45	mA
			See Notes 1 and 2 SYSCLK = 3 MHz		20	30	mA
			See Notes 1 and 2 SYSCLK = 0.5 MHz		7	11	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 4)		See Notes 1 and 2 SYSCLK = 5 MHz		10	17	mA
			See Notes 1 and 2 SYSCLK = 3 MHz		8	11	mA
			See Notes 1 and 2 SYSCLK = 0.5 MHz		2	3.5	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 5)		See Notes 1 and 2 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 1 and 2 SYSCLK = 0.5 MHz		2	3.0	mA
I_{CC}	Supply current (HALT mode)		See Note 1 XTALK2/CLKIN < 0.2 V		2	30	µA

Notes:
1) Microcontroller single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} −0.2 V.
2) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).
3) Maximum operating current = 7.6(SYSCLK) + 7 mA.
4) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0.)
5) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit = 1; valid only up to 3-MHz SYSCLK.)
6) Input current I_{PP} is a maximum of 50 mA only when an EPROM is being programmed.

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18.12.2 TMS370Cx4xA Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–33. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–31.

2) This pulse can be either a high pulse, as illustrated in Figure 18–21, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–21. External Clock Timing for Divide-by-4 Clock

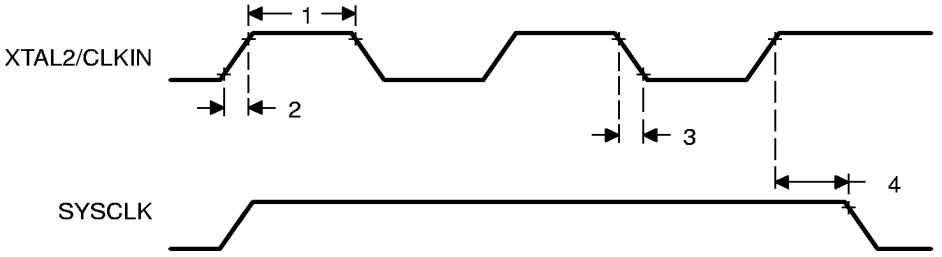

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Table 18–34. External Clocking Requirements for Divide-by-1 Clock (PLL) (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–31.

2) This pulse can be either a high pulse, as illustrated in Figure 18–22, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–22. External Clock Timing for Divide-by-1 Clock

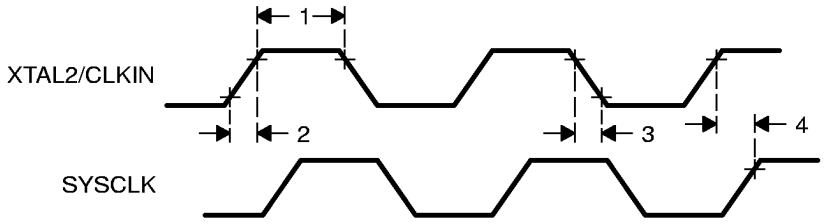
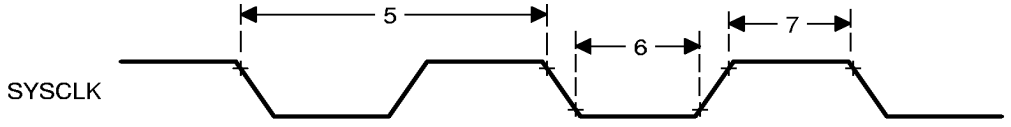


Table 18–35. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system-clock cycle time = 1/SYSCLK.

Figure 18–23. SYSCLK Timing



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18.13 TMS370Cx5xA and TMS370Cx5xB Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx5xA and TMS370Cx5xB categories. These devices include the following:

TMS370C050A	TMS370C150A	TMS370C250A	TMS370C350A
TMS370C052A	TMS370C352A	TMS370C452A	TMS370C353A
TMS370C056A	TMS370C156A	TMS370C256A	TMS370C356A
TMS370C456A	TMS370C756A	SE370C756A	TMS370C058A
TMS370C358A	TMS370C758A	TMS370C758B,	SE370C758A
SE370758B	TMS370C059A	TMS370C759A	SE370C759A

Note:

Some electrical specifications and timings differ for TMS370Cx5x devices. Refer to Appendix A.

18.13.1 TMS370Cx5xA and TMS370Cx5xB Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–36 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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Table 18–36. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC1}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{CC2}	Digital I/O supply voltage		4.5	5	5.5	V
V_{CC3}	Analog supply voltage		4.5	5	5.5	V
V_{SS2}	Digital I/O supply ground		–0.3	0	0.3	V
V_{SS3}	Analog supply ground		–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS1}		0.8	V
		MC, normal operation	V_{SS1}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC1}	V
		MC (non-WPO mode)	$V_{CC1}-0.3$		$V_{CC1}+0.3$	V
		XTAL2/CLKIN	$0.8V_{CC1}$		V_{CC1}	V
		$\overline{\text{RESET}}$	$0.7V_{CC1}$		V_{CC1}	V
V_{MC}	MC (mode control) voltage (see Note 3)	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microprocessor mode	$V_{CC1}-0.3$		$V_{CC1}+0.3$	V
		Microcomputer mode	V_{SS1}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS1}.

2) $\overline{\text{RESET}}$ must be externally activated when V_{CC1} or SYSCLK is not within the recommended operating range.

3) The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system-clock cycles ($2t_c$) before $\overline{\text{RESET}}$ goes inactive (high). The WPO mode can be selected any time a sufficient voltage is present on MC.

CAUTION

You cannot use the internal connectors between pins (e.g., the connector between V_{SS1} and V_{SS2}) for a jumper from one side of the chip to another.

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Table 18–37. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage (see Note 1)		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I < V_{CC1} − 0.3 V			50	µA
			V_{CC1} − 0.3 V ≤ V_I ≤ V_{CC1} + 0.3 V			10	µA
			V_{CC1} + 0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 2)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC1}			±10	µA
I_{OL}	Low-level output current (see Note 1)		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC1}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC1}	Supply current (operating mode) OSC POWER bit = 0 (see Note 5)	TMS370Cx50A TMS370Cx52A	See Notes 3 and 4 SYSCLK = 5 MHz		30	45	mA
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B			35	56	mA

† TMS370Cx59 operates only up to 3-MHz SYSCLK.

Notes: 1) In prior versions of the TMS370 family, I_{OL} was equal to 2 mA for ports A, B, C, and D and $\overline{\text{RESET}}$.

2) Input current Ipp is a maximum of 50 mA only when EPROM is being programmed.

3) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} − 0.2 V.

4) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).

5) Maximum operating current for TMS370Cx50A and TMS370Cx52A = 7.6(SYSCLK) + 7 mA. Maximum operating current for the 'Cx53A, 'Cx56A, 'Cx58A, and 'Cx58B = 10(SYSCLK) + 5.8 mA.

6) Maximum standby current for the 'Cx5xA and 'Cx5xB = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).

7) Maximum standby current for the 'Cx5xA and 'Cx5xB = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit = 1; valid only up to 3-MHz SYSCLK.)

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Table 18–37. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Continued)

Parameter			Test Conditions	Min	Typ	Max	Unit
I_{CC1}	Supply current (operating mode) OSC POWER bit = 0 (see Note 5)	TMS370Cx50A TMS370Cx52A	See Notes 3 and 4 SYSCLK = 3 MHz		20	30	mA
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B			25	36	mA
		TMS370Cx59A†			46	55	mA
I_{CC1}	Supply current (operating mode) OSC POWER bit = 0 (see Note 5)	TMS370Cx50A TMS370Cx52A	See Notes 3 and 4 SYSCLK = 0.5 MHz		5	11	mA
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B			13	18	mA
		TMS370Cx59A†			22	28	mA
I_{CC1}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 6)		See Notes 3 and 4 SYSCLK = 5 MHz		12	17	mA
			See Notes 3 and 4 SYSCLK = 3 MHz		8	11	mA
			See Notes 3 and 4 SYSCLK = 0.5 MHz		2.5	3.5	mA
I_{CC1}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 7)		See Notes 3 and 4 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 3 and 4 SYSCLK = 0.5 MHz		2	3	mA
I_{CC1}	Supply current (HALT mode)		See Note 3 XTAL2/CLKIN < 0.2 V		2	30	µA

† TMS370Cx59A operates only up to 3-MHz SYSCLK.

Notes: 1) I then prior versions of the TMS370 family, I_{OL} was equal to 2 mA for ports A, B, C, and D and $\overline{\text{RESET}}$.
2) Input current Ipp is a maximum of 50 mA only when EPROM is being programmed.
3) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} – 0.2 V.
4) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).
5) Maximum operating current for the 'Cx50A and 'Cx52A = 7.6(SYSCLK) + 7 mA. Maximum operating current for the 'Cx53A, 'Cx56A, 'Cx58A and 'Cx58B = 10(SYSCLK) + 5.8 mA.
6) Maximum standby current for the 'Cx5xA and 'Cx5xB = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).
7) Maximum standby current for the 'Cx5xA and 'Cx5xB = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit = 1; valid only up to 3-MHz SYSCLK.)

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18.13.2 TMS370Cx5xA and TMS370Cx5xB Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–38. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency (see Note 3)	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Notes 4 and 5)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–36.

2) This pulse can be either a high pulse, as illustrated in Figure 18–24, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) TMS370Cx59A operates up to 12-MHz CLKIN.

4) TMS370Cx59A operates up to 3-MHz SYSCLK.

5) SYSCLK = CLKIN/4

Figure 18–24. External Clock Timing for Divide-by-4 Clock

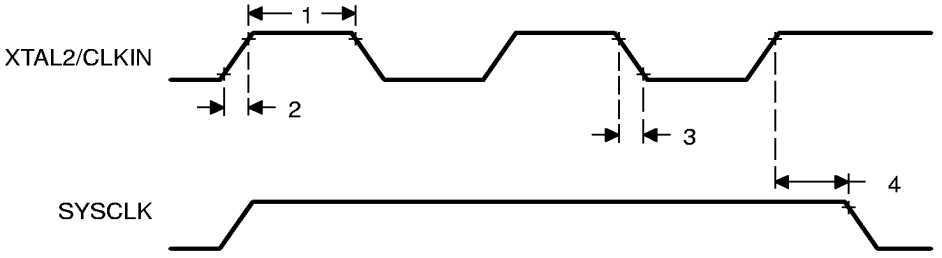

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Table 18–39. External Clocking Requirements for Divide-by-1 Clock (PLL) (see Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency (see Note 3)	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Notes 4 and 5)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–36.

2) This pulse can be either a high pulse, as illustrated in Figure 18–25, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) TMS370Cx59A operates up to 3-MHz CLKIN (for the divide-by-1 clock option).

4) TMS370Cx59A operates up to 3-MHz SYSCLK.

5) SYSCLK = CLKIN/1

Figure 18–25. External Clock Timing for Divide-by-1 Clock

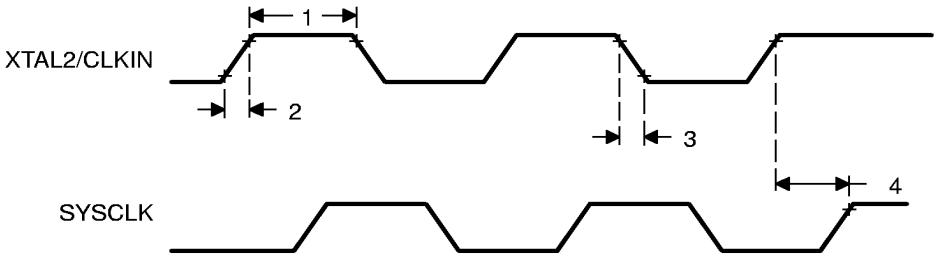

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Table 18–40. Switching Characteristics and Timing Requirements for External Read and Write (See Note 1)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock (PLL)	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 25$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns
8	$t_{d(SCL-A)}$	Delay time, SYSCLK low to address, R/$\overline{W}$, and $\overline{OCF}$ valid			$0.25t_c + 75$	ns
9	$t_{v(A)}$	Valid time, address valid to $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low		$0.5t_c - 90$		ns
10	$t_{su(D)}$	Setup time, write data to $\overline{EDS}$ high		$0.75t_c - 80$ See Note 2		ns
11	$t_{h(EH-A)}$	Hold time, address, R/$\overline{W}$, and $\overline{OCF}$ from $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ high		$0.5t_c - 60$		ns
12	$t_{h(EH-D)W}$	Hold time, write data from $\overline{EDS}$ high		$0.75t_c + 15$		ns
13	$t_{d(DZ-EL)}$	Delay time, data bus high impedance to $\overline{EDS}$ low (read cycle)		$0.25t_c - 35$		ns
14	$t_{d(EH-D)}$	Delay time, $\overline{EDS}$ high to data bus enable (read cycle)		$1.25t_c - 40$		ns
15	$t_{d(EL-DV)R}$	Delay time, $\overline{EDS}$ low to read data valid			$t_c - 95$ See Note 2	ns
16	$t_{h(EH-D)R}$	Hold time, read from $\overline{EDS}$ high		0		ns
17	$t_{su(WT-SCH)}$	Setup time, $\overline{WAIT}$ to SYSCLK high		$0.25t_c + 70$ See Note 3		ns
18	$t_{h(SCH-WT)}$	Hold time, $\overline{WAIT}$ time from SYSCLK high		0		ns
19	$t_{d(EL-WTV)}$	Delay time, $\overline{EDS}$ low to $\overline{WAIT}$ valid			$0.5t_c - 60$	ns
20	t_w	Pulse duration, $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low		$t_c - 80$ See Note 2	$t_c + 40$ See Note 2	ns
21	$t_{d(AV-DV)R}$	Delay time, address valid to read data valid			$1.5t_c - 115$ See Note 2	ns
22	$t_{d(AV-WTV)}$	Delay time, address valid to $\overline{WAIT}$ valid			$t_c - 115$	ns
23	$t_{d(AV-EH)}$	Delay time, address valid to $\overline{EDS}$ high (end of write)		$1.5t_c - 85$ See Note 2		ns

Notes: 1) t_c = system-clock cycle time = 1/SYSCLK

2) If wait states, PFWait, or the autowait feature is used, add t_c to this value for each wait state invoked.

3) If the autowait feature is enabled, the $\overline{WAIT}$ input can assume a “don’t care” condition until the third cycle of the access. The $\overline{WAIT}$ signal must be synchronized with the high pulse of the SYSCLK signal while still conforming to the minimum setup time.

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Figure 18–26. External Read Timing

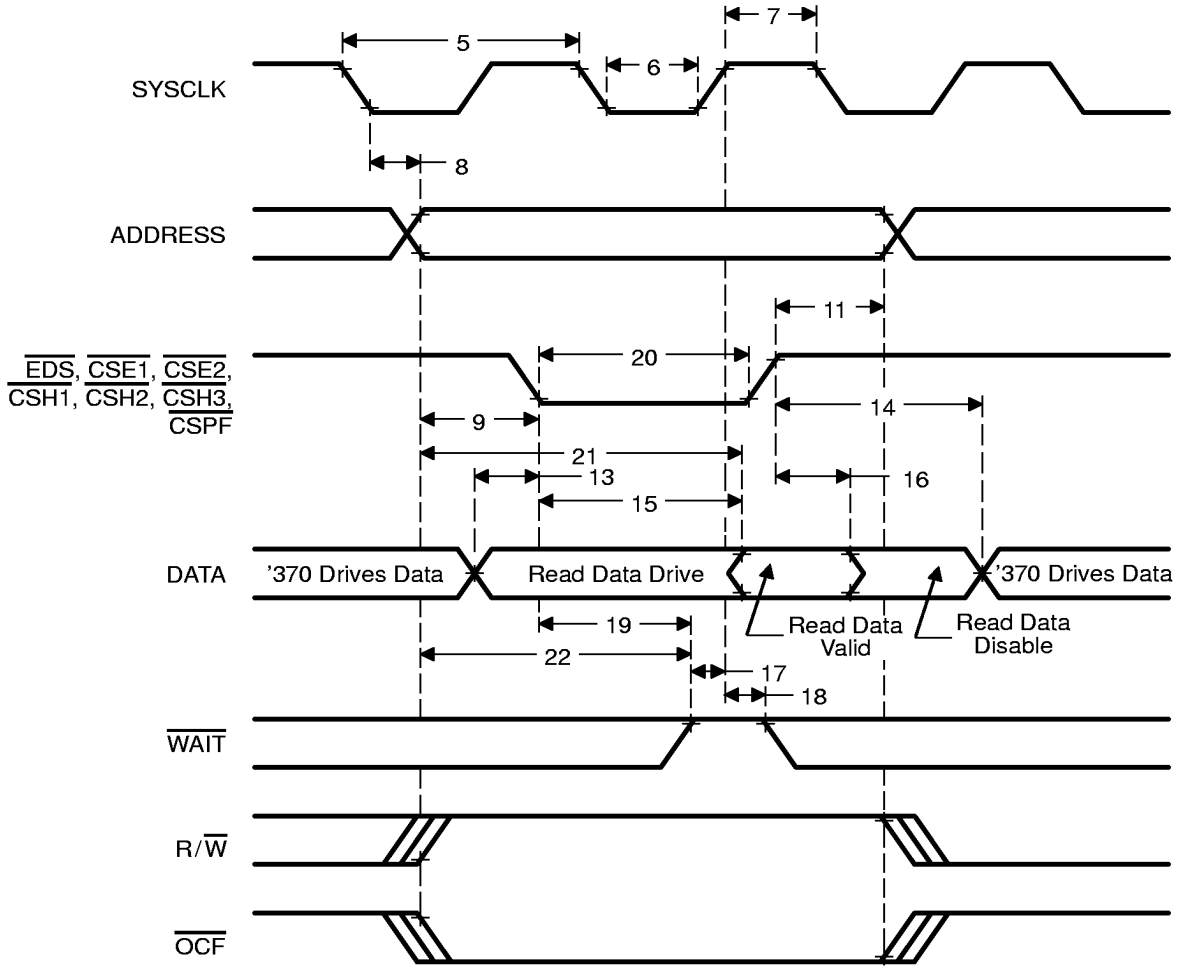

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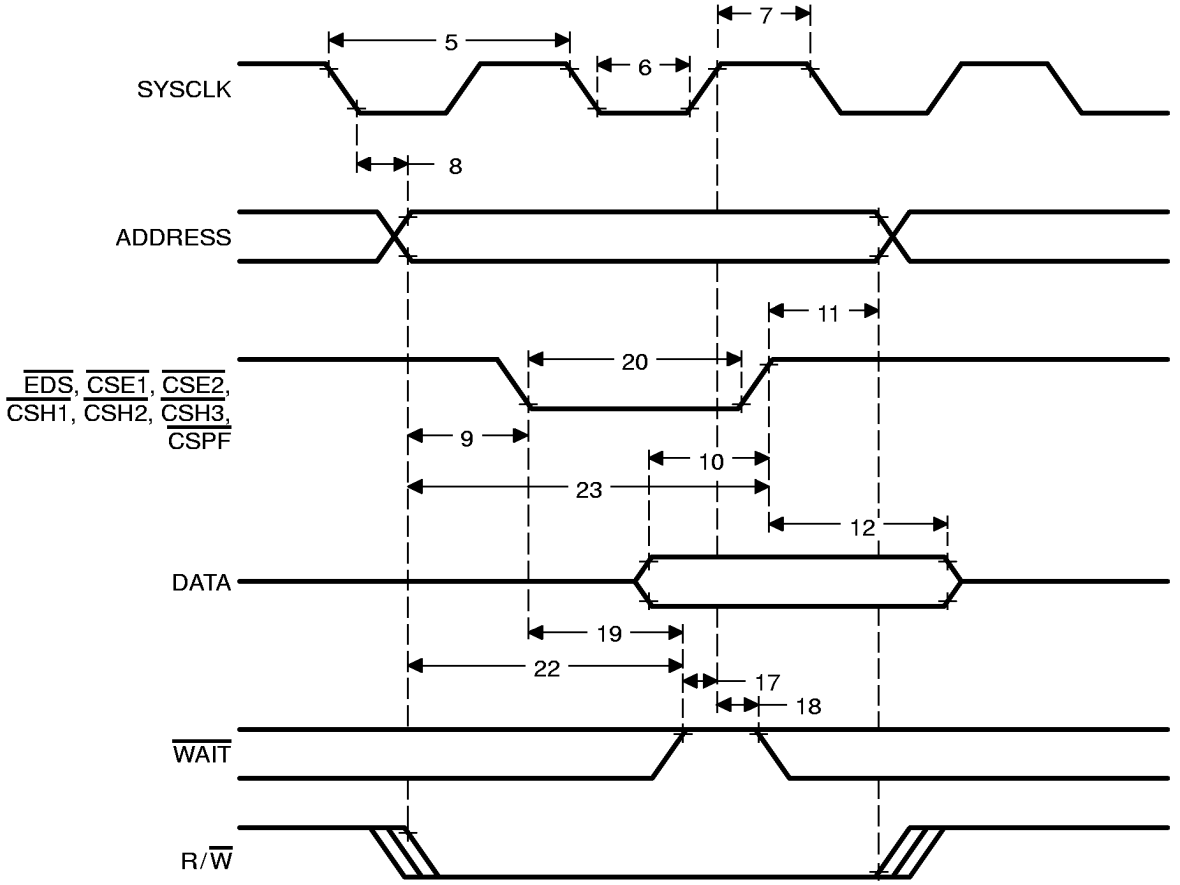
Figure 18–27. External Write Timing



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18.14 TMS370Cx6xA Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx6xA category. These devices include the TMS370C067A, TMS370C068A, TMS370C069A, TMS370C768A, TMS370C769A, SE370C768A, and SE370C769A.

18.14.1 TMS370Cx6xA Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–41 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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Table 18–41. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC1}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{CC2}	Digital I/O supply voltage		4.5	5	5.5	V
V_{CC3}	Analog supply voltage		4.5	5	5.5	V
V_{SS2}	Digital I/O supply ground		–0.3	0	0.3	V
V_{SS3}	Analog supply ground		–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS1}		0.8	V
		MC, normal operation	V_{SS1}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC1}	V
		MC (non-WPO mode)	$V_{CC1}-0.3$		$V_{CC1}+0.3$	V
		XTAL2/CLKIN	$0.8V_{CC1}$		V_{CC1}	V
		$\overline{\text{RESET}}$	$0.7V_{CC1}$		V_{CC1}	V
V_{MC}	MC (mode control) voltage (see Note 3)	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microprocessor mode	$V_{CC1}-0.3$		$V_{CC1}+0.3$	V
		Microcomputer mode	V_{SS1}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS1}.
2) $\overline{\text{RESET}}$ must be externally activated when V_{CC1} or SYSCLK is out of the recommended operating range.
3) The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system-clock cycles ($2t_c$) before $\overline{\text{RESET}}$ goes inactive (high). The WPO mode can be selected any time a sufficient voltage is present on MC.

You cannot use the internal connections between pins (for example, the connection between V_{SS1} and V_{SS2}) for a jumper from one side of the chip to the other.

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Table 18–42. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC1}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I < V_{CC1} − 0.3 V			50	µA
			V_{CC1} − 0.3 V ≤ V_I ≤ V_{CC1} + 0.3 V			10	µA
			V_{CC1} + 0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 1)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC1}			±10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC1}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC1}	Supply current (operating mode) OSC POWER bit = 0 (see Note 4)	'Cx67A, 'Cx68A	See Notes 2 and 3 SYSCLK = 5 MHz		35	56	mA
		'Cx67A, 'Cx68A	See Notes 2 and 3 SYSCLK = 3 MHz		25	36	mA
		'Cx69A†			46	55	mA
		'Cx67A, 'Cx68A	See Notes 2 and 3 SYSCLK = 0.5 MHz		13	18	mA
		'Cx69A†			22	28	mA
I_{CC1}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 5)		See Notes 2 and 3 SYSCLK = 5 MHz		12	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		8	11	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2.5	3.5	mA
I_{CC1}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 6)		See Notes 2 and 3 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3	mA
I_{CC1}	Supply current (HALT mode)		See Note 2 XTAL2/CLKIN < 0.2 V		2	30	µA

† TMS370Cx69A operates only up to 3 MHz SYSLCK.

Notes: 1) Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.
2) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} − 0.2 V.
3) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).
4) Maximum operating current = 10(SYSCLK) + 5.8 mA.
5) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).
6) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit = 1; valid only up to 3-MHz SYSCLK).

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18.14.2 TMS370Cx6xA Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–43. External Clocking Requirements for Divide-by-4 Clock (see Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency (see note 3)	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Notes 4 and 5)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions table in Table 18–41.

2) This pulse can be either a high pulse, as illustrated in Figure 18–28, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) TMS370Cx69A operates up to 12 MHz CLKIN.

4) TMS370Cx69A operates up to 3 MHz SYSCLK.

5) SYSCLK = CLKIN/4

Figure 18–28. External Clock Timing for Divide-by-4 Clock

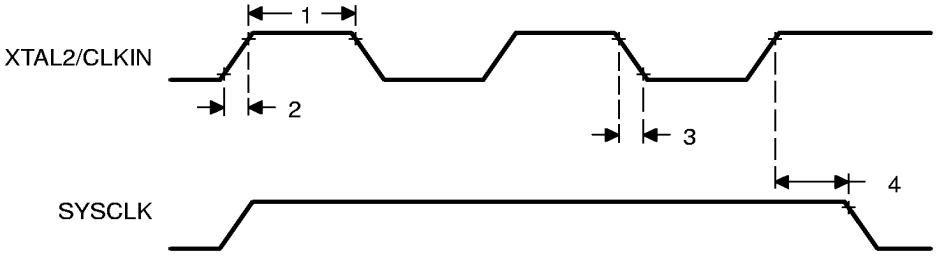

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Table 18–44. External Clocking Requirements for Divide-by-1 Clock (PLL)(See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency (see Note 3)	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Notes 4 and 5)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–41.

2) This pulse can be either a high pulse, as illustrated in Figure 18–29, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) TMS370Cx69A operates up to 3-MHz CLKIN (for the divide-by-1 clock option).

4) TMS370Cx69A operates up to 3 MHz SYSCLK.

5) SYSCLK = CLKIN/1

Figure 18–29. External Clock Timing for Divide-by-1 Clock

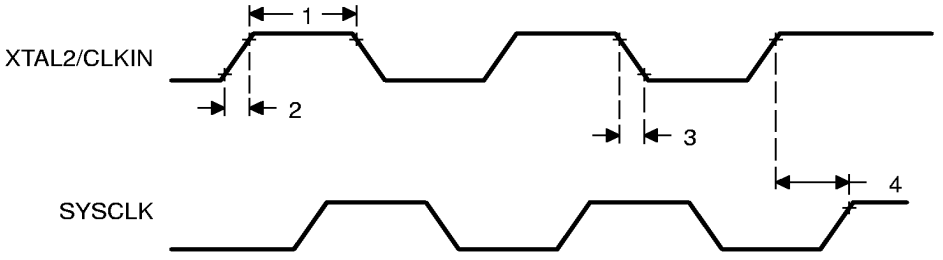

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Table 18–45. Switching Characteristics and Timing Requirements for External Read and Write (See Note 1)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock (PLL)	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 25$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns
8	$t_{d(SCL-A)}$	Delay time, SYSCLK low to address, R/$\overline{W}$, and $\overline{OCF}$ valid			$0.25t_c + 75$	ns
9	$t_{v(A)}$	Valid time, address valid to $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSH1}$, and $\overline{CSPF}$ low		$0.5t_c - 90$		ns
10	$t_{su(D)}$	Setup time, write data to $\overline{EDS}$ high		$0.75t_c - 80$ See Note 2		ns
11	$t_{h(EH-A)}$	Hold time, address, R/$\overline{W}$, and $\overline{OCF}$ from $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSH1}$, and $\overline{CSPF}$ high		$0.5t_c - 60$		ns
12	$t_{h(EH-D)W}$	Hold time, write data time from $\overline{EDS}$ high		$0.75t_c + 15$		ns
13	$t_{d(DZ-EL)}$	Delay time, data bus high impedance to $\overline{EDS}$ low (read cycle)		$0.25t_c - 35$		ns
14	$t_{d(EH-D)}$	Delay time, $\overline{EDS}$ high to data bus enable (read cycle)		$1.25t_c - 40$		ns
15	$t_{d(EL-DV)R}$	Delay time, $\overline{EDS}$ low to read data valid			$t_c - 95$ See Note 2	ns
16	$t_{h(EH-D)R}$	Hold time, read from $\overline{EDS}$ high		0		ns
17	$t_{su(WT-SCH)}$	Setup time, $\overline{WAIT}$ to SYSCLK high		$0.25t_c + 70$ See Note 3		ns
18	$t_{h(SCH-WT)}$	Hold time, $\overline{WAIT}$ from SYSCLK high		0		ns
19	$t_{d(EL-WTV)}$	Delay time, $\overline{EDS}$ low to $\overline{WAIT}$ valid			$0.5t_c - 60$	ns
20	t_w	Pulse duration, $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSH1}$, and $\overline{CSPF}$ low		$t_c - 80$ See Note 2	$t_c + 40$ See Note 2	ns
21	$t_{d(AV-DV)R}$	Delay time, address valid to read data valid			$1.5t_c - 115$ See Note 2	ns
22	$t_{d(AV-WTV)}$	Delay time, address valid to $\overline{WAIT}$ valid			$t_c - 115$	ns
23	$t_{d(AV-EH)}$	Delay time, address valid to $\overline{EDS}$ high (end of write)		$1.5t_c - 85$ See Note 2		ns

Notes: 1) t_c = system clock cycle time = 1/SYSCLK

2) If wait states, PFWait, or the autowait feature is used, add t_c to this value for each wait state invoked.

3) If the autowait feature is enabled, the $\overline{WAIT}$ input can assume a “don’t care” condition until the third cycle of the access. The $\overline{WAIT}$ signal must be synchronized with the high pulse of the SYSCLK signal while still conforming to the minimum setup time.

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Figure 18–30. External Read Timing

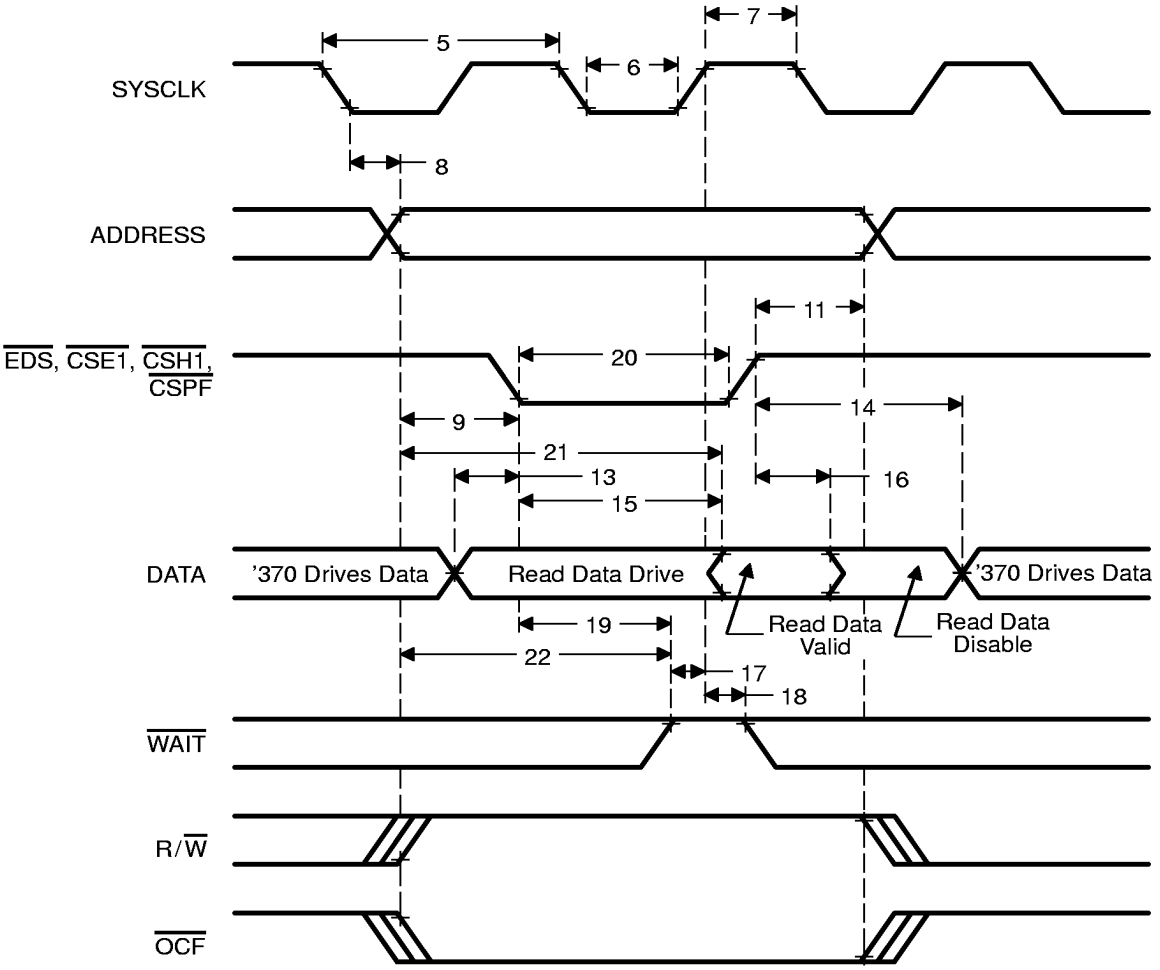

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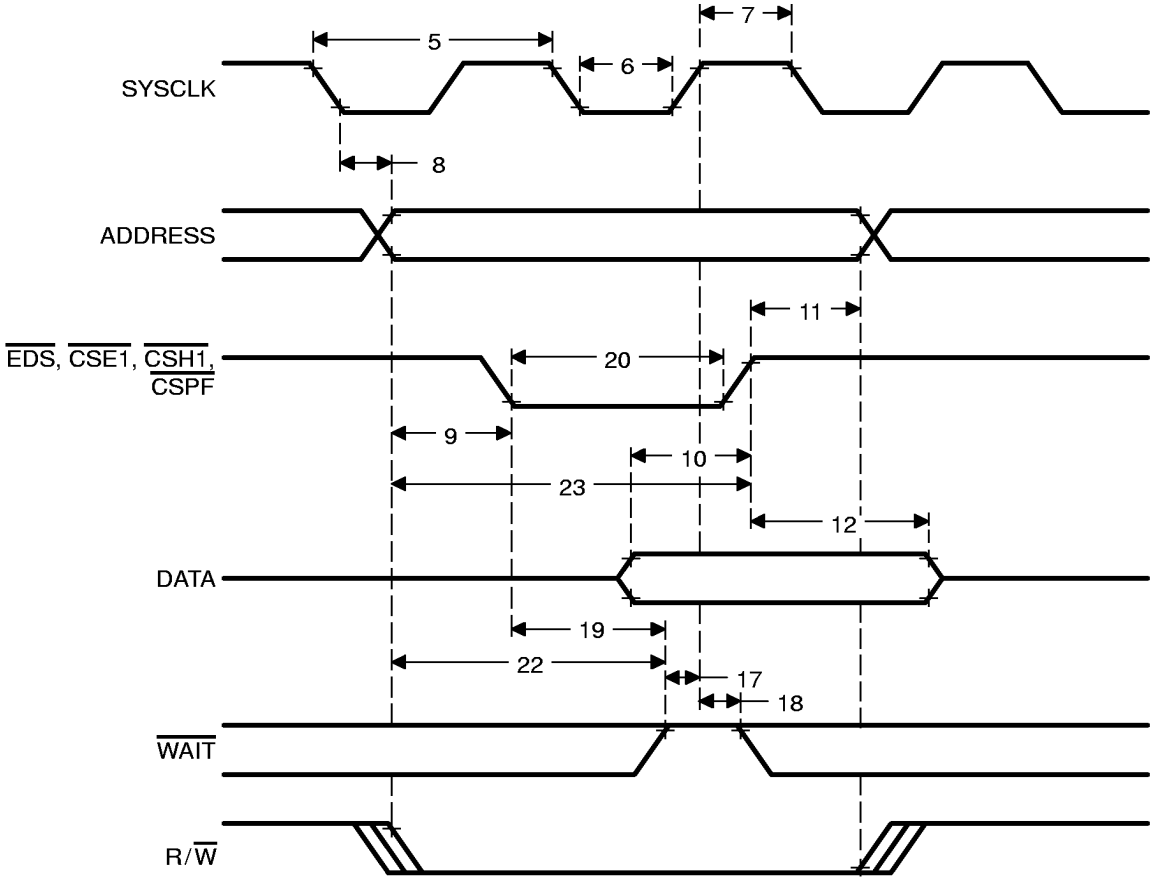
Figure 18–31. External Write Timing



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18.15 TMS370Cx7xA Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx7xA category. These devices include the TMS370C077A, TMS370C777A, and SE370C777A.

18.15.1 TMS370Cx7xA Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–46 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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Table 18–46. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC1}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{CC2}	Digital I/O supply voltage		4.5	5	5.5	V
V_{CC3}	Analog supply voltage		4.5	5	5.5	V
V_{SS2}	Digital I/O supply ground		–0.3	0	0.3	V
V_{SS3}	Analog supply ground		–0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS1}		0.8	V
		MC, normal operation	V_{SS1}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC1}	V
		MC (non-WPO mode)	$V_{CC1}-0.3$		$V_{CC1}+0.3$	V
		XTAL2/CLKIN	$0.8V_{CC1}$		V_{CC1}	V
		$\overline{\text{RESET}}$	$0.7V_{CC1}$		V_{CC1}	V
V_{MC}	MC (mode control) voltage (see Note 3)	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microprocessor mode	$V_{CC1}-0.3$		$V_{CC1}+0.3$	V
		Microcomputer mode	V_{SS1}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS1}.
2) $\overline{\text{RESET}}$ must be activated externally when V_{CC1} or SYSCLK is out of the recommended operating range.
3) The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system clock cycles ($2t_c$) before $\overline{\text{RESET}}$ goes inactive (high). The WPO mode can be selected any time a sufficient voltage is present on MC.

You cannot use the internal connections between pins (for example, the connection between V_{SS1} and V_{SS2}) for a jumper from one side of the chip to the other.

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Table 18–47. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC1}$			V
			I_{OH} = −2 mA	2.4			
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I < V_{CC1} − 0.3 V			50	
			V_{CC1} − 0.3 V ≤ V_I ≤ V_{CC1} + 0.3 V			10	
			V_{CC1} + 0.3 V < V_I ≤ 13 V			650	
			12 V ≤ V_I ≤ 13 V (see Note 1)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC1}			±10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC1}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 4)		See Notes 2 and 3 SYSCLK = 5 MHz		35	56	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		25	36	
			See Notes 2 and 3 SYSCLK = 0.5 MHz		13	18	
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 5)		See Notes 2 and 3 SYSCLK = 5 MHz		12	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		8	11	
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2.5	3.5	
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 6)		See Notes 2 and 3 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3	
I_{CC}	Supply current (HALT mode)		See Note 2 XTAL2/CLKIN < 0.2 V		2	30	µA

Notes: 1) Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.
2) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} − 0.2 V.
3) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).
4) Maximum operating current = 10(SYSCLK) + 5.8 mA.
5) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).
6) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit =1; valid only up to 3-MHz SYSCLK).

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18.15.2 TMS370Cx7xA Timings

Refer to Sections18.1 and 18.2 (page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–48. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–46.

2) This pulse can be either a high pulse, as illustrated in Figure 18–32, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–32. External Clock Timing for Divide-by-4 Clock

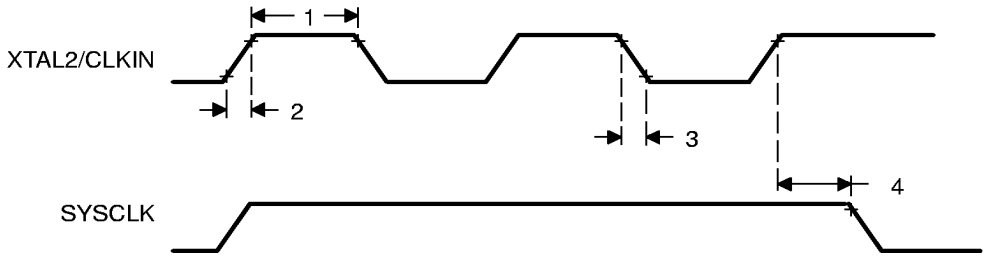

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Table 18–49. External Clocking Requirements for Divide-by-1 Clock (PLL)(see Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–46.

2) This pulse can be either a high pulse, as illustrated in Figure 18–33, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–33. External Clock Timing for Divide-by-1 Clock

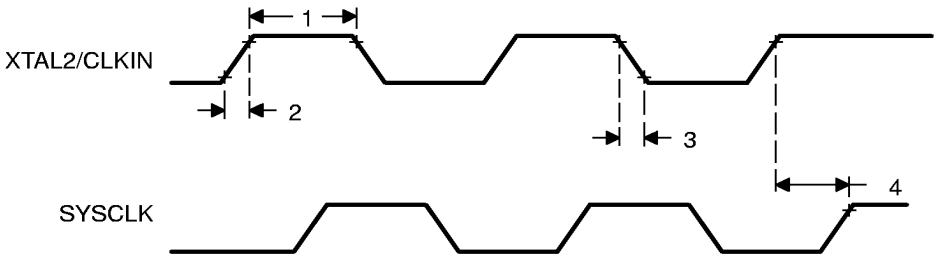

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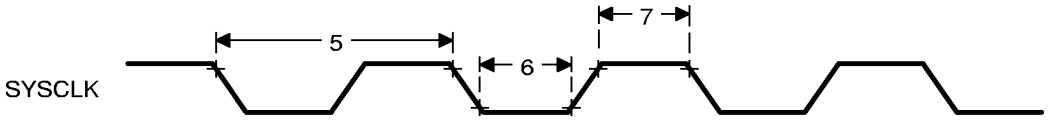
Table 18–50. Switching Characteristics and TIming Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock (PLL)	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 25$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system clock cycle time = 1/SYSCLK

Figure 18–34. SYSCLK Timing



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18.16 TMS370Cx8xA Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx8xA category. These devices include the TMS370C080A, TMS370C380A, TMS370C686A, and SE370C686A.

18.16.1 TMS370Cx8xA Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–51 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 18–51. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	$0.8V_{CC}$		V_{CC}	V
		$\overline{\text{RESET}}$	$0.7V_{CC}$		V_{CC}	V
V_{MC}	MC (mode control) voltage	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microcomputer mode	V_{SS}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS} (ground).
2) $\overline{\text{RESET}}$ must be externally activated when V_{CC} or SYSCLK is not within the recommended operating range.

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Table 18–52. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 1)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC}			± 10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 4)		See Notes 2 and 3 SYSCLK = 5 MHz		30	45	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		20	30	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		7	11	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 5)		See Notes 2 and 3 SYSCLK = 5 MHz		10	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		8	11	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.5	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 6)		See Notes 2 and 3 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.0	mA
I_{CC}	Supply current (HALT mode)		See Note 2 XTAL2/CLKIN < 0.2 V		2	30	µA

Notes: 1) Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.

2) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2 V.

3) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).

4) Maximum operating current = 7.6(SYSCLK) + 7 mA.

5) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).

6) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit = 1; valid only up to 3-MHz SYSCLK).

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18.16.2 TMS370Cx8xA Timings

Refer to Section 18.1 and Section 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–53. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–51.

2) This pulse may be either a high pulse, as illustrated in Figure 18–35, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–35. External Clock Timing for Divide-by-4 Clock

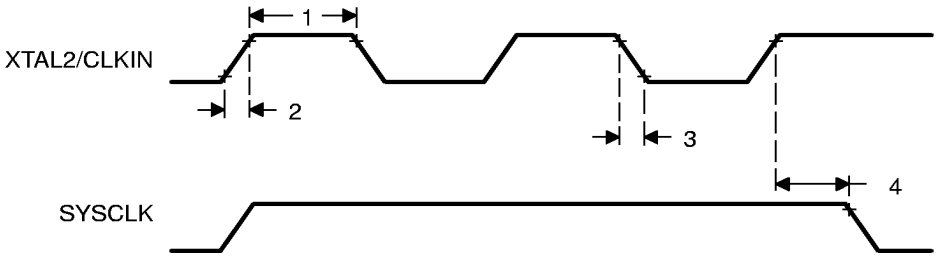

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Table 18–54. External Clocking Requirements for Divide-by-1 Clock (PLL) (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–51.

2) This pulse can be either a high pulse, as illustrated in Figure 18–36, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–36. External Clock Timing for Divide-by-1 Clock

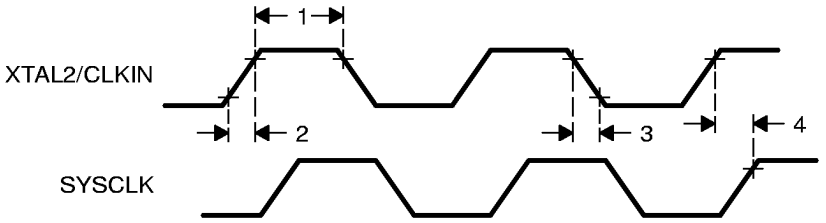

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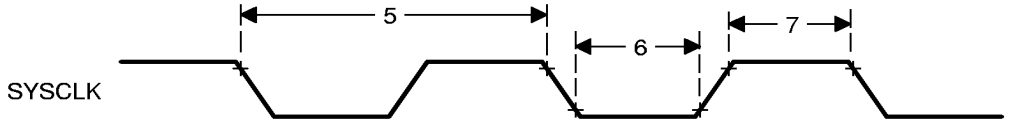
Table 18–55. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system-clock cycle time = 1/SYSCLK

Figure 18–37. SYSCLK Timing



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18.17 TMS370Cx9xA Specifications

The tables in this section give specifications that apply to the devices in the TMS370Cx9xA category. These devices include the TMS370C090A, TMS370C792A, and SE370C792A.

18.17.1 TMS370Cx9xA Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–56 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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Table 18–56. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{CC3}	Analog supply voltage		3		5.5	V
V_{SS3}	Analog supply ground		– 0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	$0.8V_{CC}$		V_{CC}	V
		$\overline{\text{RESET}}$	$0.7V_{CC}$		V_{CC}	V
V_{MC}	MC (mode control) voltage	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microcomputer mode	V_{SS}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS} (ground).

2) $\overline{\text{RESET}}$ must be externally activated when V_{CC} or SYSCLK is out of the recommended operating range.

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Table 18–57. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 1)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC}			±10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 4)		See Notes 2 and 3 SYSCLK = 5 MHz		30	45	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		20	30	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		7	11	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 5)		See Notes 2 and 3 SYSCLK = 5 MHz		10	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		8	11	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.5	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 6)		See Notes 2 and 3 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3	mA
I_{CC}	Supply current (HALT mode)		See Note 2 XTAL2/CLKIN < 0.2 V		2	30	µA

Notes: 1) Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.
2) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2 V.
3) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).
4) Maximum operating current = 7.6(SYSCLK) + 7 mA.
5) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).
6) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit =1; valid only up to 3-MHz SYSCLK).

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18.17.2 TMS370Cx9xA Timings

Refer to Section 18.1 and Section 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–58. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–56.

2) This pulse can be either a high pulse, as illustrated in Figure 18–38, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–38. External Clock Timing for Divide-by-4 Clock

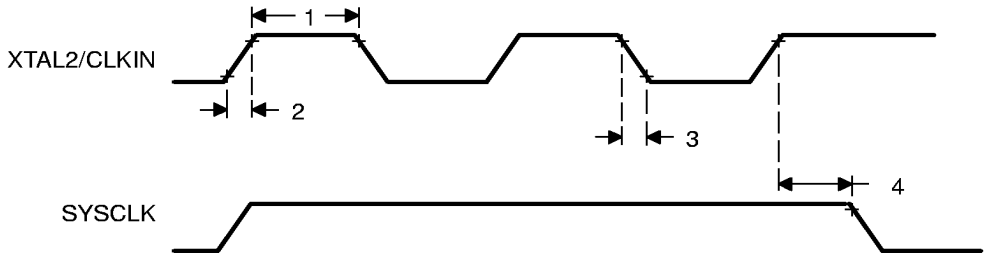

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Table 18–59. External Clocking Requirements for Divide-by-1 Clock (PLL) (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–56.

2) This pulse can be either a high pulse, as illustrated in Figure 18–39, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–39. External Clock Timing for Divide-by-1 Clock

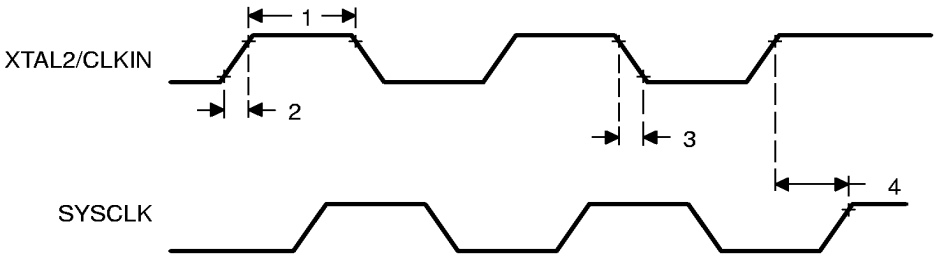

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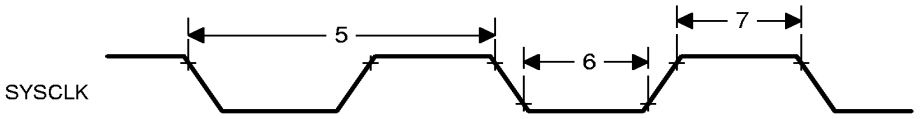
Table 18–60. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock (PLL)	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system-clock cycle time = 1/SYSCLK

Figure 18–40. SYSCLK Timing



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18.18 TMS370CxAxA Specifications

The tables in this section give specifications that apply to the devices in the TMS370CxAxA category. These devices include the TMS370C3A7A.

18.18.1 TMS370CxAxA Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–61 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 18–61. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	$0.8V_{CC}$		V_{CC}	V
		$\overline{\text{RESET}}$	$0.7V_{CC}$		V_{CC}	V
V_{MC}	MC (mode control) voltage	Microcomputer mode	V_{SS}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS} (ground).
2) $\overline{\text{RESET}}$ must be activated externally when V_{CC} or SYSCLK is out of the recommended operating range.

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Table 18–62. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	µA
		I/O pins	0 V ≤ V_I ≤ V_{CC}			±10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 3)		See Notes 2 and 3 SYSCLK = 5 MHz		30	45	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		20	30	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		7	11	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 4)		See Notes 2 and 3 SYSCLK = 5 MHz		10	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		8	11	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.5	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 5)		See Notes 2 and 3 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.0	mA
I_{CC}	Supply current (HALT mode)		See Note 1 XTAL2/CLKIN < 0.2 V		2	30	µA

Notes: 1) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2 V.
2) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).
3) Maximum operating current = 7.6(SYSCLK) + 7 mA.
4) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).
5) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit = 1; valid only up to 3-MHz SYSCLK).

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18.18.2 TMS370CxAxA Timings

Refer to Section 18.1 and Section 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement points.

Table 18–63. External Clocking Requirements for Divide-by-4 Clock (see Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–61.

2) This pulse can be either a high pulse, as illustrated in Figure 18–41, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–41. External Clock Timing for Divide-by-4 Clock

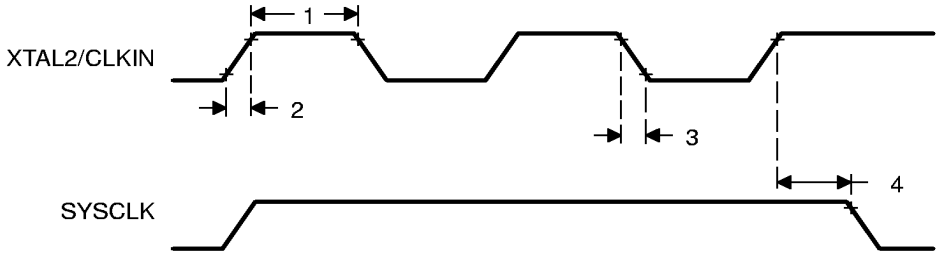

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Table 18–64. External Clocking Requirements for Divide-by-1 Clock (PLL) (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–61.

2) This pulse can be either a high pulse, as illustrated in Figure 18–42, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–42. External Clock Timing for Divide-by-1 Clock

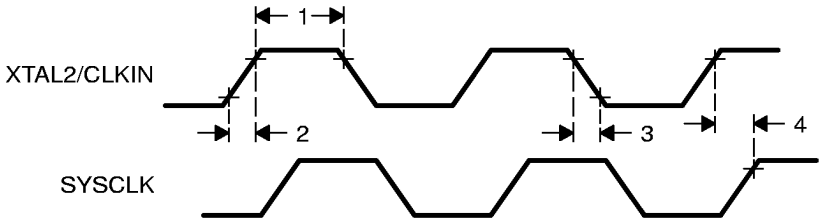

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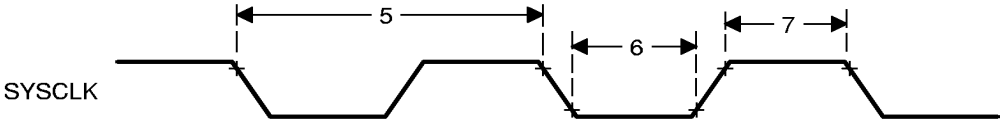
Table 18–65. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock (PLL)	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system-clock cycle time = 1/SYSCLK

Figure 18–43. SYSCLK Timing



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18.19 TMS370CxBxA Specifications

The tables in this section give specifications that apply to the devices in the TMS370CxBxA category. These devices include the TMS370C0B6A.

18.19.1 TMS370CxBxA Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–66 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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Table 18–66. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC1}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{CC2}	Digital I/O supply voltage		4.5	5	5.5	V
V_{CC3}	Analog supply voltage		4.5	5	5.5	V
V_{SS2}	Digital I/O supply ground		– 0.3	0	0.3	V
V_{SS3}	Analog supply ground		– 0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS1}		0.8	V
		MC, normal operation	V_{SS1}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC1}	V
		MC (non-WPO mode)	V_{CC1} – 0.3		V_{CC1} + 0.3	V
		XTAL2/CLKIN	$0.8V_{CC1}$		V_{CC1}	V
		$\overline{\text{RESET}}$	$0.7V_{CC1}$		V_{CC1}	V
V_{MC}	MC (mode control) voltage (see Note 3)	EEPROM write-protect override (WPO) mode	11.7	12	13	V
		Microprocessor mode	V_{CC1} – 0.3		V_{CC1} + 0.3	V
		Microcomputer mode	V_{SS1}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS1}.
2) $\overline{\text{RESET}}$ must be externally activated when V_{CC1} or SYSCLK is out of the recommended operating range.
3) The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system clock cycles ($2t_c$) before $\overline{\text{RESET}}$ goes inactive (high). The WPO mode can be selected any time a sufficient voltage is present on MC.

You cannot use the internal connections between pins (for example, the connection between V_{SS1} and V_{SS2}) for a jumper from one side of the chip to the other.

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Table 18–67. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC1}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I < V_{CC1} − 0.3 V			50	µA
			V_{CC1} − 0.3 V ≤ V_I ≤ V_{CC1} + 0.3 V			10	µA
			V_{CC1} + 0.3 V < V_I ≤ 13 V			650	µA
		I/O pins	0 V ≤ V_I ≤ V_{CC1}			± 10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC1}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode), OSC POWER bit = 0 (see Note 3)		See Notes 1 and 2 SYSCLK = 5 MHz		35	56	mA
			See Notes 1 and 2 SYSCLK = 3 MHz		25	36	mA
			See Notes 1 and 2 SYSCLK = 0.5 MHz		13	18	mA
I_{CC}	Supply current (STANDBY mode), OSC POWER bit = 0 (see Note 4)		See Notes 1 and 2 SYSCLK = 5 MHz		12	17	mA
			See Notes 1 and 2 SYSCLK = 3 MHz		8	11	mA
			See Notes 1 and 2 SYSCLK = 0.5 MHz		2.5	3.5	mA
I_{CC}	Supply current (STANDBY mode), OSC POWER bit = 1 (see Note 5)		See Notes 1 and 2 SYSCLK = 3 MHz		6	8.6	mA
			See Notes 1 and 2 SYSCLK = 0.5 MHz		2	3	mA
I_{CC}	Supply current (HALT mode)		See Note 1 XTAL2/CLKIN < 0.2 V		2	30	µA

Notes: 1) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} − 0.2 V.

2) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).

3) Maximum operating current = 10(SYSCLK) + 5.8 mA.

4) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).

5) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit =1; valid only up to 3-MHz SYSCLK).

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18.19.2 TMS370CxBxA Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2) for timing symbol definitions and parameter measurement information.

Table 18–68. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(ClH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–66.

2) This pulse can be either a high pulse, as illustrated in Figure 18–44, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–44. External Clock Timing for Divide-by-4 Clock

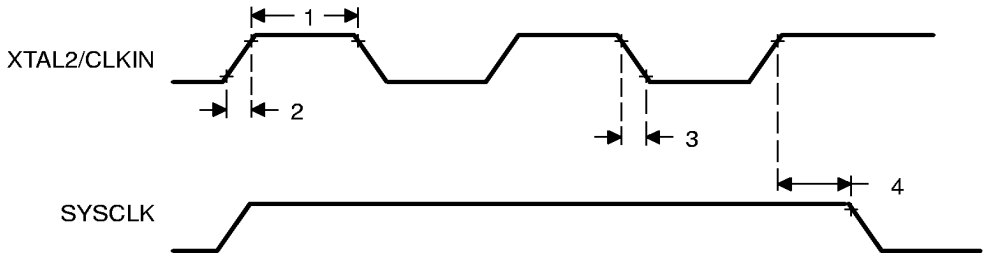

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Table 18–69. External Clocking Requirements for Divide-by-1 Clock (PLL) (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–66.

2) This pulse can be either a high pulse, as illustrated in Figure 18–45, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–45. External Clock Timing for Divide-by-1 Clock

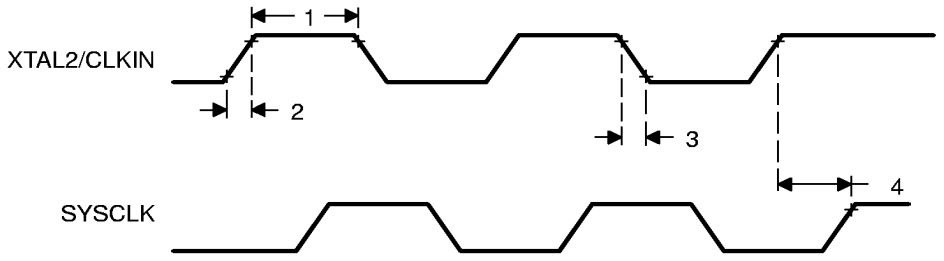

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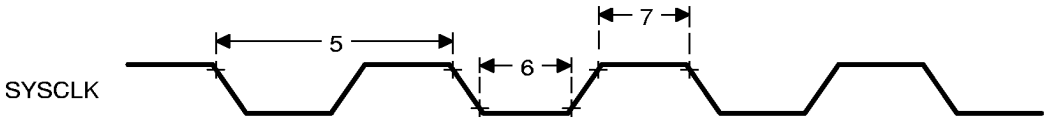
Table 18–70. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock (PLL)	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 25$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system clock cycle time = 1/SYSCLK

Figure 18–46. SYSCLK Timing



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18.20 TMS370CxCxA Specifications

The tables in this section give specifications that apply to the devices in the TMS370CxCxA category. These devices include the TMS370C3C0A, TMS370C6C2A and SE370C6C2A.

18.20.1 TMS370CxCxA Electrical Specifications

Stresses beyond those listed in Table 18–1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions in Table 18–71 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 18–71. Recommended Operating Conditions (See Note 1)

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	$0.8V_{CC}$		V_{CC}	V
		$\overline{\text{RESET}}$	$0.7V_{CC}$		V_{CC}	V
V_{MC}	MC (mode control) voltage	EPROM programming voltage (V_{PP})	13	13.2	13.5	V
		Microcomputer mode	V_{SS}		0.3	V
T_A	Operating free-air temperature	L version	0		70	°C
		A version	–40		85	°C
		T version	–40		105	°C

Notes: 1) Unless otherwise noted, all voltage values are with respect to V_{SS} (ground).

2) $\overline{\text{RESET}}$ must be activated externally when V_{CC} or SYSCLK is out of the recommended operating range.

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Table 18–72. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter			Test Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = −50 µA	$0.9V_{CC}$			V
			I_{OH} = −2 mA	2.4			V
I_I	Input current	MC	0 V ≤ V_I ≤ 0.3 V			10	µA
			0.3 V < V_I ≤ 13 V			650	µA
			12 V ≤ V_I ≤ 13 V (see Note 1)			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC}			± 10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = $0.9V_{CC}$	–50			µA
			V_{OH} = 2.4 V	–2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 4)		See Notes 2 and 3 SYSCLK = 5 MHz		20	36	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		13	25	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		5	11	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 5)		See Notes 2 and 3 SYSCLK = 5 MHz		10	17	mA
			See Notes 2 and 3 SYSCLK = 3 MHz		6.5	11	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		2	3.5	mA
I_{CC}	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 6)		See Notes 2 and 3 SYSCLK = 3 MHz		4.5	8.6	mA
			See Notes 2 and 3 SYSCLK = 0.5 MHz		1.5	3.0	mA
I_{CC}	Supply current (HALT mode)		See Note 2 XTAL2/CLKIN < 0.2 V		1	30	µA

Notes: 1) Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.

2) Single-chip mode, ports configured as inputs or as outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2 V.

3) XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).

4) Maximum operating current = 5.6(SYSCLK) + 8 mA.

5) Maximum standby current = 3(SYSCLK) + 2 mA (OSC POWER bit = 0).

6) Maximum standby current = 2.24(SYSCLK) + 1.9 mA (OSC POWER bit = 1; valid only up to 3-MHz SYSCLK).

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18.20.2 TMS370CxCxA Timings

Refer to Sections 18.1 and 18.2 (both on page 18-2)) for timing symbol definitions and parameter measurement points.

Table 18–73. External Clocking Requirements for Divide-by-4 Clock (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	0.5	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–71.

2) This pulse can be either a high pulse, as illustrated in Figure 18–47, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/4

Figure 18–47. External Clock Timing for Divide-by-4 Clock

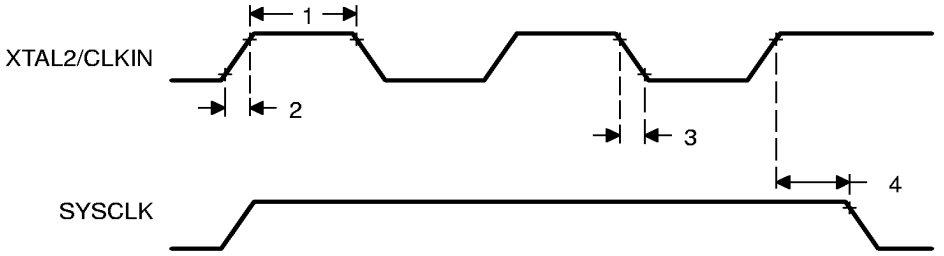

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Table 18–74. External Clocking Requirements for Divide-by-1 Clock (PLL) (See Note 1)

No.	Parameter		Min	Max	Unit
1	$t_{w(CI)}$	Pulse duration, XTAL2/CLKIN (see Note 2)	20		ns
2	$t_{r(CI)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(CI)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	Internal system clock operating frequency (see Note 3)	2	5	MHz

Notes: 1) For V_{IL} and V_{IH}, refer to recommended operating conditions in Table 18–71.

2) This pulse can be either a high pulse, as illustrated in Figure 18–48, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

3) SYSCLK = CLKIN/1

Figure 18–48. External Clock Timing for Divide-by-1 Clock

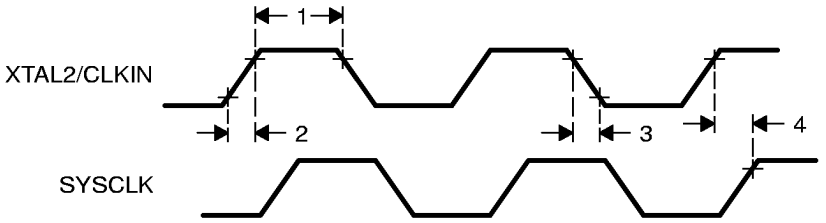

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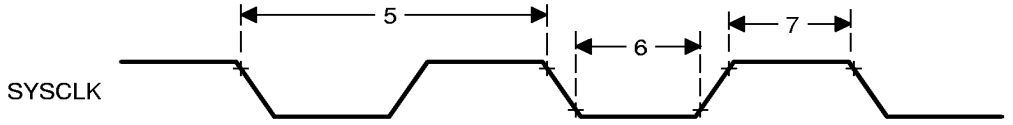
Table 18–75. Switching Characteristics and Timing Requirements (See Note)

No.	Parameter			Min	Max	Unit
5	t_c	Cycle time, SYSCLK	Divide-by-4 clock	200	2000	ns
			Divide-by-1 clock (PLL)	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c - 20$	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c + 20$	ns

Note: t_c = system clock cycle time = 1 / SYSCLK

Figure 18–49. SYSCLK Timing



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18.21 SCI Timings

This section contains timing tables and figures for devices that have the serial communications interface (SCI) module.

Note: Parameter Difference

The $t_{d(SCCL–TXDV)}$ parameter differs for TMS370Cxxx devices. Refer to subsection A.9.2 on page A-9.

Table 18–76. SCI Isosynchronous Mode Timing Characteristics and Requirements for Internal Clock (See Note)

No.	Parameter		Min	Max	Unit
24	$t_{c(SCC)}$	Cycle time, SCICLK	$2t_c$	$131\,072t_c$	ns
25	$t_{w(SCCL)}$	Pulse duration, SCICLK low	$t_c - 45$	$0.5t_{c(SCC)} + 45$	ns
26	$t_{w(SCCH)}$	Pulse duration, SCICLK high	$t_c - 45$	$0.5t_{c(SCC)} + 45$	ns
27	$t_{d(SCCL-TXDV)}$	Delay time, SCITXD valid after SCICLK low	–50	60	ns
28	$t_{v(SCCH-TXD)}$	Valid time, SCITXD data valid after SCICLK high	$t_{w(SCCH)} - 50$		ns
29	$t_{su(RXD-SCCH)}$	Setup time, SCIRXD to SCICLK high	$0.25\ t_c + 145$		ns
30	$t_{v(SCCH-RXD)}$	Valid time, SCIRXD data valid after SCICLK high	0		ns

Note: t_c = system clock cycle time = 1/SYSCLK

Figure 18–50. SCI Isosynchronous Mode Timing for Internal Clock

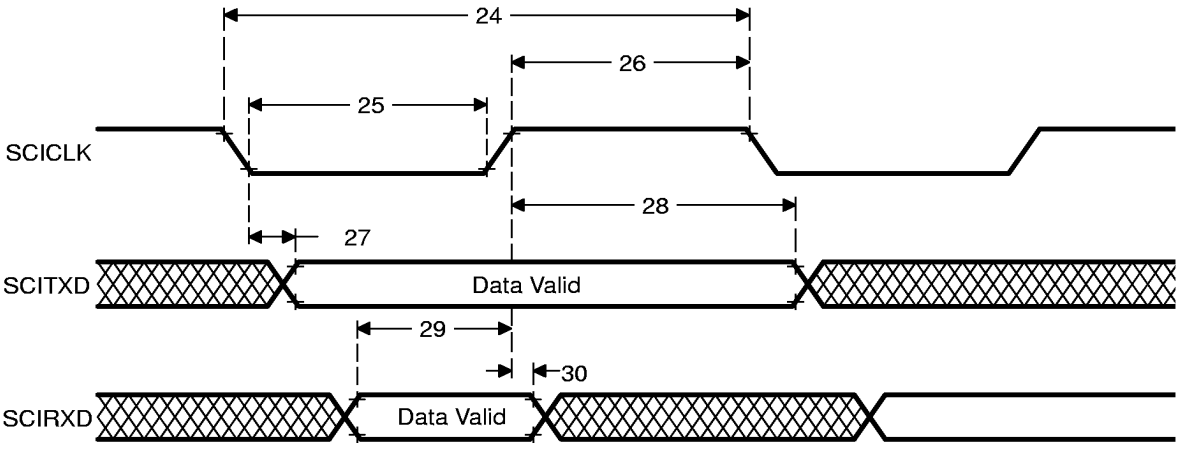

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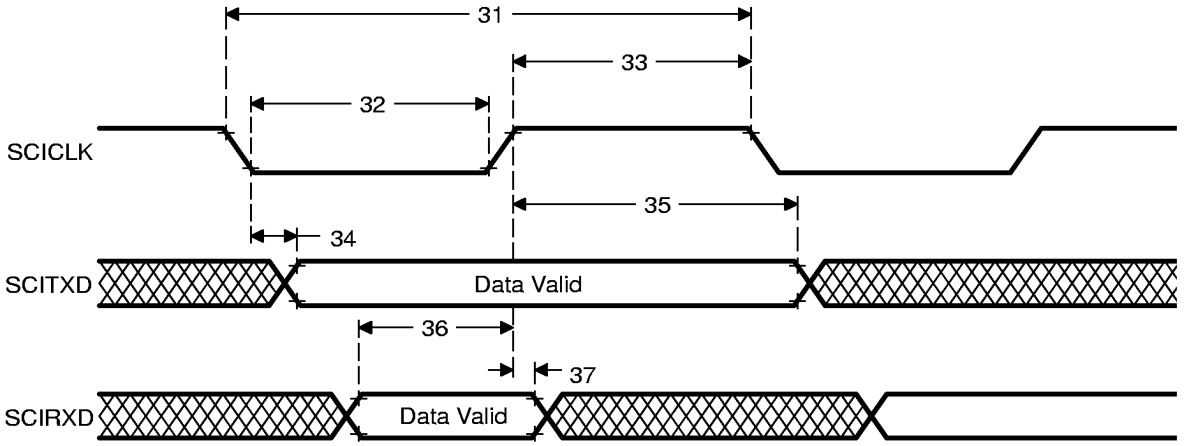
Table 18–77. SCI Isosynchronous Mode Timing Characteristics and Requirements for External Clock (See Note)

No.	Parameter		Min	Max	Unit
31	$t_{c(SCC)}$	Cycle time, SCICLK	$10t_c$		ns
32	$t_{w(SCCL)}$	Pulse duration, SCICLK low	$4.25t_c + 120$		ns
33	$t_{w(SCCH)}$	Pulse duration, SCICLK high	$t_c + 120$		ns
34	$t_{d(SCCL-TXDV)}$	Delay time, SCITXD valid after SCICLK low		$4.25t_c + 145$	ns
35	$t_{v(SCCH-TXD)}$	Valid time, SCITXD data valid after SCICLK high	$t_{w(SCCH)}$		ns
36	$t_{su(RXD-SCCH)}$	Setup time, SCIRXD to SCICLK high	40		ns
37	$t_{v(SCCH-RXD)}$	Valid time, SCIRXD data after SCICLK high	$2t_C$		ns

Note: t_c = system clock cycle time = 1/SYSCLK

Figure 18–51. SCI Isosynchronous Mode Timing for External Clock



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18.22 SPI Timings

This section contains timing tables and diagrams for the devices that have the serial peripheral interface (SPI) module in the following categories: TMS370Cx1x, TMS370Cx2x, TMS370Cx36, TMS370Cx5x, and TMS370Cx6x.

Note: Electrical/Timing Specification Differences

Some SPI electrical specifications and timings differ for TMS370Cxxx devices. Refer to subsection A.9.2 on page A-9.

Table 18–78. SPI Master Mode External Timing Characteristics and Requirements (See Note)

No.	Parameter		Min	Max	Unit
38	$t_{c(SPC)M}$	Cycle time, SPICLK	$2t_c$	$256t_c$	ns
39	$t_{w(SPCL)M}$	Pulse duration, SPICLK low	$t_c - 45$	$0.5t_{c(SPC)} + 45$	ns
40	$t_{w(SPCH)M}$	Pulse duration, SPICLK high	$t_c - 55$	$0.5t_{c(SPC)} + 45$	ns
41	$t_{d(SPCL-SIMOV)M}$	Delay time, SPISIMO valid after SPICLK low (polarity = 1)	– 65	50	ns
42	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO after SPICLK high (polarity =1)	$t_{w(SPCH)} - 50$		ns
43	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI to SPICLK high (polarity = 1)	$0.25\ t_c + 150$		ns
44	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI after SPICLK high (polarity = 1)	0		ns

Note: t_c = system clock cycle time = 1/SYSCLK

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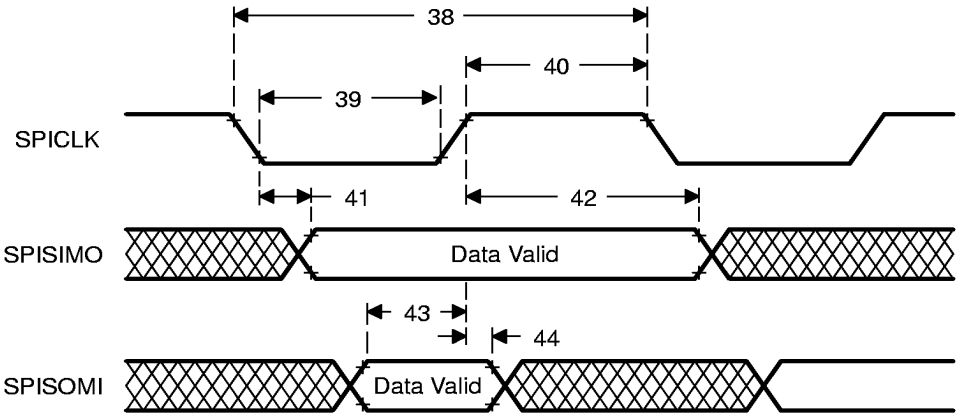
Figure 18–52. SPI Master Mode External Clock Timing



Note: In this figure, polarity = 1. SPICLK is inverted when polarity = 0.

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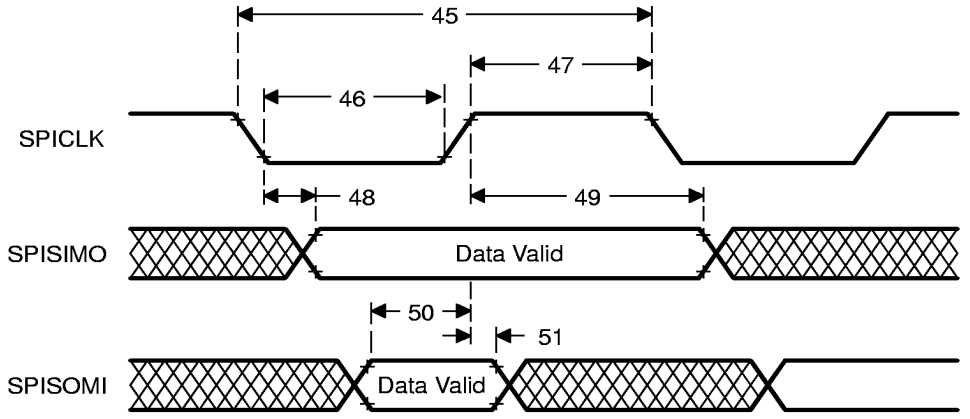
Table 18–79. SPI Slave Mode External Timing Characteristics and Requirements (See Note)

No.			Min	Max	Unit
45	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_c$		ns
46	$t_{w(SPCL)S}$	Pulse duration, SPICLK low	$4t_c - 45$	$0.5t_{c(SPC)S} + 45$	ns
47	$t_{w(SPCH)S}$	Pulse duration, SPICLK high	$4t_c - 45$	$0.5t_{c(SPC)S} + 45$	ns
48	$t_{d(SPCL-SOMIV)S}$	Delay time, SPISOMI valid after SPICLK low (polarity = 1)		$3.25t_c + 130$	ns
49	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI after SPICLK high (polarity =1)	$t_{w(SPCH)S}$		ns
50	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO to SPICLK high (polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO after SPICLK high (polarity = 1)	$3t_c + 100$		ns

Note: t_c = system clock cycle time = 1/SYSCLK

Figure 18–53. SPI Mode Slave External Timing



Notes: 1) In this figure, polarity = 1. SPICLK is inverted when polarity = 0.
2) As a slave, the SPICLK pin is used as the input for the serial clock, which is supplied from the network master.

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18.23 Analog-to-Digital Converter 1 (ADC1) Module Specifications

This section contains specifications for the devices that have the analog-to-digital converter 1 (ADC1) module in the following categories: TMS370Cx32, TMS370Cx36, TMS370Cx4x, TMS370Cx5x, TMS370Cx6x, TMS370Cx7x and TMS370CxBx.

The ADC1 module has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3}. The purpose is to enhance ADC1 performance by preventing digital switching noise of the logic circuitry that may be present on V_{SS} and V_{CC} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution . . . . . 8-bits (256 values)
Monotonic . . . . . Yes
Output conversion code . . . . . 00h to FFh
(00h for $V_I \leq V_{SS3}$; FFh for $V_I \geq V_{ref}$)
Conversion time (excluding sample time) . . . . . 164 t_c
(where t_c = system clock cycle time)

Table 18–80. Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
V_{CC3}	Analog supply voltage	4.5	5	5.5	V
		V_{CC} – 0.3		V_{CC} + 0.3	V
V_{SS3}	Analog ground	V_{SS} – 0.3		V_{SS} + 0.3	V
V_{ref}	Non-V_{CC3} reference (see Note)	2.5	V_{CC3}	V_{CC3} + 0.1	V
	Analog input for conversion	V_{SS3}		V_{ref}	V

Note: V_{ref} must be stable, within ± 1/2 LSB of the required resolution, during the entire conversion time. $V_{CC} = V_{CC1}$ and $V_{SS} = V_{SS1}$ for 'x32, 'x36, 'x5x, 'x6x, 'x7x, and 'xBx devices.

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Table 18–81. ADC1 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter		Test Conditions	Min	Max	Unit
	Absolute accuracy (see Note 1)	V_{CC3} = 5.5 V, V_{ref} = 5.1 V		±1.5	LSB
	Differential/integral linearity error (see Notes 1 and 2)	V_{CC3} = 5.5 V, V_{ref} = 5.1 V		±0.9	LSB
I_{CC3}	Analog supply current	Converting		2	mA
		Nonconverting		5	µA
I_I	Input current, AN0–AN7	0 V ≤ V_I ≤ 5.5 V		2	µA
I_{ref}	input charge current			1	mA
Z_{ref}	Source impedance of V_{ref}	SYSCLK ≤ 3 MHz		24	kΩ
		3 MHz < SYSCLK ≤ 5 MHz		10	kΩ

Notes: 1) Absolute resolution = 20 mV. At V_{ref} = 5 V, this is one LSB. As V_{ref} decreases, LSB size decreases. Therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

2) Excluding quantization error of 1/2 LSB

The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that high-impedance sources can be accommodated without penalty to low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter resets the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

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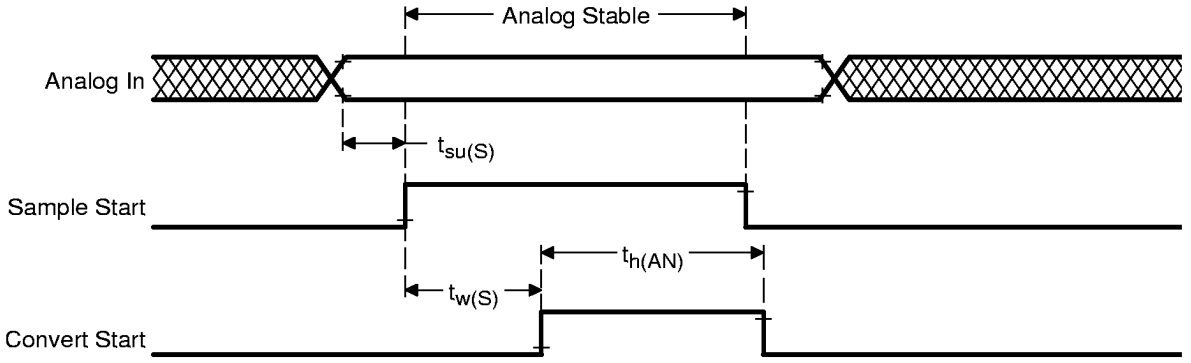
Table 18–82. Analog Timing Requirements

Parameter		Min	Max	Unit
$t_{su(S)}$	Setup time, analog to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion	$18t_c$		ns
$t_{w(S)}$	Pulse duration, sample time per kilohm of source impedance (see Note)	1		µs/kΩ

Note: The value given is valid for a signal with a source impedance > 1 kΩ. If the source impedance is < 1 kΩ, use a minimum sampling time of 1 µs.

Figure 18–54. Analog Timing



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18.24 Analog-to-Digital Converter 2 (ADC2) Module Specifications

This section contains specifications for the TMS370CxCx device category, which has the analog-to-digital converter 2 (ADC2) module. ADC2 shares the V_{CC} power bus for its analog and digital circuitry. All ADC2 specifications are given with respect to V_{SS} unless otherwise noted.

Resolution . . . . . 8-bits (256 values)
Monotonic . . . . . Yes
Output conversion code . . . . . 00h to FFh
(00h for $V_I \leq V_{SS} \leq$; FFh for $V_I \leq V_{ref}$)
Conversion time (excluding sample time) . . . . . 164 t_c
(where t_c = system clock cycle time)

Table 18–83. Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
V_{CC}	Analog supply voltage	4.5	5	5.5	V
V_{ref}	Non-V_{CC} reference (see Note)	2.5	V_{CC}	V_{CC} + 0.1	V
	Analog input for conversion	V_{SS}		V_{ref}	V

Note: V_{ref} must be stable, within ±1/2 LSB of the required resolution during the entire conversion time.

Table 18–84. ADC2 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter		Test Conditions	Min	Max	Unit
	Absolute accuracy (see Note 1)	V_{CC} = 5.5 V, V_{ref} = 5.1 V		+1.5	LSB
	Differential/integral linearity error (see Notes 1 and 2)	V_{CC} = 5.5 V, V_{ref} = 5.1 V		±0.9	LSB
I_{CC}	Analog supply current	Converting		2	mA
		Nonconverting		5	µA
I_I	Input current, AN0-AN3	0 V ≤ V_I ≤ 5.5 V		2	µA
I_{ref}	Input charge current			1	mA
Z_{ref}	Source impedance of V_{ref}	SYSCLK ≤ 3 MHz		24	kΩ
		3 MHz < SYSCLK ≤ 5 MHz		10	kΩ

Notes: 1) Absolute resolution = 20 mV. At V_{ref} = 5 V, this is 1 LSB. As V_{ref} decreases, LSB size decreases and thus absolute accuracy and differential / integral linearity errors in terms of LSBs increases.
2) Excluding quantization error of 1/2 LSB

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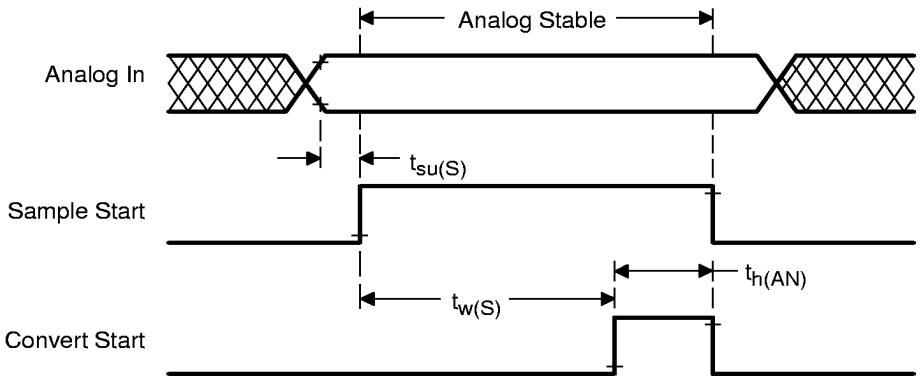
The ADC2 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that high-impedance sources can be accommodated without penalty to low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC2 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter resets the SAMPLE START and CONVERT START bits, signaling that a conversion has started and the analog signal can be removed.

Table 18–85. Analog Timing Requirements

Parameter		Min	Max	Unit
$t_{su(S)}$	Setup time, analog input to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion	$18t_c$		ns
$t_{w(S)}$	Pulse duration, sample time per kilohm of source impedance (see Note)	1		µs/kΩ

Note: The value given is valid for a signal with a source impedance > 1 kΩ. If the source impedance is < 1 kΩ, use a minimum sampling time of 1 µs.

Figure 18–55. Analog Timing



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18.25 Analog-to-Digital Converter 3 (ADC3) Module Specifications

This section contains specifications for the TMS370Cx9x device category, which has the analog-to-digital converter 3 (ADC3) module.

The ADC3 module has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3}. The purpose is to enhance ADC3 performance by preventing digital switching noise of the logic circuitry that may be present on V_{SS} and V_{CC} from coupling into the ADC3 analog stage. All ADC3 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution . . . . . 8-bits (256 values)
Monotonic . . . . . Yes
Output conversion code . . . . . 00h to FFh
(00h for $V_I \leq V_{SS3} \leq$; FFh for $V_I \leq V_{ref}$)
Conversion time (excluding sample time) . . . . . 164 t_c
(where t_c = system clock cycle time)

Table 18–86. Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
V_{CC3}	Analog supply voltage	4.5	5	5.5	V
		V_{CC} – 0.3		V_{CC} + 0.3	V
V_{SS3}	Analog input ground	V_{SS} – 0.3		V_{SS} + 0.3	V
V_{ref}	Non-V_{CC3} reference (see Note)	2.5	V_{CC3}	V_{CC3} + 0.1	V
	Analog input for conversion	V_{SS3}		V_{ref}	V

Note: V_{ref} must be stable, within ±1/2 LSB of the required resolution during the entire conversion time.

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Table 18–87. ADC3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter		Test Conditions	Min	Max	Unit
	Absolute accuracy (see Note 1)	V_{CC3} = 5.5 V, V_{ref} = 5.1 V		±1.5	LSB
	Differential/integral linearity error (see Notes 1 and 2)	V_{CC3} = 5.5 V , V_{ref} = 5.1 V		±0.9	LSB
I_{CC3}	Analog supply current	Converting		2	mA
		Nonconverting		5	µA
I_I	Input current, AN0–AN14	0 V ≤ V_I ≤ 5.5 V		2	µA
I_{ref}	Input charge current			1	mA
Z_{ref}	Source impedance of V_{ref}	SYSCLK ≤ 3 MHz		24	kΩ
		3 MHz < SYSCLK ≤ 5 MHz		10	kΩ

Notes: 1) Absolute resolution = 20 mV. At V_{ref} = 5 V, this is 1 LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

2) Excluding quantization error of 1/2 LSB

The ADC3 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that high-impedance sources can be accommodated without penalty to low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC3 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter resets the SAMPLE START and CONVERT START bits, signaling that a conversion has started and the analog signal can be removed.

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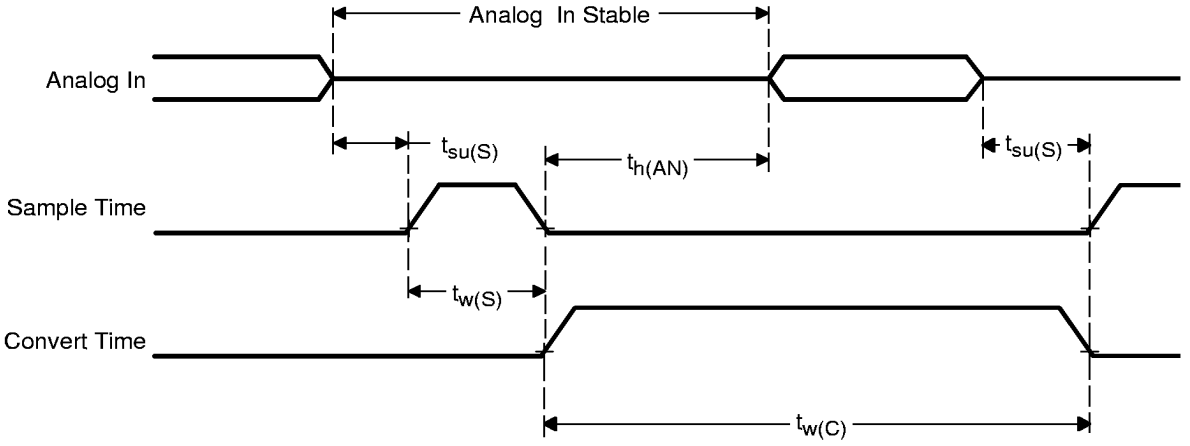
Table 18–88. Analog Timing Requirements

Parameter		Min	Max	Unit
$t_{su(S)}$	Setup time, analog to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion (see Note 2)	$(N+2)t_c$		ns
$t_{w(C)}$	Conversion time (see Note 2)	$(10N + 4)t_c$		ns
$t_{w(S)}$	Pulse duration, sample time per kilohm of source impedance (see Note 1)	1		µs/kΩ

Notes: 1) The value given is valid for a signal with a source impedance > 1 kΩ. If the source impedance is < 1 kΩ, use a minimum sampling time of 1µs.

2) N = 16, 8, 4, or 2 upon selected conversion rate.

Figure 18–56. Analog Timing



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