P3C214
ULTRA HIGH-SPEED
16K x 16 LATCHED RAM

FEATURES

- Cache RAM for 3.3V i386 and i486 Processors
- Supports Processor Speeds up to 66 MHz
- Easily Configurable
  Direct Map 16Kx16
  Two-Way Set 2x8Kx16
- On-chip Address Latch
- Separate Lower & Upper Byte Select
- Single 3.3V ±0.3V Power Supply
- CMOS for Optimum Speed/Power
- Common Data I/O
- TTL Compatible Inputs & Outputs
- Three-State Outputs
- 52-pin PLCC Package

DESCRIPTION

The P3C214 is a 262,144-bit ultra high-speed CMOS cache SCRAM (Static CMOS Random Access Memory) with latched addresses. It is ideally suited as cache RAM for 3.3V i386 and i486 processors from AMD and Intel.

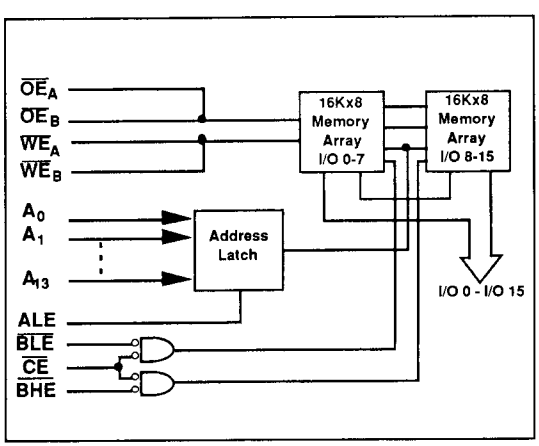
A mode control pin (MODE) controls the configuration of the memory. When this pin is Low, the SCRAM functions as a direct mapped 16Kx16-bit RAM with A0 having a faster addressing speed. When the MODE pin is High, the SCRAM functions as a two-way associative 2x8Kx16. In this mode, address bit A0 is not used and should be externally wired to ground.

The P3C214 operates from a 3.3V ±0.3V tolerance power supply. The lower voltage reduces power dissipation to 50% of that for a comparable 5V SRAM. In addition, smaller output swings improve the noise margin, enabling simpler system design at higher frequencies. Access times of 11ns permit operation up to 66MHz. Two devices form a 64KByte cache; four devices form a 128KByte cache, when used with an iX86.

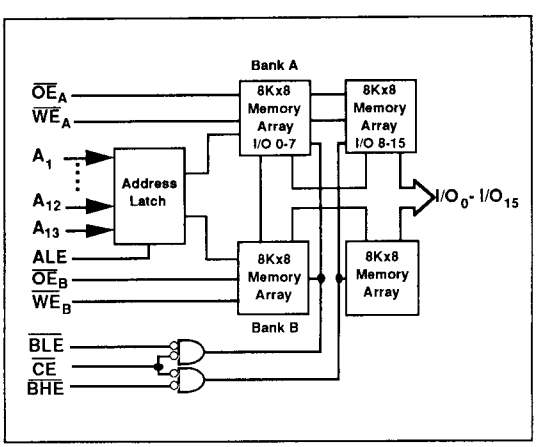
The P3C214 is manufactured using PACE III technology and is available in a 52-pin PLCC surface-mount package, providing excellent board-level density.

6

DIRECT MAP (MODE = L)



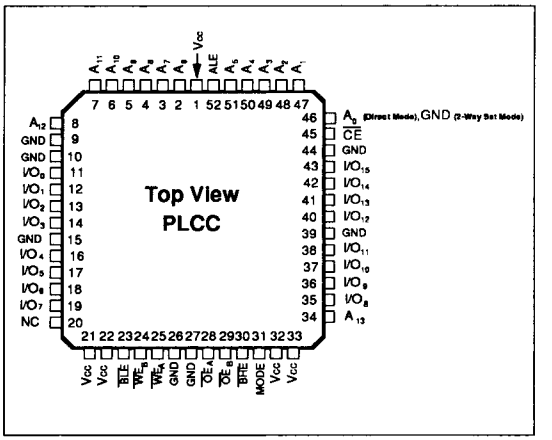
TWO-WAY SET (MODE = H)



PIN DESCRIPTIONS

Symbol	Type Description
$A_1 - A_{13}$	Address Inputs: Latched on the negative edge of ALE.
A_0	Fast Latched Address Input: Latched on the negative edge of ALE. Used in direct mode only. ***Must be GND for 2-way mode.***
ALE	Address Latch Enable: When ALE is high, the latch is transparent. The negative edge latches the current address inputs (A_0–A_{13}).
$\overline{CE}$	Chip Enable: To facilitate depth expansion.
$\overline{BLE}$, $\overline{BHE}$	Byte Selects: These control signals control the lower and upper byte selection on the A or B side of the array. They also facilitate depth expansion.
$\overline{OE}_A$, $\overline{OE}_B$	Output Enables: In the Two-Way Set Associative Mode, Active LOW enables cache bank A or B to drive the data bus. In the direct mode, these two pins must be wired together.
$\overline{WE}_B$, $\overline{WE}_A$	Write Enables: These active LOW signals enable bank A or B. In the Two-Way Associative Mode, data may be written to bank A or B. In the direct mode, these two pins must be wired together.
I/O_0 - I/O_{15}	Data inputs and outputs.
Vcc	3.3V ±0.3V
GND	Ground
MODE	Configuration Control: When signal is LOW, the device functions as a direct map 16Kx16. When signal is HIGH, the device functions as a two-way associative 2x8Kx16.

PIN CONFIGURATION



i386 / i486 SYSTEM APPLICATION