IQ Family Data Sheet Update

IQ96, IQ64B, IQ48, IQ32B

Features

- 32, 48, 64 and 96 I/O Ports
- SRAM-based Programming for In-system Reconfigurability
- Switch Matrix Architecture
  - Non-blocking
  - Predictable & Uniform Delays
  - One-to-One & One-to-Many Connections
  - Incremental Connection Changes
- Programmable I/O Ports
  - Individually Programmable as Input, Output or Bidirectional
  - Programmable TTL/CMOS Output
- Clocked and Flow-through Dataflow Modes
  - Pin-to-Pin Delay as low as 5 ns in Flow-through Mode
  - Up to 150 MHz Clock Frequency
- RapidConnect™ Interface for Switching of Connections in under 30 ns
- JTAG for Boundary Scan Testing and Configuration

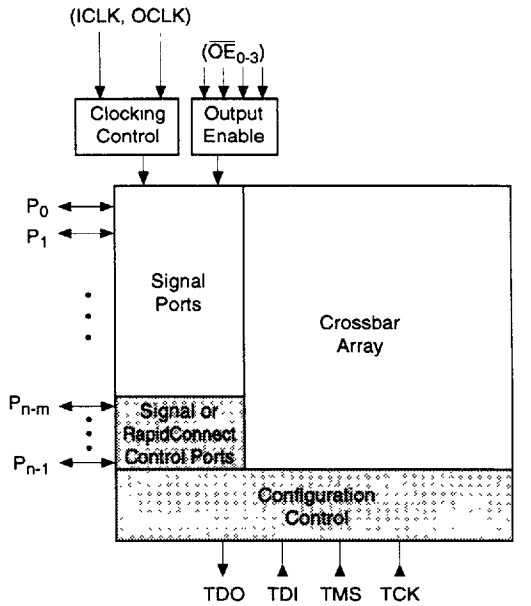
Description

These additional members in the IQ (previously called FPID) family are based on 0.6µm CMOS Process.

The IQ devices are designed for use in switching and interconnect applications. In switching applications, these devices are used to dynamically switch one or more signals. When used in interconnect applications, the IQ devices allow static routing of signals on a board or backplane.

At the heart of these devices is a non-blocking switch matrix, allowing total flexibility in routing signals. Every signal in the crossbar switch can be connected to one or more other signals. The I/O ports, connected to the switch matrix lines, are individually programmable as input, output or bidirectional. The IQ devices support either flow-through or clocked signal flow. The delays through the devices are identical and predictable.

The crossbar connections are programmed and the I/O port attributes are configured by storing data in the internal SRAM cells. The IQ devices use a JTAG-based serial mode for configuration. For dynamic switching, the RapidConnect interface allows fast connection changes.



Device	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
n	320	240	160	128	96	64	48	32
m	24	24	20	18	18	16	15	13

n = total number of usable I/O pins
m = I/O pins used for RapidConnect

Figure 1: IQ Family Functional Block Diagram

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The first eight devices in the IQ family are summarized below. Contact I-Cube Marketing for information on the other devices in the family.

Device	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
Number of Usable I/O	320	240	160	128	96	64	48	32
Crossbar Matrix Size	320 x 320	240 x 240	160 x 160	128 x 128	96 x 96	64 x 64	48 x 48	32 x 32
Pin-to-Pin Delay	12 ns	12 ns	10 ns	10 ns	6 ns	6 ns	5 ns	5 ns
NRZ Data Rate	133 Mb/s	133 Mb/s	160 Mb/s	160 Mb/s	200 Mb/s	200 Mb/s	250 Mb/s	250 Mb/s
Clock Frequency	80 MHz	80 MHz	100 MHz	100 MHz	125 MHz	125 MHz	150 MHz	150 MHz
I/O Current Drive	16 mA	16 mA	16 mA	16 mA	16 mA	16 mA	16 mA	16 mA

Table 1: The IQ Family

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ın Summary

e pin summary for the first eight members of the IQ family is given here in Table 2 and 3. Contact I-Cube ırketing for information on other devices not listed here.

Pin Name								Description
IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B	
00 - P295	P000 - P215	P000 - P139	P000 - P109	P00 - P77	P00 - P47	P00 - P32	P00 - P18	I/O port pins
96 - P305/ ₀ - CA_9	P216 - P225/ CA_0 - CA_9	P140 - P147/ CA_0 - CA_7	P110 - P116/ CA_0 - CA_6	P78 - P84/ CA_0 - CA_6	P48 - P53/ CA_0 - CA_5	P33 - P38/ CA_0 - CA_5	P19 - P23/ CA_0 - CA_4	I/O port pins in JTAG serial configuration mode and crossbar column address pins in RapidConnect mode
06 - P315/ ₀ - RA_9	P226 - P235/ RA_0 - RA_9	P148 - P155/ RA_0 - RA_7	P117 - P123/ RA_0 - RA_6	P85 - P91/ RA_0 - RA_6	P54 - P59/ RA_0 - RA_5	P39 - P44/ RA_0 - RA_5	P24 - P28/ RA_0 - RA_4	I/O port pins in JTAG serial configuration mode and crossbar row address pins in RapidConnect mode
16/C_0	P236/C_0	P156/C_0	P124/C_0	P92/C_0	P60/C_0	P45/C_0	P29/C_0	I/O port or RapidConnect control bit 0
17/C_1	P237/C_1	P157/C_1	P125/C_1	P93/C_1	P61/C_1	-	-	I/O port or RapidConnect control bit 1
18/$\overline{WE}$	P238/$\overline{WE}$	P158/$\overline{WE}$	P126/$\overline{WE}$	P94/$\overline{WE}$	P62/$\overline{WE}$	P46/$\overline{WE}$	P30/$\overline{WE}$	I/O port or RapidConnect write enable, Active low
19/$\overline{STROBE}$	P239/$\overline{STROBE}$	P159/$\overline{STROBE}$	P127/$\overline{STROBE}$	P95/$\overline{STROBE}$	P63/$\overline{STROBE}$	P47/$\overline{STROBE}$	P31/$\overline{STROBE}$	I/O port or RapidConnect strobe, Active low
:0-3	$\overline{OE}_{0-3}$	$\overline{OE}_{0-3}$	$\overline{OE}_{0-3}$	$\overline{OE}_{0-3}$	$\overline{OE}_{0-3}$	$\overline{OE}_0$	$\overline{OE}_0$	Dedicated output enable control pins. Active low. Each pin controls an equal number of I/O pins. See next table.
_K	ICLK	ICLK	ICLK	ICLK	ICLK	ICLK	ICLK	Clock for input registers
:LK	OCLK	OCLK	OCLK	OCLK	OCLK	OCLK	OCLK	Clock for output registers
)I, TMS,)O, TCK,	TDI, TMS, TDO, TCK,	TDI, TMS, TDO, TCK,	TDI, TMS, TDO, TCK,	TDI, TMS, TDO, TCK,	TDI, TMS, TDO, TCK,	TDI, TMS, TDO, TCK,	TDI, TMS, TDO, TCK,	JTAG serial bus pins
ST*	TRST*	TRST*	TRST*	TRST*	TRST*	TRST*	TRST*	Chip Reset, Active low
)D	R_{OD}	N/A	N/A	N/A	N/A	N/A	N/A	12K resistor to ground
)	R_{ID}	N/A	N/A	N/A	N/A	N/A	N/A	12K resistor to ground
'U	R_{PU}	N/A	N/A	N/A	N/A	N/A	N/A	18K resistor to ground

Table 2: Pin Summary

	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
$\overline{OE}_0$	0 -79	0-59	0-39	0-31	0-23	0-15	0-47	0-31
$\overline{OE}_1$	80-159	60-119	40-79	32-63	24-47	16-31	-	-
$\overline{OE}_2$	160-239	120-179	80-119	64-95	48-71	32-47	-	-
$\overline{OE}_3$	240-319	180-239	120-159	96-127	72-95	48-63	-	-

Table 3: I/O Ports and Controlling Output Enable Signals

NOTE:

On the newer members in the IQ family, IQ96, IQ64B, IQ48 and IQ32B, power pins (designated as V_{DD}.PAD) for the I/O buffer drivers are separated from the power pins (designated as V_{DD}) for the rest of the circuitry. By lowering the V_{DD}.PAD voltage and configuring the programmable I/Os for CMOS voltage level, the IQ devices can be easily interfaced with 3V/3.3V devices.

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Electrical Specification

Absolute Maximum Ratings (1)

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	-0.3 to +7.0	V
V_{IN}	Input Voltage (1)	-0.3 to V_{DD}+0.3	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	+4.75 to +5.25	V
T_A	Operating Temperature	0 to +70	°C

Capacitance (2)

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance (JTAG, OE and CLK pins)	5	pF
C_{OUT}	Output Capacitance (TDO pin)	8	pF
C_{PORT}	Signal Port Capacitance	8	pF

Notes:
(1) Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Capacitance measured at 25°C. Sample-tested only.

DC Specifications

(T_A = 0°C to 70°C)

(V_{DD} and V_{DD}.PAD = 5V ± 5%) and (T_A = 0°C to 70°C, V_{DD} = 5V ± 5%, V_{DD}.PAD = 3V ± 10%)

Symbol	Parameter	Condition	IQ96, IQ64B		IQ48, IQ32B		Units
			Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	V_{DD}+0.3	2.0	V_{DD}+0.3	V
V_{IL}	Low-Level Input Voltage		- 0.3	0.8	- 0.3	0.8	V
V_{OH}	High-Level Output Voltage (1)	V_{DD} = Min, I_{OH} = - 8mA,- 4(6)mA	2.4	-	2.4	-	V
V_{OL}	Low-Level Output Voltage	V_{DD} = Min, I_{OL} = 16 mA	-	0.4	-	0.4	V
$\|I_{IL}\|$ $\|I_{IH}\|$	Input Leakage Current for I/O Ports (2)	V_{DD} = Max, 0 ≤ V_{IN} ≤ V_{DD}	-	5	-	5	µA
$\|I_{IL}\|$ $\|I_{IH}\|$	Input Leakage Current for Other Input Pins (3)	V_{DD} = Max, 0 ≤ V_{IN} ≤ V_{DD}	5	20	5	20	µA
$\|I_{OZ}\|$	Tristate Output Off-State Current	V_{DD} = Max, 0 ≤ V_{IN} ≤ V_{DD}	-	5	-	5	µA
I_{PU-LO}	Programmed-Low Additional Bus-Repeater Current (1)	V_{DD} = Min, V_O = GND	2.5	4.5	2.5	4.5	mA
I_{PU-HI}	Programmed-High Additional Bus-Repeater Current (1)	V_{DD} = Min, V_O = GND	10	15	10	15	mA
I_{OS}	Short Circuit Current (1, 4, 5)	V_{DD} = Min, V_O = GND	-60	-	-60	-	mA
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max, V_O = GND	-	3.0	-	1.5	mA
Q_{DDD}	Dynamic Power Supply Current per Input per MHz (4)	V_{DD} = Max, No Load, Connect one output per input, Toggle one input @ 50% duty cycle with all other inputs at GND or V_{DD}	-	0.1	-	0.1	mA/ MHz

Notes:
(1) For TTL output mode.
(2) Transient currents of 250 µA are required to pull I/O ports from logic high to logic low.
(3) Transient currents of 650 µA are required to pull input pins from logic high to logic low.
(4) These parameters are guaranteed but not tested in production.
(5) No more than one output should be tested at a time, and the duration of the test should be less than one second.
(6) I_{OH} when V_{DD}.PAD = 3V ± 10%

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AC Specifications IQ96, IQ64B

(T_A = 0°C to 70°C)

(V_{DD} and V_{DD}.PAD = 5V ± 5%) and (T_A = 0°C to 70°C, V_{DD} = 5V ± 5%, V_{DD}.PAD = 3V ± 10%)

	Speed Grade	-6		-10		-12		-15		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay Time	-	6	-	10	-	12.5	-	15	ns
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)	-	0.25	-	0.25	-	0.25	-	0.25	ns
$t_{\Delta BR}$	Additional Delay in Bus Repeater (BR) Mode	-	0	-	0	-	0	-	0	ns
$t_{\Delta CMOS}$	Additional Delay When Output Voltage Level is CMOS	-	0.5	-	0.5	-	0.5	-	0.5	ns
t_{SK}	Skew Between Output Ports (1)	-	1.0	-	1.0	-	1.0	-	1.0	ns
R_{DATA}	NRZ Data Rate (1)	-	200	-	160	-	133	-	100	Mbs
t_{W+}	Positive Input signal Pulse Width	6	-	7	-	8.5	-	11	-	ns
t_{W-}	Negative Input signal Pulse Width	4	-	5.5	-	6.5	-	9	-	ns
t_{PZL}, t_{PZH}	Output Enable to Data Valid Time	-	8	-	12	-	14.5	-	17	ns
t_{PLZ}, t_{PHZ}	Output Disable to Output at High Z Time (1)	-	8	-	12	-	14.5	-	17	ns
f_{RI}	Register Input Clock Frequency (1)	-	125	-	100	-	80	-	66	MHz
t_{W-RI}	Register Input Clock Pulse Width, Low or High	3.5	-	4.5	-	5.5	-	6.5	-	ns
t_{S-RI}	Register Input Setup Time	1	-	1	-	1	-	1	-	ns
t_{H-RI}	Register Input Hold Time	1	-	1	-	1	-	1	-	ns
t_{P-RI}	Register Input Clock to Output Data Valid	-	10	-	14	-	16.5	-	19	ns
f_{RO}	Register Output Clock Frequency (1)	-	125	-	100	-	80	-	66	MHz
t_{W-RO}	Register Output Clock Pulse Width, Low or High	3.5	-	4.5	-	5.5	-	6.5	-	ns
t_{S-RO}	Register Output Setup Time	4	-	5	-	6	-	7	-	ns
t_{H-RO}	Register Output Hold Time	0	-	0	-	0	-	0	-	ns
t_{P-RO}	Register Output Clock to Data Valid	-	7.5	-	11.5	-	14	-	16.5	ns
f_{RIO}	Register Input/Output Clock Frequency (1)	-	125	-	100	-	80	-	66	MHz
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High	3.5	-	4.5	-	5.5	-	6.5	-	ns
t_{S-RIO}	Register Input/Output Setup Time	1	-	1	-	1	-	1	-	ns
t_{H-RIO}	Register Input/Output Hold Time	1	-	1	-	1	-	1	-	ns
t_{P-RIO}	Register Input/Output Clock to Data Valid	-	7.5	-	10	-	12.5	-	15	ns
t_{SK-ZC}	ICLK/OCLK skew for zero clock delay output (1)	4		4		4		4		ns
t_{SK-OC}	ICLK/OCLK skew for one clock delay output (1)		1		1		1		1	ns
f_{JTAG}	JTAG Clock (TCK) Frequency	-	25	-	25	-	25	-	25	MHz
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width, Low or High	20	-	20	-	20	-	20	-	ns
t_{S-JTAG}	JTAG Setup Time	15	-	15	-	15	-	15	-	ns
t_{H-JTAG}	JTAG Hold Time	15	-	15	-	15	-	15	-	ns
t_{P-JTAG}	JTAG Clock to Output Valid	15	-	15	-	15	-	15	-	ns
f_{RC}	Rapid Connect Strobe Frequency (1)	-	25	-	25	-	25	-	25	MHz
T_{RC}	RapidConnect Strobe Period	30	-	30	-	30	-	30	-	ns
t_{W-RC}	RapidConnect Strobe Pulse Width	13.5	-	13.5	-	13.5	-	13.5	-	ns
t_{S-RC}	RapidConnect Address and Data Set up Time	8	-	8	-	8	-	8	-	ns
t_{H-RC}	RapidConnect Address and Data Hold Time	8	-	8	-	8	-	8	-	ns
t_{P-RC}	RapidConnect Strobe Falling Edge to Data Valid for Making Connection or to Data Invalid for Breaking Connection	30	-	30	-	30	-	30	-	ns

Notes:
(1) These parameters are guaranteed but not tested in production.

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AC Specifications for IQ48, IQ32B

(T_A = 0°C to 70°C)

(V_{DD} and V_{DD}.PAD = 5V ± 5%) and (T_A = 0°C to 70°C, V_{DD} = 5V ± 5%, V_{DD}.PAD = 3V ± 10%)

	Speed Grade	-5		-7		-10		-12		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay Time	-	5	-	7.5	-	10	-	12.5	ns
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)	-	0.25	-	0.25	-	0.25	-	0.25	ns
$t_{\Delta BR}$	Additional Delay in Bus Repeater (BR) Mode	-	0	-	0	-	0	-	0	ns
$t_{\Delta CMOS}$	Additional Delay When Output Voltage Level is CMOS	-	0.5	-	0.5	-	0.5	-	0.5	ns
t_{SK}	Skew Between Output Ports (1)	-	0.5	-	0.5	-	0.5	-	0.5	ns
R_{DATA}	NRZ Data Rate (1)	-	250	-	200	-	160	-	133	Mbs
t_{W+}	Positive Input signal Pulse Width	5	-	6	-	7	-	8.5	-	ns
t_{W-}	Negative Input signal Pulse Width	3	-	4	-	5.5	-	6.5	-	ns
t_{PZL}, t_{PZH}	Output Enable to Data Valid Time	-	6	-	8.5	-	11	-	13.5	ns
t_{PLZ}, t_{PHZ}	Output Disable to Output at High Z Time (1)	-	6	-	8.5	-	11	-	13.5	ns
f_{RI}	Register Input Clock Frequency (1)	-	150	-	125	-	100	-	80	MHz
t_{W-RI}	Register Input Clock Pulse Width, Low or High	3	-	3.5	-	4.5	-	5.5	-	ns
t_{S-RI}	Register Input Setup Time	1	-	1	-	1	-	1	-	ns
t_{H-RI}	Register Input Hold Time	1	-	1	-	1	-	1	-	ns
t_{P-RI}	Register Input Clock to Output Data Valid	-	10	-	12	-	14	-	16.5	ns
f_{RO}	Register Output Clock Frequency (1)	-	150	-	125	-	100	-	80	MHz
t_{W-RO}	Register Output Clock Pulse Width, Low or High	3	-	3.5	-	4.5	-	5.5	-	ns
t_{S-RO}	Register Output Setup Time	3.5	-	4	-	5	-	6	-	ns
t_{H-RO}	Register Output Hold Time	0	-	0	-	0	-	0	-	ns
t_{P-RO}	Register Output Clock to Data Valid	-	6	-	8.5	-	11	-	13.5	ns
f_{RIO}	Register Input/Output Clock Frequency (1)	-	150	-	125	-	100	-	80	MHz
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High	3	-	3.5	-	4.5	-	5.5	-	ns
t_{S-RIO}	Register Input/Output Setup Time	1	-	1	-	1	-	1	-	ns
t_{H-RIO}	Register Input/Output Hold Time	1	-	1	-	1	-	1	-	ns
t_{P-RIO}	Register Input/Output Clock to Data Valid	-	6	-	8.5	-	11	-	13.5	ns
t_{SK-ZC}	ICLK/OCLK skew for zero clock delay output (1)		-		-	7	-	8	-	ns
t_{SK-OC}	ICLK/OCLK skew for one clock delay output (1)	-		-		-	4.5	-	5	ns
f_{JTAG}	JTAG Clock (TCK) Frequency	-	25	-	25	-	25	-	25	MHz
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width, Low or High	20	-	20	-	20	-	20	-	ns
t_{S-JTAG}	JTAG Setup Time	15	-	15	-	15	-	15	-	ns
t_{H-JTAG}	JTAG Hold Time	15	-	15	-	15	-	15	-	ns
t_{P-JTAG}	JTAG Clock to Output Valid	15	-	15	-	15	-	15	-	ns
f_{RC}	RapidConnect Strobe Frequency (1)	-	25	-	25	-	25	-	25	MHz
T_{RC}	RapidConnect Strobe Period	30	-	30	-	30	-	30	-	ns
t_{W-RC}	RapidConnect Strobe Pulse Width	13.5	-	13.5	-	13.5	-	13.5	-	ns
t_{S-RC}	RapidConnect Address and Data Set up Time	8	-	8	-	8	-	8	-	ns
t_{H-RC}	RapidConnect Address and Data Hold Time	8	-	8	-	8	-	8	-	ns
t_{P-RC}	RapidConnect Strobe Falling Edge to Data Valid for Making Connection or to Data Invalid for Breaking Connection	30	-	30	-	30	-	30	-	ns

Notes:
(1) These parameters are guaranteed but not tested in production.

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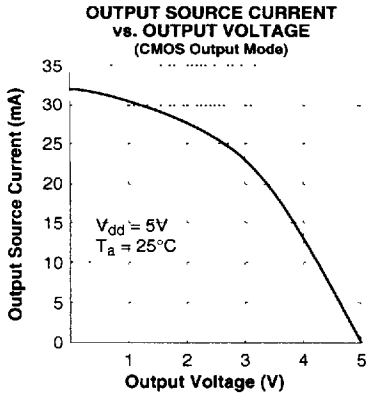
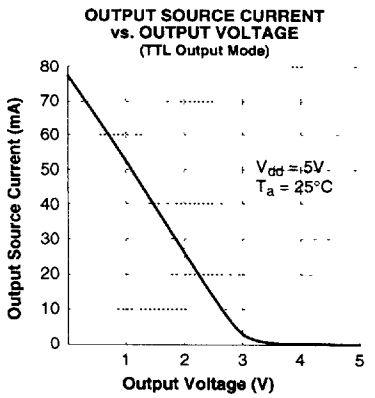
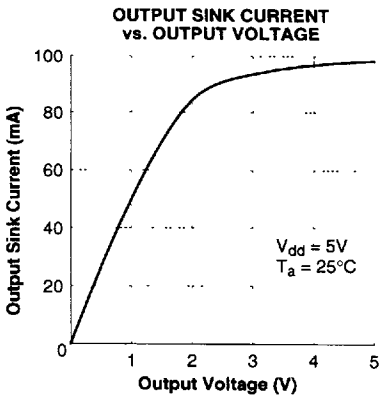
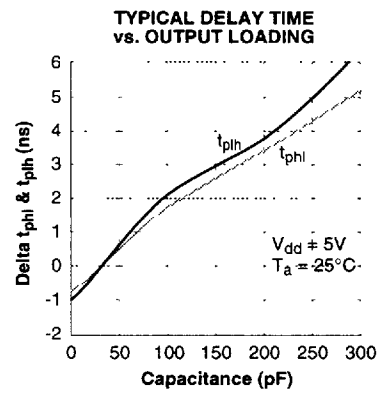
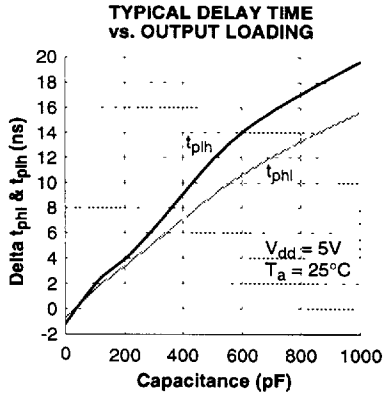
Typical AC and DC Characteristics of IQ96 and IQ64B

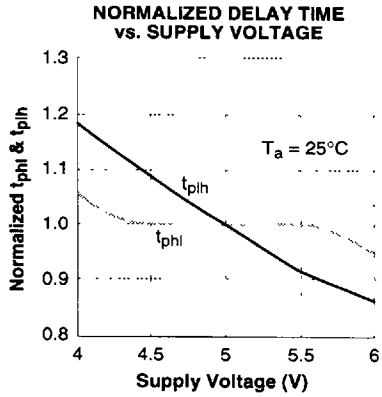


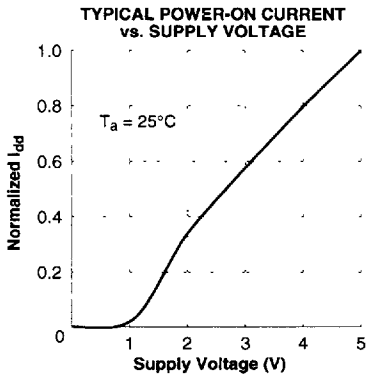


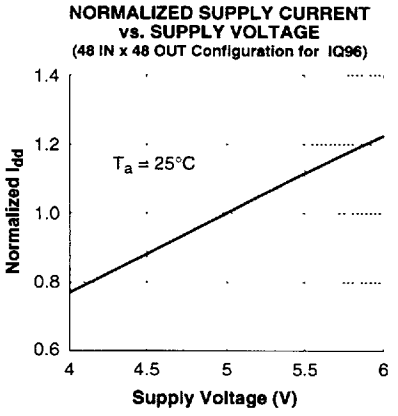


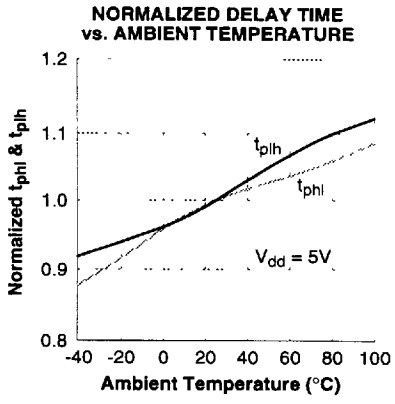












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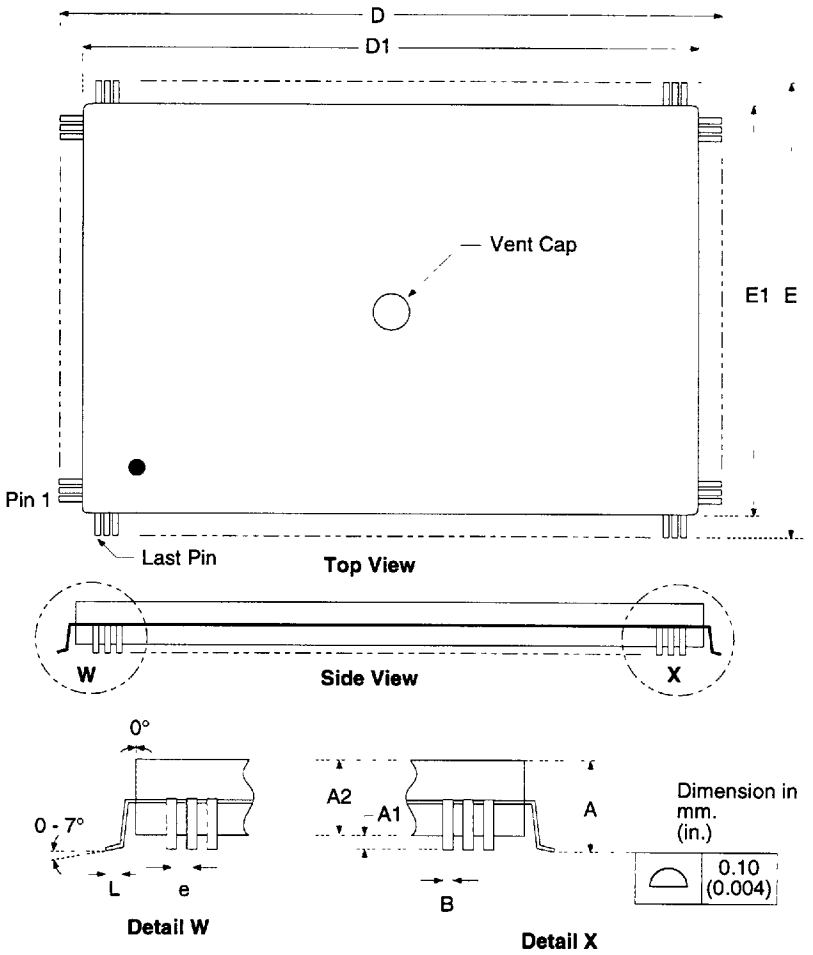
Mechanical Specifications

Mechanical specifications for the different device and package combinations are shown on the following pages. Data for the other package types will be available at a later date. Contact I-Cube Marketing for more information.

MQUAD Package Dimensions



Package Dimension Table		MQUAD/144L		MQUAD/100L	
		inch	mm	inch	mm
A	max	.152	3.96	.128	3.26
A1	min	0.14	0.35	.011	0.28
	max	0.21	0.53	.019	0.48
A2	min	.125	3.17	.099	2.51
	max	.135	3.43	.109	2.78
D	min	1.219	30.95	.904	22.95
	max	1.238	31.45	.923	23.45
D1	min	1.086	27.59	.777	19.74
	max	1.094	27.79	.781	19.84
E	min	1.219	30.95	.667	16.95
	max	1.238	31.45	.687	17.45
E1	min	1.086	27.59	.541	13.74
	max	1.094	27.79	.545	13.84
L	min	.029	0.73	.029	0.73
	max	.041	1.03	.041	1.03
B	min	.009	0.22	.009	0.22
	max	.014	0.35	.014	0.35
e	BSC.	.0256	0.65	.0256	0.65

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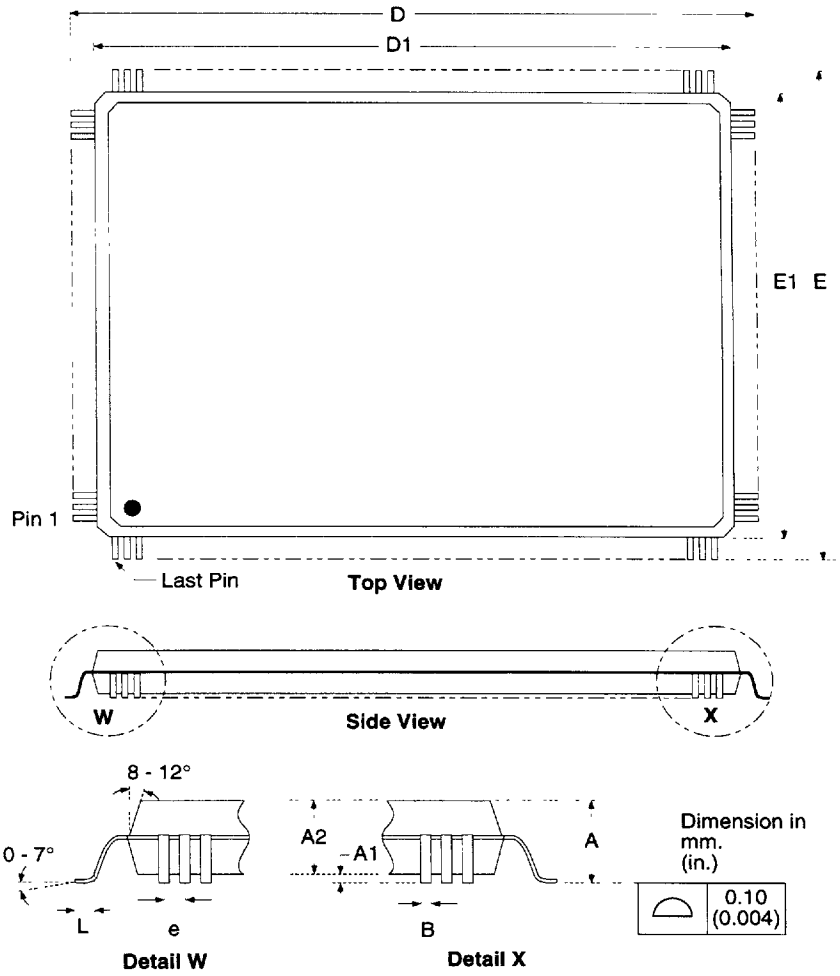
PQFP Package Dimensions



Package Dimension Table		PQFP/144L		PQFP/100L		PQFP/80L		PQFP/52L	
		inch	mm	inch	mm	inch	mm	inch	mm
A	max	.157	3.99	.130	3.30	.127	3.23	.096	2.45
A1	min	.010	0.25	.011	0.27	.012	0.30	.010	0.25
	max	.017	0.43	.017	0.43	.017	0.43	.015	0.38
A2	min	.135	3.43	.102	2.60	.102	2.60	.077	1.95
	max	.140	3.56	.110	2.80	.110	2.80	.081	2.07
D	min	1.219	31.01	.903	22.95	.904	22.95	.510	12.95
	max	1.238	31.49	.923	23.45	.923	23.45	.530	13.45
D1	min	1.098	27.93	.783	19.90	.783	19.90	.390	9.90
	max	1.106	28.14	.791	20.10	.791	20.10	.398	10.10
E	min	1.219	31.01	.667	16.95	.667	16.95	.510	12.95
	max	1.238	31.49	.687	17.45	.687	17.45	.530	13.45
E1	min	1.098	27.93	.547	13.90	.547	13.90	.390	9.90
	max	1.106	28.14	.555	14.10	.555	14.10	.398	10.10
L	min	.029	0.74	.023	0.60	.029	0.73	.029	0.73
	max	.041	1.04	.039	1.00	.041	1.03	.041	1.03
B	min	.009	0.23	.010	0.25	.012	0.30	.009	0.22
	max	.014	0.36	.014	0.35	.018	0.45	.014	0.35
e	BSC.	.0256	0.65	.0256	0.65	.0315	0.80	.0256	0.65

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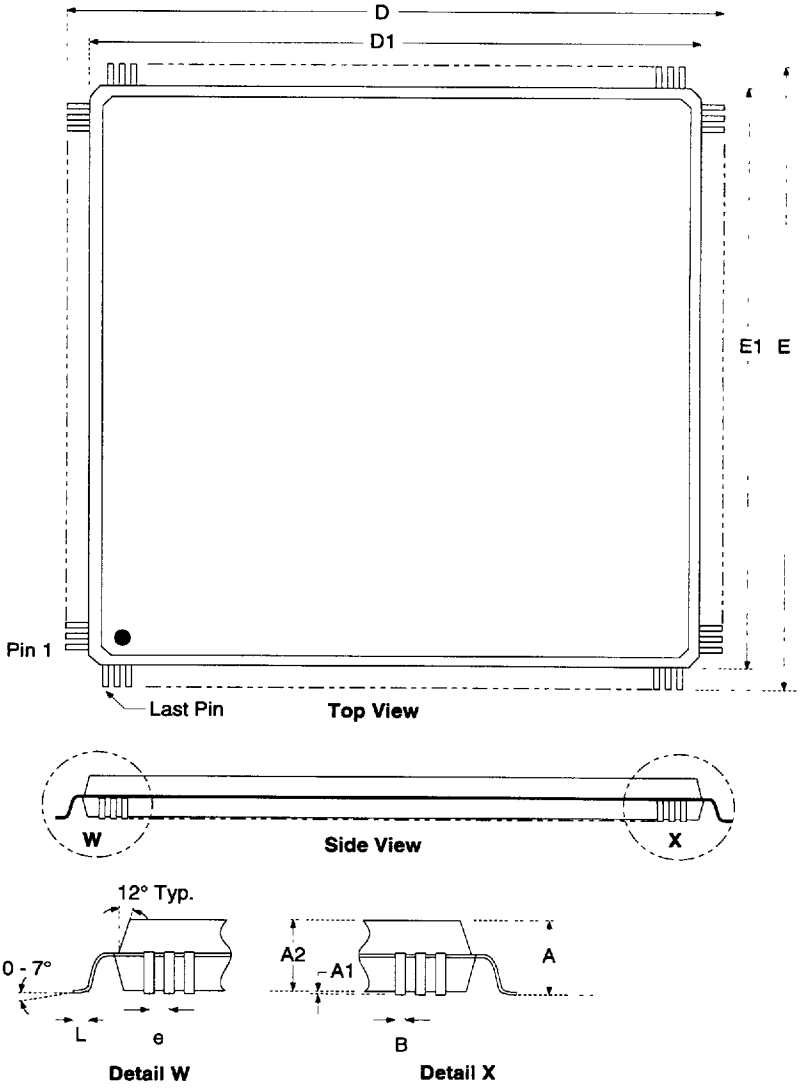
TQFP Package Dimensions



Package Dimension Table		TQFP/144L		TQFP/100L		TQFP/80L		TQFP/52L	
		inch	mm	inch	mm	inch	mm	inch	mm
A	max	.063	1.60	.063	1.60	.063	1.60	.063	1.60
A1	min	.002	0.05	.002	0.05	.002	0.05	.002	0.05
	max	.006	0.15	.006	0.15	.006	0.15	.006	0.15
A2	min	.053	1.35	.053	1.35	.053	1.35	.053	1.35
	max	.057	1.45	.057	1.45	.057	1.45	.057	1.45
D	min	.858	21.80	.622	15.80	.622	15.80	.465	11.80
	max	.874	22.20	.638	16.20	.638	16.20	.480	12.20
D1	min	.783	19.90	.547	13.90	.547	13.90	.390	9.90
	max	.791	20.10	.555	14.10	.555	14.10	.398	10.10
E	min	.858	21.80	.622	15.80	.622	15.80	.465	11.80
	max	.874	22.20	.638	16.20	.638	16.20	.480	12.20
E1	min	.783	19.90	.547	13.90	.547	13.90	.390	9.90
	max	.791	20.10	.555	14.10	.555	14.10	.398	10.10
L	min	.018	0.45	.012	0.30	.018	0.45	.018	0.45
	max	.030	0.75	.028	0.70	.030	0.75	.030	0.75
B	min	.007	0.17	0.007	0.17	.009	0.22	.009	0.22
	max	.011	0.2 7	0.111	0.27	.015	0.38	.015	0.38
e	BSC.	.0197	0.50	.0197	0.50	.0256	0.65	.0256	0.65

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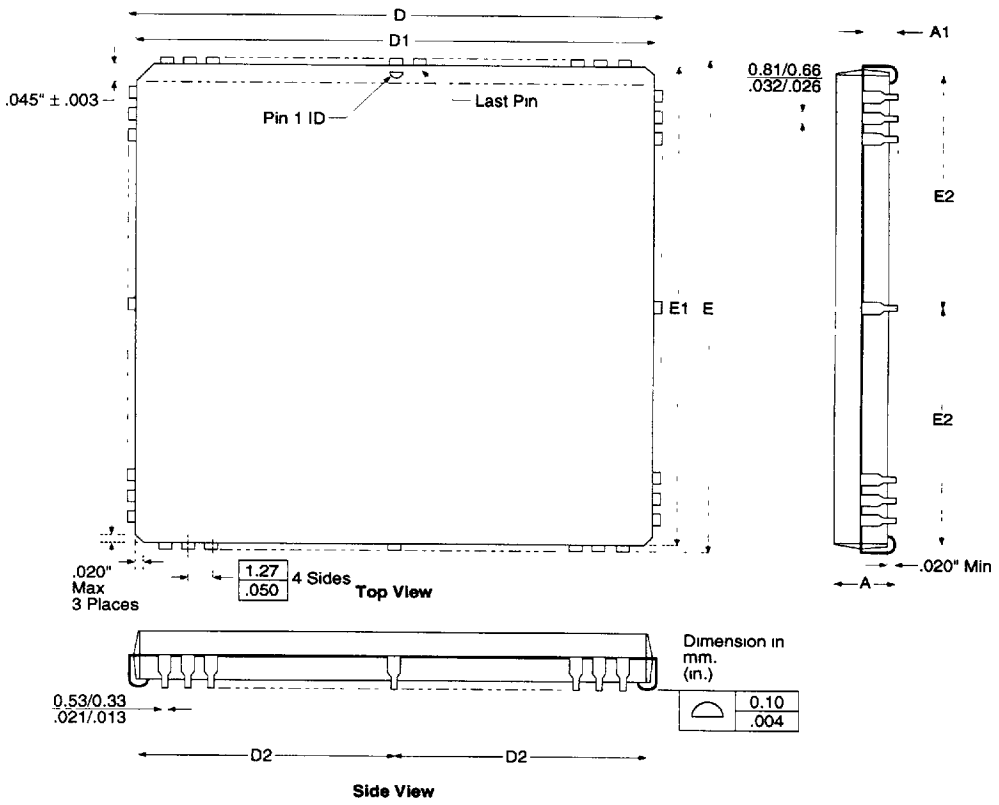
PLCC Package Dimensions



Package Dimension Table		PLCC/84L		PLCC/68L		PLCC/52L	
		inch	mm	inch	mm	inch	mm
A	max	.200	5.08	.200	5.08	.200	5.08
A1	min	.090	2.28	.090	2.28	.090	2.28
	max	.130	3.30	.130	3.30	.130	3.30
D	min	1.185	30.09	.985	25.01	.785	19.93
	max	1.195	30.35	.995	25.27	.795	20.19
D1	min	1.150	29.21	.950	24.13	.750	19.05
	max	1.158	29.41	.958	24.33	.756	19.20
D2	min	.545	13.84	.445	11.30	.345	8.76
	max	.565	14.35	.465	11.81	.365	9.27
E	min	1.185	30.09	.985	25.01	.785	19.93
	max	1.195	30.35	.995	25.27	.795	20.19
E1	min	1.150	29.21	.950	24.13	.750	19.05
	max	1.158	29.41	.958	24.33	.756	19.20
E2	min	.545	13.84	.445	11.30	.345	8.76
	max	.565	14.35	.465	11.81	.365	9.27

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Pinout

Pinout information for the device and package combinations currently available is given on the following pages. Contact I-Cube Marketing for data on other devices and packages.

IQ96 [MQUAD®, PQFP, and TQFP Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	TMS	37	$\overline{OE}_1$	73	P048	109	$\overline{OE}_3$
2	TDO	38	P022	74	P049	110	P074
3	TCK	39	P023	75	VDD	111	Vss.PAD
4	VDD	40	P024	76	Vss.PAD	112	VDD
5	TRST*	41	P025	77	P050	113	P075
6	Vss.PAD	42	Vss.PAD	78	P051	114	P076
7	P000	43	VDD	79	P052	115	Vss.PAD
8	P001	44	P026	80	P053	116	P077
9	P002	45	P027	81	Vss.PAD	117	VSS
10	P003	46	P028	82	P054	118	VDD.PAD
11	Vss.PAD	47	P029	83	P055	119	P078/CA_0
12	P004	48	Vss.PAD	84	P056	120	P079/CA_1
13	P005	49	P030	85	P057	121	P080/CA_2
14	P006	50	P031	86	Vss.PAD	122	P081/CA_3
15	P007	51	P032	87	P058	123	P082/CA_4
16	VDD.PAD	52	P033	88	P059	124	Vss.PAD
17	Vss.PAD	53	Vss.PAD	89	VDD.PAD	125	P083/CA_5
18	P008	54	VDD.PAD	90	P060	126	P084/CA_6
19	P009	55	P034	91	P061	127	P085/RA_0
20	P010	56	P035	92	Vss.PAD	128	Vss.PAD
21	P011	57	P036	93	P062	129	P086/RA_1
22	Vss.PAD	58	P037	94	P063	130	P087/RA_2
23	P012	59	Vss.PAD	95	P064	131	P088/RA_3
24	P013	60	P038	96	P065	132	P089/RA_4
25	P014	61	P039	97	Vss.PAD	133	P090/RA_5
26	P015	62	P040	98	P066	134	P091/RA_6
27	Vss.PAD	63	P041	99	P067	135	ICLK
28	P016	64	VDD.PAD	100	P068	136	Vss.PAD
29	P017	65	Vss.PAD	101	P069	137	VDD.PAD
30	P018	66	P042	102	VDD.PAD	138	OCLK
31	P019	67	P043	103	VSS	139	Vss.PAD
32	VDD.PAD	68	P044	104	P070	140	P092/C_0
33	VSS	69	P045	105	P071	141	P093/C_1
34	P020	70	VSS	106	P072	142	P094/$\overline{WE}$
35	P021	71	P046	107	P073	143	P095/$\overline{STROBE}$
36	$\overline{OE}_0$	72	P047	108	$\overline{OE}_2$	144	TDI

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IQ64B [MQUAD PQFP, and TQFP Package Pinout]

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	TMS	26	$\overline{OE}_0$	51	P031	76	V_{DD}
2	TDO	27	$\overline{OE}_1$	52	P032	77	V_{SS}
3	TCK	28	P014	53	P033	78	P048/CA_0
4	V_{DD}	29	P015	54	P034	79	P049/CA_1
5	TRST*	30	V_{SS}.PAD	55	P035	80	P050/CA_2
6	V_{SS}.PAD	31	P016	56	P036	81	P051/CA_3
7	P000	32	P017	57	P037	82	P052/CA_4
8	P001	33	V_{SS}.PAD	58	V_{SS}.PAD	83	V_{SS}.PAD
9	V_{SS}.PAD	34	V_{DD}.PAD	59	P038	84	P053/CA_5
10	P002	35	P018	60	P039	85	P054/RA_0
11	P003	36	P019	61	P040	86	V_{SS}.PAD
12	V_{DD}.PAD	37	P020	62	P041	87	P055/RA_1
13	V_{SS}.PAD	38	P021	63	V_{SS}.PAD	88	P056/RA_2
14	P004	39	V_{SS}.PAD	64	P042	89	P057/RA_3
15	P005	40	P022	65	P043	90	P058/RA_4
16	P006	41	P023	66	P044	91	P059/RA_5
17	P007	42	P024	67	P045	92	ICLK
18	V_{SS}.PAD	43	P025	68	V_{SS}.PAD	93	V_{SS}.PAD
19	P008	44	V_{SS}.PAD	69	P046	94	V_{DD}.PAD
20	P009	45	P026	70	P047	95	OCLK
21	P010	46	P027	71	V_{SS}.PAD	96	P060/C_0
22	P011	47	P028	72	V_{DD}.PAD	97	P061/C_1
23	V_{SS}	48	P029	73	V_{SS}	98	P062/$\overline{WE}$
24	P012	49	V_{SS}	74	$\overline{OE}_2$	99	P063/$\overline{STROBE}$
25	P013	50	P030	75	$\overline{OE}_3$	100	TDI

IQ64B [PLCC Package] Pinout

Note:

There are no separate power and ground pads for I/O buffer drivers for this package.

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P005	22	P056/RA_2	43	V_{SS}	64	P021
2	P004	23	P055/RA_1	44	P041	65	P020
3	V_{SS}	24	V_{SS}	45	P040	66	P019
4	P003	25	P054/RA_0	46	P039	67	P018
5	P002	26	P053/CA_5	47	P038	68	V_{SS}
6	P001	27	P052/CA_4	48	P037	69	P017
7	P000	28	P051/CA_3	49	P036	70	P016
8	TRST*	29	P050/CA_2	50	P035	71	V_{SS}
9	TCK	30	P049/CA_1	51	P034	72	P015
10	TDO	31	P048/CA_0	52	P033	73	P014
11	TMS	32	V_{DD}	53	P032	74	$\overline{OE}_1$
12	TDI	33	$\overline{OE}_3$	54	P031	75	$\overline{OE}_0$
13	P063/$\overline{STROBE}$	34	$\overline{OE}_2$	55	P030	76	P013
14	P062/$\overline{WE}$	35	V_{SS}	56	P029	77	P012
15	P061/C_1	36	V_{DD}	57	P028	78	V_{DD}
16	P060/C_0	37	P047	58	P027	79	P011
17	OCLK	38	P046	59	P026	80	P010
18	ICLK	39	P045	60	P025	81	P009
19	P059/RA_5	40	P044	61	P024	82	P008
20	P058/RA_4	41	P043	62	P023	83	P007
21	P057/RA_3	42	P042	63	P022	84	P006

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IQ48 [PQFP, TQFP Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	NC	21	NC	41	NC	61	NC
2	TCK	22	TMS	42	OCLK	62	TDI
3	TRST*	23	P012	43	ICLK	63	P036/CA_3
4	P000	24	P013	44	P024	64	P037/CA_4
5	P001	25	P014	45	P025	65	P038/CA_5
6	P002	26	V_{SS}.PAD	46	P026	66	V_{SS}.PAD
7	V_{SS}.PAD	27	P015	47	V_{SS}.PAD	67	P039/RA_0
8	P003	28	P016	48	P027	68	P040/RA_1
9	P004	29	P017	49	P028	69	P041/RA_2
10	P005	30	V_{DD}.PAD	50	P029	70	V_{DD}.PAD
11	V_{DD}.PAD	31	V_{DD}	51	V_{DD}.PAD	71	V_{DD}
12	P006	32	P018	52	P030	72	P042/RA_3
13	P007	33	P019	53	P031	73	P043/RA_4
14	P008	34	P020	54	P032	74	P044/RA_5
15	V_{SS}.PAD	35	V_{SS}.PAD	55	V_{SS}.PAD	75	V_{SS}.PAD
16	P009	36	P021	56	P033/CA_0	76	P045/C_0
17	P010	37	P022	57	P034/CA_1	77	P046/$\overline{WE}$
18	P011	38	P023	58	P035/CA_2	78	P047/$\overline{STROBE}$
19	$\overline{OE}_0$	39	V_{SS}	59	TDO	79	V_{SS}
20	NC	40	NC	60	NC	80	NC

IQ48 [PLCC Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P005	18	V_{DD}	35	P029	52	V_{DD}
2	P004	19	V_{DD}.PAD	36	P028	53	V_{DD}.PAD
3	P003	20	P041/RA_2	37	P027	54	P017
4	V_{SS}.PAD	21	P040/RA_1	38	V_{SS}.PAD	55	P016
5	P002	22	P039/RA_0	39	P026	56	P015
6	P001	23	P038/CA_5	40	P025	57	P014
7	P000	24	P037/CA_4	41	P024	58	P013
8	TRST*	25	P036/CA_3	42	ICLK	59	P012
9	TCK	26	TDI	43	OCLK	60	TMS
10	V_{SS}	27	TDO	44	V_{SS}	61	$\overline{OE}_0$
11	P047/$\overline{STROBE}$	28	P035/CA_2	45	P023	62	P011
12	P046/$\overline{WE}$	29	P034/CA_1	46	P022	63	P010
13	P045/C_0	30	P033/CA_0	47	P021	64	P009
14	V_{SS}.PAD	31	V_{SS}.PAD	48	V_{SS}.PAD	65	V_{SS}.PAD
15	P044/RA_5	32	P032	49	P020	66	P008
16	P043/RA_4	33	P031	50	P019	67	P007
17	P042/RA_3	34	P030	51	P018	68	P006

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.B [PQFP Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	14	TMS	27	OCLK	40	P022/CA_3
2	TCK	15	P007	28	ICLK	41	P023/CA_4
3	TRST*	16	P008	29	P015	42	P024/RA_0
4	P000	17	P009	30	P016	43	P025/RA_1
5	P001	18	P010	31	V_{SS}.PAD	44	P026/RA_2
6	V_{SS}.PAD	19	V_{DD}.PAD	32	P017	45	V_{DD}.PAD
7	P002	20	V_{DD}	33	P018	46	V_{DD}
8	P003	21	P011	34	V_{SS}.PAD	47	P027/RA_3
9	V_{SS}.PAD	22	V_{SS}.PAD	35	P019/CA_0	48	P028/RA_4
10	P004	23	P012	36	P020/CA_1	49	V_{SS}.PAD
11	P005	24	P013	37	P021/CA_2	50	P029/C_0
12	P006	25	P014	38	TDO	51	P030/$\overline{WE}$
13	$\overline{OE}_0$	26	V_{SS}	39	TDI	52	P031/$\overline{STROBE}$

B [PLCC Package] Pinout

Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	P002	14	V_{DD}	27	P018	40	V_{DD}
2	V_{SS}.PAD	15	V_{DD}.PAD	28	P017	41	V_{DD}.PAD
3	P001	16	P026/RA_2	29	V_{SS}.PAD	42	P010
4	P000	17	P025/RA_1	30	P016	43	P009
5	TRST*	18	P024/RA_0	31	P015	44	P008
6	TCK	19	P023/CA_4	32	ICLK	45	P007
7	V_{SS}	20	P022/CA_3	33	OCLK	46	TMS
8	P047/$\overline{STROBE}$	21	TDI	34	V_{SS}	47	$\overline{OE}_0$
9	P030/$\overline{WE}$	22	TDO	35	P014	48	P006
10	P029/C_0	23	P021/CA_2	36	P013	49	P005
11	V_{SS}.PAD	24	P020/CA_1	37	P012	50	P004
12	P028/RA_4	25	P019/CA_0	38	V_{SS}.PAD	51	V_{SS}.PAD
13	P027/RA_3	26	V_{SS}.PAD	39	P011	52	P003

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Configuring IQ Devices

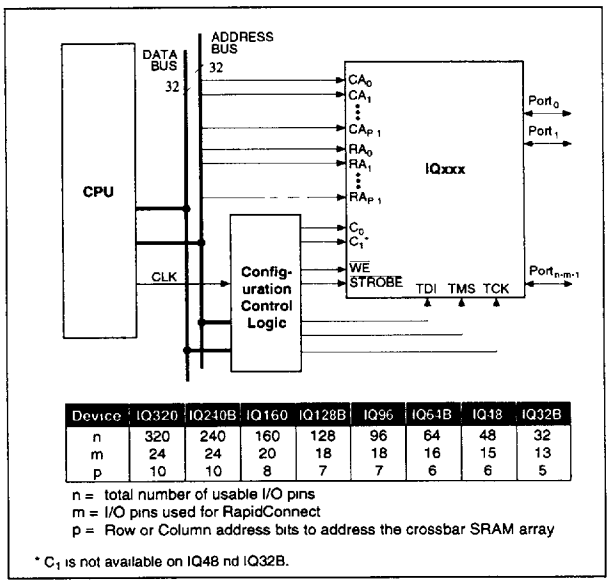
The IQ devices in this family offer two configuration modes, a JTAG-based serial mode and a much faster mode called RapidConnect. Table 8 shows the number of JTAG cycles, configuration time and bit stream size for full configuration of IQ devices. In addition, the number of JTAG cycles and configuration time to Make or Break a single connection and change attributes of one or more I/Os is shown in the table.

Operation	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
Complete Configuration [All I/O ports plus all crossbar switches]	68,000 (3.4ms)	54,000 (2.7ms)	22,000 (1.1ms)	18,000 (0.72ms)	10,000 (0.4ms)	8,000 (0.32ms)	3,000 (0.15ms)	2,500 (.125ms)
I/O/B functions for one or more I/O ports	1306 (65.3µs)	1306 (65.3µs)	666 (33.3µs)	666 (33.3µs)	410 (16.4µs)	410 (16.4µs)	218 (8.72µs)	218 (8.72µs)
Make or Break a single connection using JTAG	346 (17.3µs)	346 (17.3µs)	186 (9.3µs)	186 (9.3µs)	122 (4.88µs)	122 (4.88µs)	74 (2.96µs)	74 (2.96µs)
Bitstream size for Complete Configuration	17 KB	13.5 KB	5.5 KB	4.5 KB	2.5 KB	2 KB	0.75 KB	0.625 KB

Table 8: JTAG Cycles, Time (for 20 MHz JTAG Clock) and Bitstream Size for Configuration

Incremental Configuration Using RapidConnect

The RapidConnect is a special mode that allows fast switching of connections by directly accessing the crossbar SRAM for writing. By using RapidConnect, a single connection can be changed (made or broken) in 30 ns. This feature is very useful for real-time switching applications. Figure 2 shows a microprocessor interface for real-time configuration of the IQ devices.



Device	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
n	320	240	160	128	96	64	48	32
m	24	24	20	18	18	16	15	13
p	10	10	8	7	7	6	6	5

n = total number of usable I/O pins
m = I/O pins used for RapidConnect
p = Row or Column address bits to address the crossbar SRAM array

* C_1 is not available on IQ48 nd IQ32B.

Figure 2: Target System Interface in RapidConnect Mode

The number of ports that can be addressed (switched) using the RapidConnect mode are:

Device	IQ320	IQ240B	IQ160	IQ128B	IQ96	IQ64B	IQ48	IQ32B
# of ports	296	216	140	102	78	48	33	19

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Component Availability and Ordering Information

The following table lists the IQ devices and the different package options, speed grades and operating temperature ranges that are currently available. Contact I-Cube Marketing for more up-to-date information on product availability.

Package	Pins	52			68	80		84	100			144			184		208		304	391	416
	Type	PQFP	TQFP	PLCC	PLCC	PQFP	TQFP	PLCC	PQFP	MQUAD	TQFP	PQFP	MQUAD	TQFP	PQFP	MQUAD	PQFP	MQUAD	MQUAD	PPGA	PBGA
	Code	PQ52	TQ52	J52	J68	PQ80	TQ80	J84	PQ100	MQ100	TQ100	PQ144	MQ144	TQ144	PQ184	MQ184	PQ208	MQ208	MQ304	PP391	PB416
IQ320	-20																			C I	C I
	-15																			C I	C I
	-12																			C	C
IQ240B	-20																		C I		
	-15																		C I		
IQ160	-20																C I	C I			
	-15																C I	C I			
	-12																C I	C I			
	-10																C	C			
IQ128B	-20														C I	C I					
	-15														C I	C I					
	-12														C I	C I					
	-10														C	C					
IQ96	-15											C I	C I	C I							
	-12											C I	C I	C I							
	-10											C I	C I	C I							
	-6											C	C	C							
IQ64B	-15							C I	C I	C I	C I										
	-12							C I	C I	C I	C I										
	-10							C I	C I	C I	C I										
	-6							C	C	C	C										
IQ48	-12				C I	C I	C I														
	-10				C I	C I	C I														
	-7				C I	C I	C I														
	-5				C	C	C														
IQ32B	-12	C I	C I	C I																	
	-10	C I	C I	C I																	
	-7	C I	C I	C I																	
	-5	C	C	C																	

C = Commercial = 0° to +70° C
I = Industrial = -40° to +85° C

Table 9: Current Component Availability

IQ XXXX-SS PP ### T

Number of Usable I/O Ports

Speed Grade

Package Code

PQ - Plastic Quad Flat Pack
MQ - MQUAD®
PP - Plastic Pin Grid Array
PB - Plastic Ball Grid Array
J - PLCC
TQ - Thin Plastic Quad Flat Package

Package Pin Count

Temperature Range

Blank - Commercial (0°C to 70°C)
I - Industrial (-40°C to 85°C)

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