Integrated Circuit Systems, Inc.

ICS9161

Preliminary Information

Dual Programmable Graphics Frequency Generator

Features

- Pin for pin and function compatible with ICD2061A
- Dual programmable graphics clock generator
- Memory and video clocks are individually programmable on-the-fly
- Ideal for designs where multiple or varying frequencies are required
- Increased frequency resolution from optional pre-divide by 2 on the M counter
- Output enable feature available for tri-stating outputs
- Independent clock outputs range from 390 kHz to 120 MHz
- Operation up to 140 MHz available
- Power-down capabilities
- Low power, high speed 0.8 µ CMOS technology
- Glitch-free transitions
- Available in 16 pin SOIC or PDIP package

General Description

The ICS9161 is a fully programmable graphics clock generator. It can generate user specified clock frequencies using an externally generated input reference or a single crystal. The output frequency is programmed by entering a 24 bit digital word through the serial port.

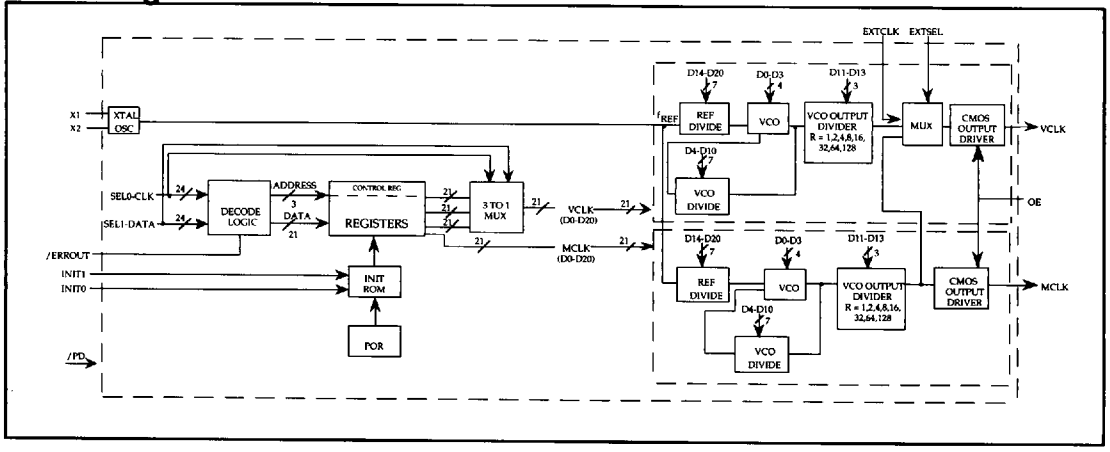
Two fully user-programmable phase-locked loops are offered in a single package. One PLL is designed to drive the memory clock, while the second drives the video clock. The outputs may be changed on-the-fly to any desired frequency between 390 kHz and 120 MHz. The ICS9161 is ideally suited for any design where multiple or varying frequencies are required.

This part is ideal for graphics applications. It generates low jitter, high speed pixel clocks. It can be used to replace multiple, expensive high speed crystal oscillators. The flexibility of the device allows it to generate non-standard graphics clocks.

The ICS9161 is also ideal in disk drives. It can generate zone clocks for constant density recording schemes. The low profile, 16 pin SOIC or PDIP package and low jitter outputs are especially attractive in board space critical disk drives.

The leader in the area of multiple output clocks on a single chip, ICS has been shipping graphics frequency generators since October, 1990, and is constantly improving the phase locked loop. The ICS9161 incorporates a patented fourth generation PLL that offers the best jitter performance available.

Block Diagram



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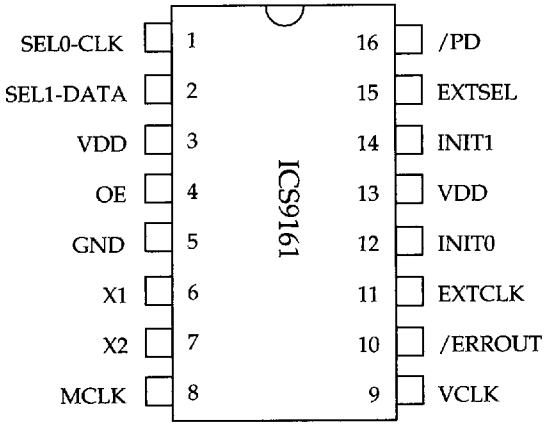
Pin Configuration



Pin Description

Pin Name	Pin #	Description
SEL0-CLK	1	Clock input in serial programming mode Clock select pin in operating mode
SEL1-DATA	2	Data input in serial programming mode Clock select pin in operating mode
AVDD	3	Power
OE	4	Tri-states outputs when low
GND	5	Ground
X1	6	Crystal input
X2	7	Crystal output
MCLK	8	Memory clock output
VCLK	9	Video clock output
/ERROUT	10	Output low signals an error in the serially programmed word
EXTCLK	11	External clock input
INIT0	12	Selects initial power-up conditions, LSB
VDD	13	Power
INIT1	14	Selects initial power-up conditions, MSB
EXTSEL	15	Selects external clock input (EXTCLK) as VCLK output
/PD	16	Power-down pin, active low

Register Definitions

The register file consists of the following six registers:

Register Addressing

Address	Register	Definition
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory Register
100	PWRDWN	Divisor for Power-down mode
110	CNTL REG	Control Register

The ICS9161 places the three video clock registers and the memory clock register in a known state upon power-up. The registers are initialized based on the state of the INIT1 and INIT0 pins at application of power to the device . The INIT pins must ramp up with VDD if a logical 1 on either pin is required. These input pins are internally pulled down and will default to a logical 0 if left unconnected.

The registers are initialized as follows:

Register Initialization

INIT1	INIT0	MREG	REG0	REG1	REG2
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	40.000	28.322	28.322
1	1	56.644	40.000	50.350	50.350

Register Selection

When the ICS9161 is operating, the video clock output is controlled with a combination of the SEL0, SEL1, /PD, and OE pins. The video clock is also multiplexed to an external clock (EXTCLK) which can be selected with the EXTSEL pin. The VCLK Selection Table shows how VCLK is selected.

VCLK Selection

OE	/PD	EXTSEL	SEL1	SEL0	VCLK
0	x	x	x	x	Tri-State
1	0	x	x	x	Forced High
1	1	x	0	0	REG0
1	1	x	0	1	REG1
1	1	0	1	0	EXTCLK
1	1	1	1	x	REG2
1	1	x	1	1	REG2

As seen in the table above, OE acts to tri-state the output. The /PD pin forces the VCLK signal high while powering down the part. The EXTCLK pin will only be multiplexed in when EXTSEL and SEL0 are logic 0 and SEL1 is a logic 1.

The memory clock outputs are controlled by /PD and OE as follows:

MCLK Selection

OE	/PD	MCLK
0	x	Tri-State
1	1	MREG
1	0	PWRDWN

The Clock Select pins SEL0 and SEL1 have two purposes. In serial programming mode, these pins act as the clock and data pins. New data bits come in on SEL1 and these bits are clocked in by a signal on SEL0. While these pins are acquiring new information, the VCLK signal remains unchanged. When SEL0 and SEL1 are acting as register selects, a timeout interval is required to determine whether the user is selecting a new register or wants to program the part. During this initial timeout, the VCLK signal remains at its previous frequency. At the end of this timeout interval, a new register is selected. A second timeout interval is required to allow the VCO to settle to its new value. During this period of time, typically 5 msec, the input reference signal is multiplexed to the VCLK signal.

When MCLK or the active VCLK register is being reprogrammed, then the reference signal is multiplexed glitch-free to the output during the first timeout interval. A second timeout interval is also required to allow the VCO to settle. During this period, the reference signal is multiplexed to the appropriate output signal.

Control Register Definitions

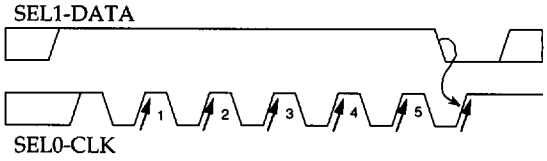
The control register allows the user to adjust various internal options. The register is defined as follows:

Bit	Bit Name	Default Value	Description
9	C5	0	This bit determines which power-down mode the /PD pin will implement. Power-down mode 1, C5 = 0, forces the MCLK signal to be a function of the power-down register. Power-down mode 2, C5 = 1, turns off the crystal and disables all outputs.
8	C4	0	This bit determines which clock is multiplexed to VCLK during frequency changes. C4 = 0 multiplexes the reference frequency to the VCLK output. C4 = 1 multiplexes MCLK to the VCLK output for applications where the graphics controller cannot run as slow as f_{REF}.
7	C3	0	This bit determines the length of the timeout interval. The timeout interval is derived from the MCLK VCO. If this VCO is programmed to certain extremes, the timeout interval maybe too short. C3 = 0, normal timeout. C3 = 1, doubled timeout interval.
6	C2	0	Reserved, must be set to 0.
5	C1	1	This bit adjusts the duty cycle. C1 = 0 causes a 1ns decrease in output high time. C1 = 1 causes no adjustment. If the load capacitance is high, the adjustment can bring the duty cycle closer to 50%.
4	C0	0	Reserved, must be set to 0.
3	NS2	0	Acts on register 2. NS2 = 0 prescales the N counter by 2. NS2 = 1 prescales the P counter value to 4.
2	NS1	0	Acts on register 1. NS1 = 0 prescales the N counter by 2. NS1 = 1 prescales the P counter value to 4.
1	NS0	0	Acts on register 0. NS0 = 0 prescales the P counter by 2. NS0 = 1 prescales the P counter value to 4.

Serial Programming Architecture

The pins SEL0 and SEL1 perform the dual functions of selecting registers and serial programming. In serial programming mode, SEL0 acts as a clock pin while SEL1 acts as the data pin. The ICS9161-01 may not be serially programmed when in power-down mode.

In order to program a particular register, an unlocking sequence must occur. The unlocking sequence is detailed in the following timing diagram:



The unlock sequence consists of at least 5 low-to-high transitions of CLK while data is high, followed immediately by a single low-to-high transition while data is low. Following this unlock sequence, data can be loaded into the serial data register.

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. The watchdog timer ensures that successive rising edges of CLK and DATA do not violate the timeout specification of 2ms. If a timeout occurs, the lock mechanism is reset and the data in the serial data register is ignored.
Since the VCLK registers are selected by the SEL0 and SEL1 pins, and since any change in their state may affect the output frequency, new data input on the selection bits is only permitted to pass through the decode logic after the watchdog timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to occur without affecting the current register selection.

Serial Data Register

The serial data is clocked into the serial data register in the order described in figure 1 below (Serial Data Timing).

The serial data is sent as follows: An individual data bit is sampled on the rising edge of CLK. The complement of the data bit must be sampled on the previous falling edge of CLK. The setup and hold time requirements must be met on both CLK edges. For specifics on timing, see the timing diagrams on pages 10, 11, and 12.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit. A total of 24 bits must always be loaded into the serial data register or an error is issued. Following the entry of the last data bit, a stop bit or load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The unlocking mechanism then resets itself following the load. Only after a timeout period are the SEL0 and SEL1 pins allowed to return to a register selection function.

The serial data register is exactly 24 bits long, enough to

	Data Bits																				Address Bits			
	LBS																		MBS		LBS		MBS	
START	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	A0	A1	A2	STOP
BIT#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	BIT#
VCO Prog-Word	M'0	M'1	M'2	M'3	M'4	M'5	M'6	R0	R1	R2	N'0	N'1	N'2	N'3	N'4	N'5	N'6	I0	I1	12	13	A0	A1	0	VCO Prog-Word
CNTL Reg	0	0	0	0	0	0	0	0	0	0	0	0	PS0	PS1	PS2	C0	C1	C2	C3	C4	C5	0	1	1	CNTL Reg
PWRDWN Reg	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P0	P1	P2	P3	0	0	1	PWRDWN Reg

Figure 1 - Serial Data Timing

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accept the data being sent. The stop bit acts as a load command that passes the contents of the Serial Data Register into the register indicated by the three address bits. If a stop bit is not received after the serial register is full, and more data is sent, all data in the register is ignored and an error issued. If correct data is received, then the unlocking mechanism rearms, all data in the serial data register is ignored, and an error is issued.

/ERROUT Operation

Any error in programming the ICS9161 is signaled by /ERROUT. When the pin goes low, an error has been detected. It stays low until the next unlock sequence. The signal is invoked for any of the following errors: incorrect start bit, incorrect data encoding, incorrect length of data word, and incorrect stop bit.

Programming the ICS9161

The ICS9161 has a wide operating range, but it is recommended that it is operated within the following limits:

$1\ MHz < F_{REF} < 60\ MHz$	F_{REF} = Input Reference Frequency
$200\ KHz < F_{REF/M} < 5\ MHz$	M = Reference divide 3 to 129
$50\ MHz < F_{VCO} < 120\ MHz$	F_{VCO} = VCO output frequency
$F_{CLK} \leq 120\ MHz$	F_{CLK} = output frequency

The frequency of the programmable oscillator F_{VCO} is determined by the following fields:

Field	# of Bits
Index (I)	4
N counter value (N')	7
Mux (R)	3
M counter value (M')	7

Where the least significant bit is the last bit of M and the most significant bit is the first bit of I.

The equations used to determined the oscillator frequency are:

$$N = N' + 3 \qquad M = M' + 2$$

$$F_{VCO} = \text{Prescale} \cdot N/M \cdot F_{CLK}$$

where $3 \leq M \leq 129$ and $4 \leq N \leq 130$

and prescale = 2 or 4, as set in the control register

The value of F_{VCO} must remain between 50 MHz and 120 MHz. As a result, for output frequencies below 50MHz, F_{VCO} must be brought into range. To achieve this, an output divisor is selected by setting the values of the Mux Field (R) as follows:

Output Divisor

R	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Unlike the ICD2061A, the ICS9161's VCO does not require tuning to place it in certain ranges. The ICS9161's VCO will operate from 50 MHz to 120 MHz without adjusting the VCO gain. However, to maintain compatability, the I bits are programmed as in the ICD2061A.

These bits are dummy bits except for the following two cases:

Index Field (I)

I	VCLK F_{VCO}	MCLK F_{VCO}
1110	Turn off VCLK	50-120 MHz
1111	Mux MCLK to VLCK	50-120 MHz

When the index field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. This is done in an effort to reduce jitter, which may increase when VCOs run at 2^n multiples of one another. If the two outputs must be multiples of one another, it is best to mux MCLK over to the output of the VCLK VCO, and to

power-down the VCLK VCO. The multiplexed frequency will be divided down by the correct divisor (M) and output on VCLK.

Power Management Issues

Power-down mode 1

The ICS9161 contains a mechanism to reduce the quiescent power when stand-by operation is desired. Power-down mode 1 is invoked by pulling /PD low and having the proper CNTL register bit set to zero. In this mode, VCOs are shut down, the VCLK output is forced high, and the MCLK output is set to a user-defined low frequency value to refresh dynamic RAM.

The power-down MCLK value is determined by the following equation:

$MCLK_{PD} = F_{REF}$ / (PWRDWN register divisor value)

The power-down register divisor is determined according to the 4-bit word programmed into the PWRDWN register (see table below).

Power-down mode 2

When there is no need for any output during power-down, an alternate mode is available which will completely shut down all outputs and the reference oscillator, but still preserves all register contents. Power-down mode 2 is invoked by first programming the power-down bit in the CNTL register and then pulling the /PD pin low.

The /PD pin

The /PD pin has a standard internal pull-up resistor during normal operation. When the chip goes into power-down mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which reduces power consumption. If the /PD pin is allowed to float after it has been pulled down, the weak pull-up will bring the signal high and allow the device to resume operation.

Power Down Register Table

PWRDWN bits P3	P2	P1	P0	PWRDWN Register Value	Power-down Divisor	$MCLK_{PD}$ (f_{REF}=14.31818)
0	0	0	0	0	n/a	n/a
0	0	0	1	1	32	447.4 KHz
0	0	1	0	2	30	477.3 KHz
0	0	1	1	3	28	511.4 KHz
0	1	0	0	4	26	550.7 KHz
0	1	0	1	5	24	596.6 KHz
0	1	1	0	6	22	650.8 KHz
0	1	1	1	7	20	715.9 KHz
1	0	0	0	8 (default)	18	795.5 KHz
1	0	0	1	9	16	894.9 KHz
1	0	1	0	A	14	1.02 MHz
1	0	1	1	B	12	1.19 MHz
1	1	0	0	C	10	1.43 MHz
1	1	0	1	D	8	1.79 MHz
1	1	1	0	E	6	2.39 MHz
1	1	1	1	F	4	3.58 MHz

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Absolute Maximum Ratings

VDD referenced to GND..... 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation..... 0.5 Watts

Note: Stresses above those listed under Absolute Maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Electrical Characteristics

(VDD = +5V ± 5%, 0°C ≤ $T_{AMBIENT}$ ≤ +70°C unless otherwise stated)

Device Specifications

Maximum Ratings

Name	Description	Min	Max	Units
VDD	Supply voltage relative to GND	-0.5	7.0	Volts
V_{IN}	Input voltage with respect to GND	-0.5	VDD + 0.5	Volts
T_{OPER}	Operating temperature	0	+70	°C
T_{STOR}	Storage temperature	-65	+150	°C
T_{SOL}	Max soldering temperature (10 sec)		+260	°C
T_j	Junction temperature		+125	°C
P_{DISS}	Package power dissipation		350	mWatts

DC Characteristics

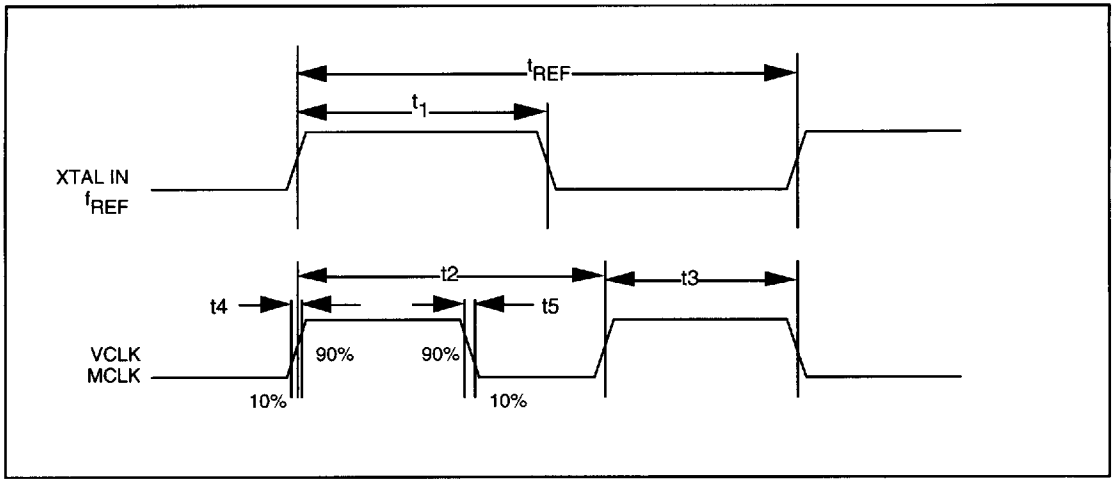
Name	Description	Min	Typ	Max	Units	Conditions
V_{IH}	High level input voltage	2.0			V	
V_{IL}	Low level input voltage			0.8	V	
V_{OH}	High level CMOS ouput voltage	3.84			V	I_{OH} = -4 ma
V_{OL}	Low level output voltage			0.4	V	I_{OL} = 4 ma
I_{IH}	Input high current			100	µa	V_{IH} = 5.25 V
I_{IL}	Input low current			-250	µa	V_{IL} = 0V
I_{OZ}	Output leakage current			10	µa	(tri-state)
I_{DD}	Power supply current	15		65	ma	
I_{DD-TYP}	Power supply current (typical)		35		ma	@60 MHz
I_{ADD}	Analog power supply current			10	ma	
I_{PD1}	Power-down current (Mode 1)		6	7.5	ma	
I_{PD2}	Power-down current (Mode 2)		25	50	µa	
C_{IN}	Input capacitance			10	pf	

AC Characteristics

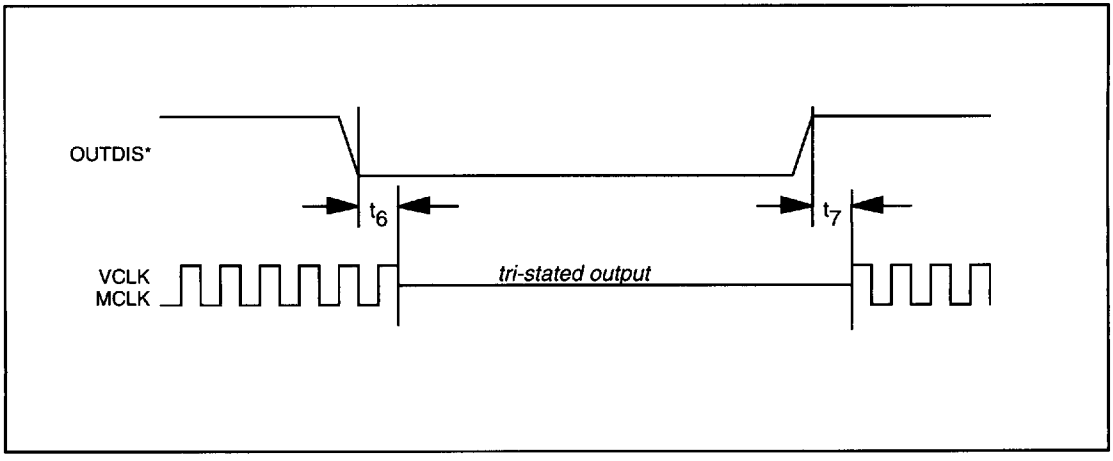
Symbol	Name	Description	Min	Typ	Max	Units
f_{REF}	Reference frequency	Reference oscillator value (note 1)	1	14.31818	60	Mhz
t_{REF}	Reference period	$1/f_{REF}$	16.6		1000	ns
t_1	Input duty cycle	Duty cycle for the input oscillator defined as t_1/t_{REF}	25%		75%	
t_2	Output clock periods	Output oscillator values	8.33 (120 MHz)		2564 (390 MHz)	ns
t_3	Output duty cycle	Duty cycle for the output oscillators (note 2)	45%		55%	
t_4	Rise times	Rise time for the ouput oscillators into a 25 pf load			3	ns
t_5	Fall times	Fall time for the output oscillator into a 25 pf load			3	ns
t_{freq1}	freq1 output	Old frequency output				
t_{freq2}	freq2 ouput	New frequency output				
t_A	f_{REF} mux time	Time clock output remains high while output muxes to reference frequency	$^{0.5}t_{REF}$		$^{1.5}t_{REF}$	ns
$t_{timeout}$	Timeout internal	Interval for serial programming and for VCO changes to settle (note 3)	2	5	10	ns
t_B	t_{freq2} muxtime	Time clock ouput remains high while output muxes to new frequency value	$^{0.5}t_{REF}$	$^{1.5}t_{REF}$		ns
t_6	Tri-state	Time for the ouput oscillators to go into tri-state mode after OUTDIS - signal assertion	0		12	ns
t_7	CLK valid	Time for the output oscillators to recover from tri-state mode after OUTDIS -signal goes high	0		12	ns
t_8	Power-Down	Time for power-down mode of operation to take effect			12	ns
t_9	Power-Up	Time for recovery from power-down mode of operation			12	ns
t_{10}	MCLKOUT high	Time for MCLK to go high after PWRDWN is asserted high	0		t_{PWRDWN}	ns
t_{11}	MCLKOUT delay	Delay of MCLK prior to f_{MCLK} signal at output	$^{0.5}t_{MCLK}$		$^{1.5}t_{MCLK}$	ns
t_{serclk}		Clock period of serial clock	$2 \cdot t_{REF}$		2	msec
t_{SU}		Setup time	20			ns
t_{HD}		Hold time	10			ns
t_{ldcmd}		Load command	0		t_1+30	ns

NOTES

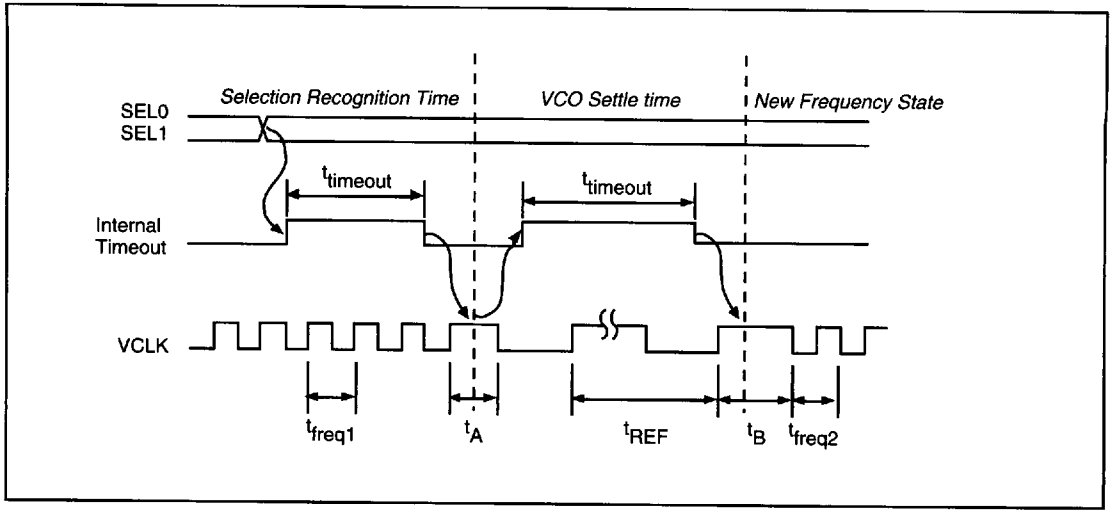
1. For reference frequencies other than 14.81818 MHz, the pre-loaded ROM frequencies will shift proportionally.
2. Duty cycle is measured at CMOS threshold levels. At 5 volts, V_{TH} = 2.5 volts).
3. If the interval is too short, see the timeout interval section in the control register definition.



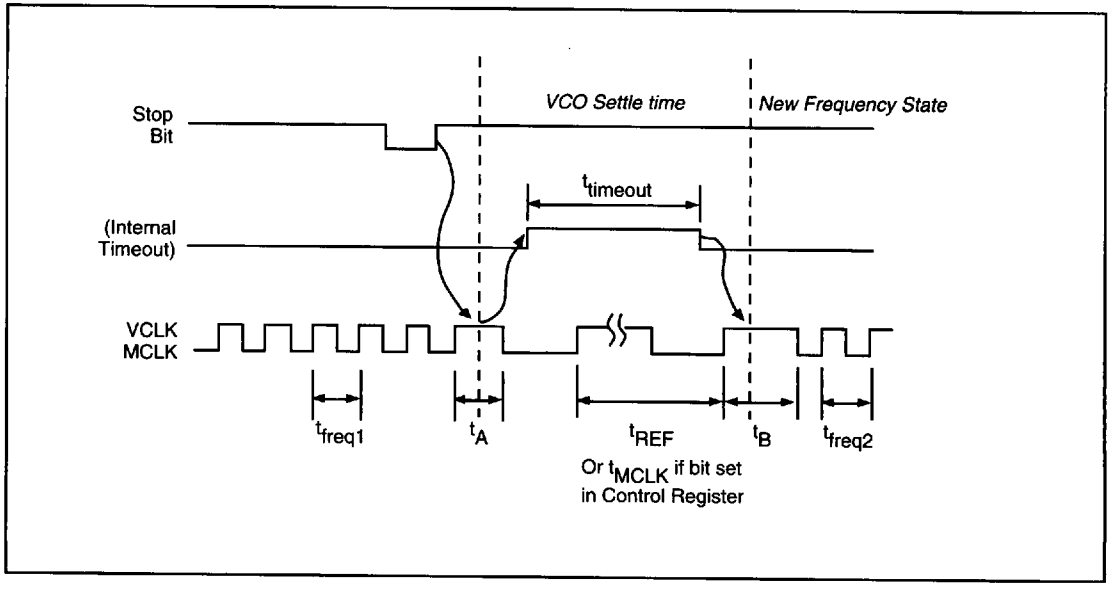
Rise and Fall Times



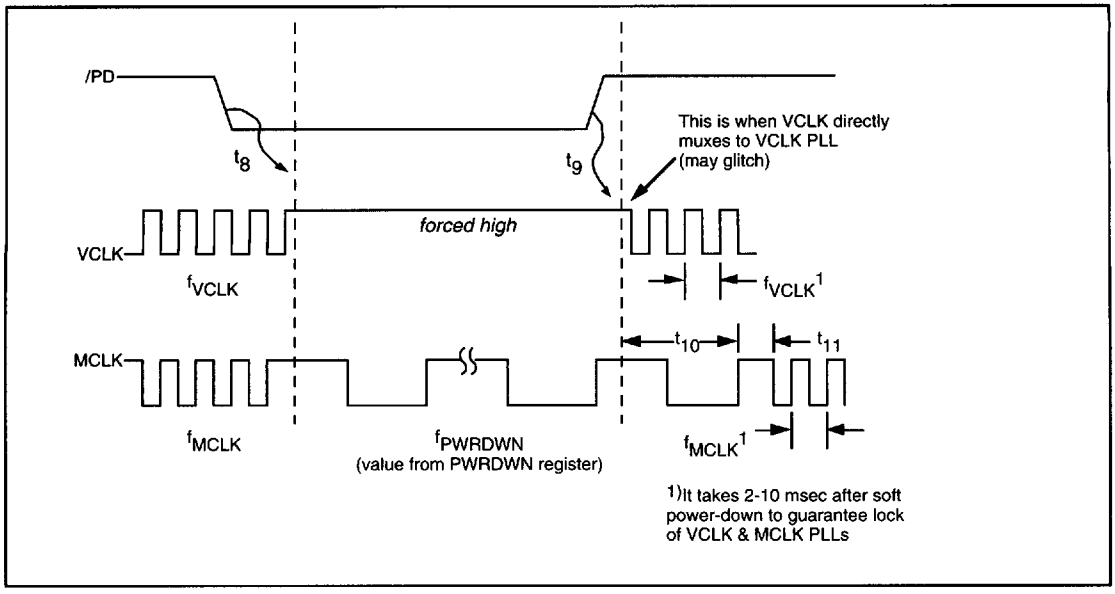
Tri-Stated Timing



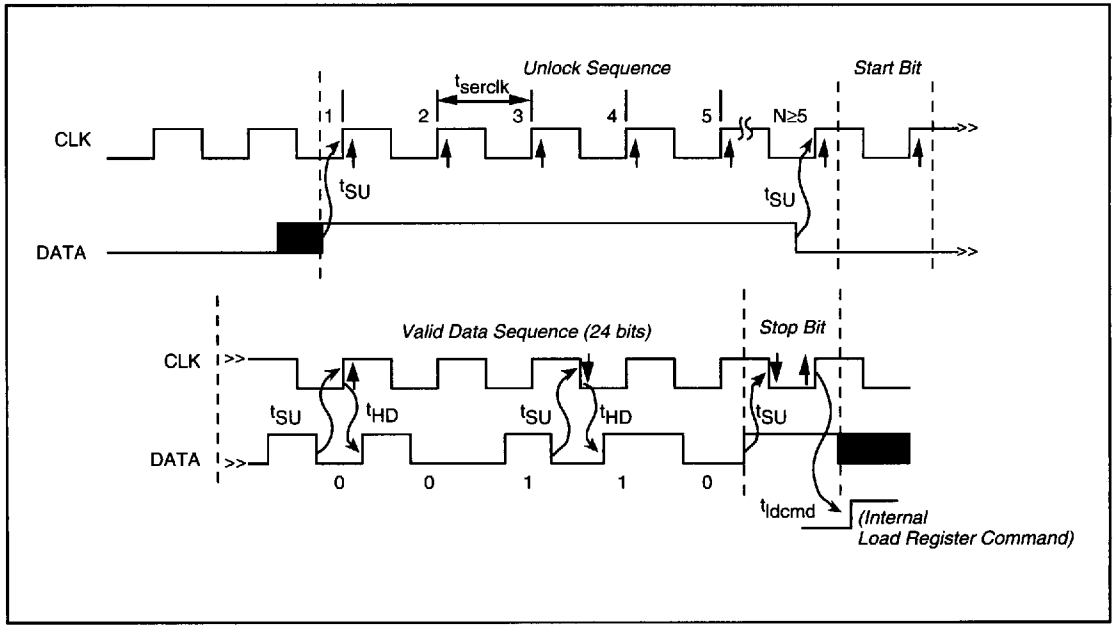
Selection Timing



MCLK & Active VCLK Register Programming Timing



Soft Power-Down Timing (Mode 2)



Serial Programming Timing

Ordering Information

Part Number	Temperature Range	Package Type
ICS9161-xxCW16	0°C to +70°C	16 lead Plastic SOIC
ICS9161-xxCN16	0°C to +70°C	16 lead Plastic DIP