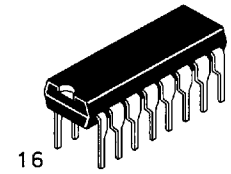
14-Bit Binary Counter

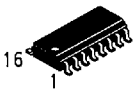
DV4020B

This device is a fourteen-stage binary counter constructed with P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse.

- **Supply voltage range = 3.0 Vdc to 18 Vdc**
- **All outputs buffered**
- **Capable of driving 4 Low Power TTL loads or one LS TTL load over the rated temperature range**
- **Diode protection on all inputs**
- **Highest noise immunity at 12V supply**

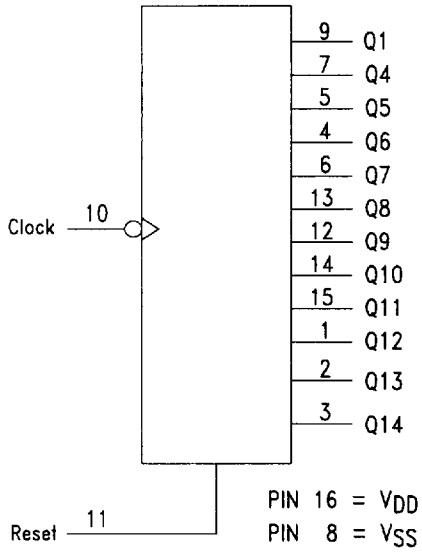


N Suffix
Plastic DIP
AVG-003 Case

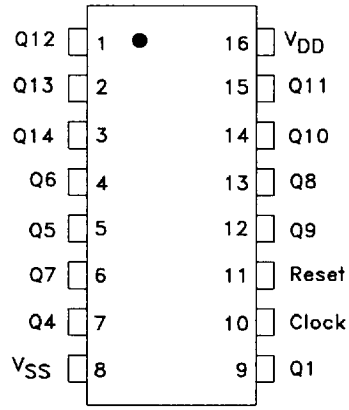


D Suffix
Plastic SOP
AVG-004 Case

4020B



PIN ASSIGNMENT



TRUTH TABLE
Positve Logic

Clock	Reset	Output State
↑	0	No Change
↓	0	Advance to next state
X	1	All outputs are low

↑ = Low to High Transition
↓ = High to Low Transition
X=Don't Care

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage (Referenced to V_{SS})	−0.5 to +18.0	V
V_{IN}, V_{OUT}	Input or Output Voltage	−0.5 to V_{DD}+0.5	V
I_{IN}, I_{OUT}	DC Current Into or Out of Any Pin	± 10	mA
P_D	Power Dissipation in Still Air, Derating: −12 mW/°C from 65° to 85°C	500	mW
T_{STG}	Storage Temperature Range	−65 to +150	°C
TL	Lead Temperature, (8 Second Soldering)	260	°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter		V_{DD}	Guaranteed Limits							Unit
				-40°C		25°C			85°C		
				Min	Max	Min	Typ	Max	Min	Max	
V_{OL}	Output Voltage $V_{IN}=V_{DD}$ or 0	"0" Level	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V_{OH}	V_{IN}= 0 or V_{DD}	"1" Level	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
V_{IL}	Input Voltage (V_O=4.5 or 0.5 Vdc) (V_O=9.0 or 1.0 Vdc) (V_O=13.5 or 1.5 Vdc)	"0" Level	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
V_{IH}	(V_O=0.5 or 4.5 Vdc) (V_O=1.0 or 9.0 Vdc) (V_O=1.5 or 13.5 Vdc)	"1" Level	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	Vdc
I_{OH}	Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	5.0 5.0 10 15	−3.0 −0.52 −1.3 −3.6	- - - -	−2.4 −0.44 −1.1 −3.0	−4.2 −0.88 −2.25 −8.8	- - - -	−1.7 −0.36 −0.9 −2.4	- - - -	mAdc
I_{OL}	(V_{OL} = 0.4 Vdc) (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	Sink	5.0 10 15	0.52 1.3 3.6	- - -	0.44 1.1 3.0	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
I_{IN}	Input Current		15	-	±0.3	-	±0.00001	±0.3	-	±1.0	µAdc
C_{IN}	Input Capacitance	V_{IN}=0	-	-	-	-	5.0	7.5	-	-	pF
I_{DD}	Quiescent Current (Per Package)		5.0 10 15	- - -	20 40 80	- - -	0.005 0.010 0.015	20 40 80	- - -	150 300 600	µAdc

SWITCHING CHARACTERISTICS (C_L=50 pF, T_A=25°C)

SWITCHING CHARACTERISTICS (Continued)

Symbol	Characteristics	V_{DD}	Min	Typ	Max	Unit
t_{TLH}, t_{THL}	Output Rise and Fall Time	5.0 10 15	- - -	100 50 40	200 100 80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to Q1	5.0 10 15	- - -	260 115 80	520 230 160	ns
	Clock to Q14	5.0 10 15	- - -	1820 805 560	3900 1725 1200	
t_{PHL}	Propagation Delay Time Reset to Q_n	5.0 10 15	- - -	370 155 115	740 310 230	ns
t_{WH}	Clock Pulse Width	5.0 10 15	500 165 125	140 55 38	- - -	ns
f_{cl}	Clock Pulse Frequency	5.0 10 15	- - -	2.0 6.0 8.0	1.0 3.0 4.0	MHz

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Symbol	Characteristics	V_{DD}	Min	Typ	Max	Unit
t_{TLH}, t_{THL}	Clock Input Rise and Fall Time	5.0 10 15		No Limit		–
t_{WL}	Reset Pulse Width	5.0 10 15	3000 550 420	320 120 80	- - -	ns
t_{rem}	Reset Removal Time	5.0 10 15	130 50 30	65 25 15	- - -	ns

SWITCHING WAVEFORMS