Features

- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 128 Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms maximum
  - 1 to 128 Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 5 mA CMOS Standby Current
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 Cycles
  - Data Retention: 10 years
- Single 5 V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

2 Megabit (256K x 8) Paged CMOS E^2PROM Module

Preliminary

Description

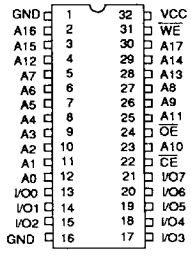
The AT28MC020 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its two megabits of memory is organized as 262,144 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 53 mA.

The AT28MC020 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte page register to allow writing of up to 128 bytes simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

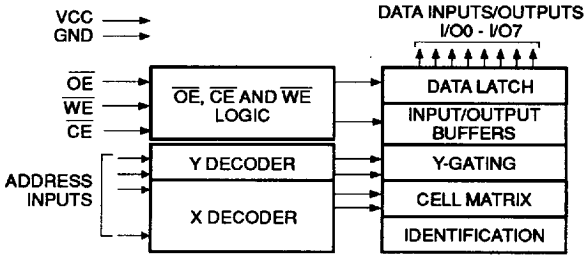
Atmel's 28MC020 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes.

Pin Configurations

Pin Name	Function
A0 - A17	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28MC020 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion.

PAGE WRITE: The page write operation of the AT28MC020 allows one to one hundred twenty-eight bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by one to one hundred twenty-seven additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28MC020 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A7-A17 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A7 - A17 must be the same.

The A0 to A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{DATA}$ POLLING: The AT28MC020 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

(continued on next page)

Device Operation (Continued)

TOGGLE BIT: In addition to $\overline{DATA}$ Polling the AT28MC020 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28MC020 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28MC020. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28MC020 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after t_{WC} the selected quadrant pointed to by A17 will be protected against inadvertent write operations. Because the AT28MC020 is comprised of two discrete memory devices the user must perform the three byte command sequence twice: once to the lower half with A17 = 0; and once to the upper half with A17 = 1.

It should be noted, that once protected the host may still perform a byte or page write to the AT28MC020. This is done by preceding the data to be written by the same three byte command sequence used to protect the device.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28MC020 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	20	40	pF	V_{IN} = 0 V
C_{OUT}	20	40	pF	V_{OUT} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT28MC020-15	AT28MC020-20	AT28MC020-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.

D.C. Characteristics

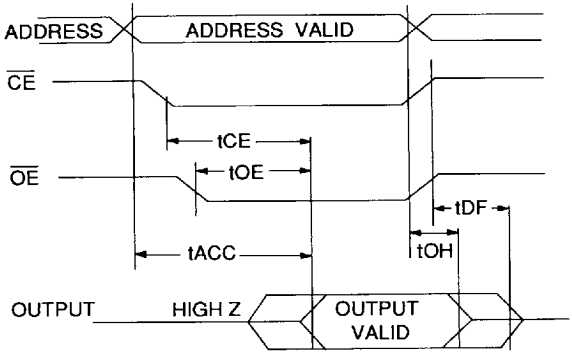
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 1 V		20	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		20	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC} + 1 V		5	mA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC} + 1 V		8	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

A.C. Read Characteristics

Symbol	Parameter	AT28MC020-15		AT28MC020-20		AT28MC020-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

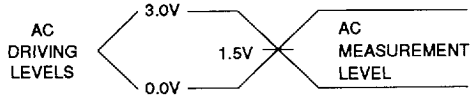
2

A.C. Read Waveforms



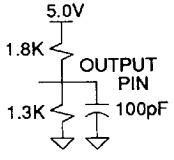
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load

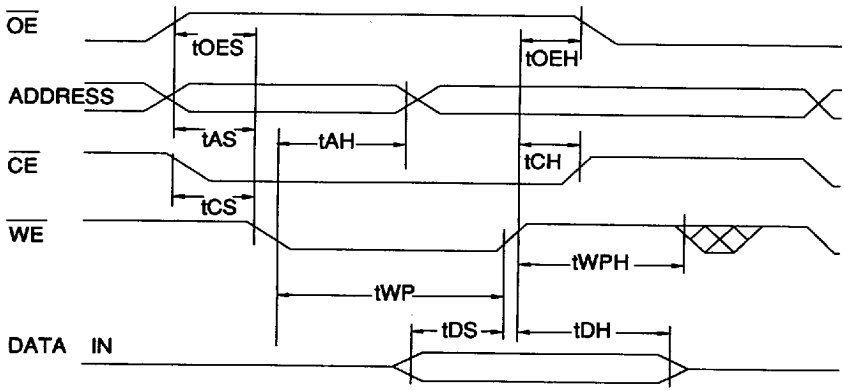


A.C. Write Characteristics

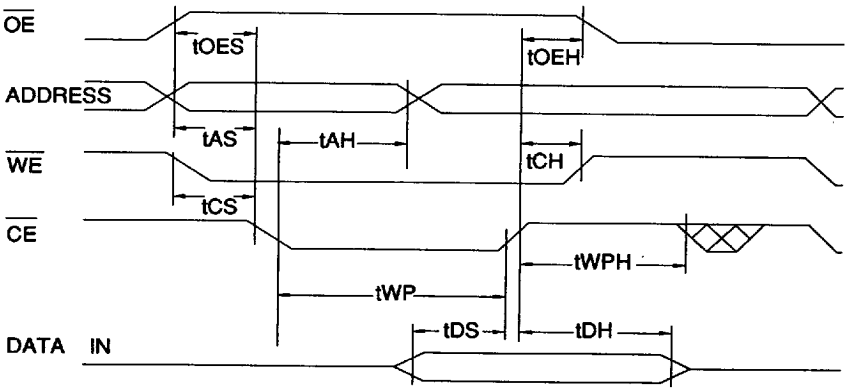
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	150		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WC}	Write Cycle Time		10	ms

Notes: 1. A17 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

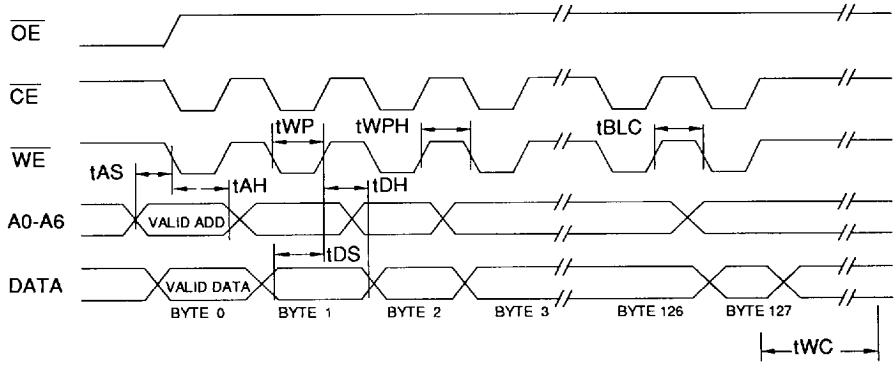


Page Mode Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	10		ns
t_{AH} (1)	Address Hold Time	100		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	150		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

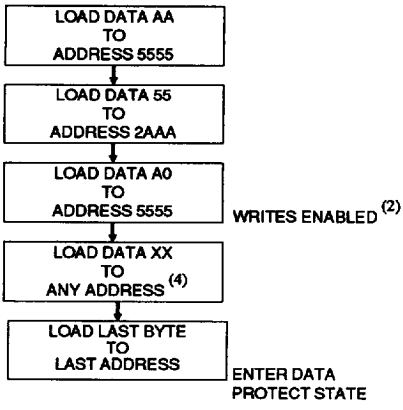
Notes: 1. A17 must remain valid throughout the $\overline{WE}$ or $\overline{CE}$ low pulse.

Page Mode Write Waveforms

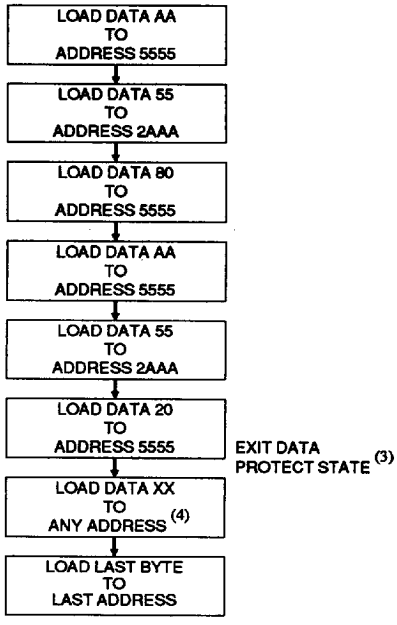


Notes: A7 through A17 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm [1,5,6]

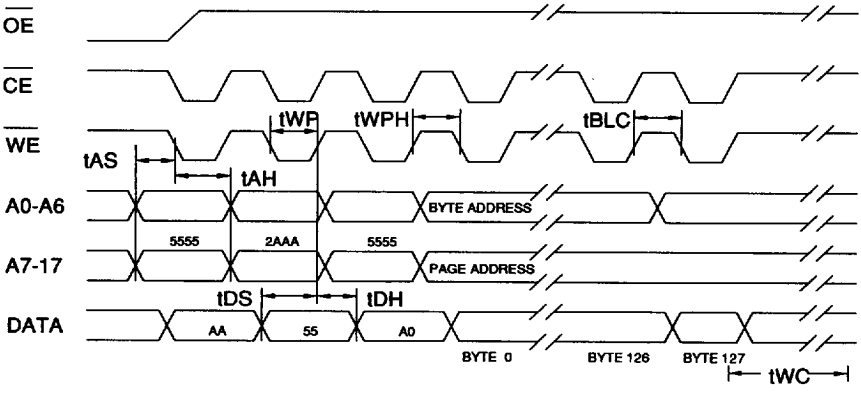


Software Data Protection Disable Algorithm [1,5,6]



Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.
5. A17 must address page to be written.
6. The quadrant determined by A17 acts independently.

Software Protected Program Cycle Waveform



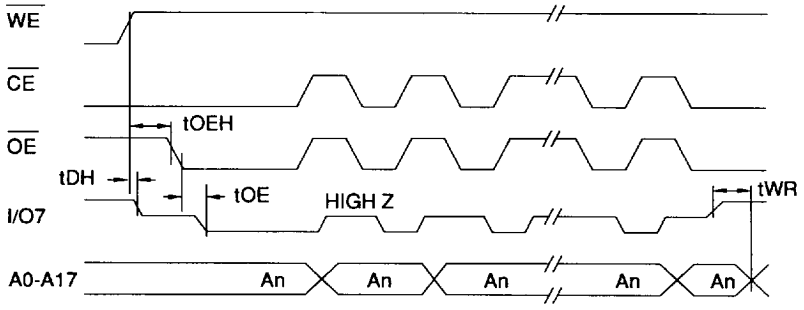
Notes: A0-A14 must conform to the addressing sequence for the first three bytes as shown above. In addition, for each write during this command sequence A17 must be the same.
After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A17) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay			100	ns
t_{WR}	Write Recovery Time	0			ns

Note: 1. These parameters are characterized and not 100% tested.

$\overline{\text{Data}}$ Polling Waveforms



Notes: For $\overline{\text{DATA}}$ Polling operations the state of A17 must be the same as it was for the byte or page write operation.

Ordering Information

tacc (ns)	Icc (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	80	0.5	AT28MC020-15ZC	32Z	Commercial (0° to 70°C)
			AT28MC020-15ZI	32Z	Industrial (-40° to 85°C)
			AT28MC020-15ZM	32Z	Military (-55°C to 125°C)
			AT28MC020-15ZMB	32Z	Screened IAW M5004 Military/883C Class B Components (-55°C to 125°C)
200	80	0.5	AT28MC020-20ZC	32Z	Commercial (0° to 70°C)
			AT28MC020-20ZI	32Z	Industrial (-40° to 85°C)
			AT28MC020-20ZM	32Z	Military (-55°C to 125°C)
			AT28MC020-20ZMB	32Z	Screened IAW M5004 Military/883C Class B Components (-55°C to 125°C)
250	80	0.5	AT28MC020-25ZC	32Z	Commercial (0° to 70°C)
			AT28MC020-25ZI	32Z	Industrial (-40° to 85°C)
			AT28MC020-25ZM	32Z	Military (-55°C to 125°C)
			AT28MC020-25ZMB	32Z	Screened IAW M5004 Military/883C Class B Components (-55°C to 125°C)

Package Type	
32Z	32 Lead, Non-Windowed, Ceramic Dual Inline 32D6 Compatible Multi-Chip Module (MCM)