REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R208-93.	93-08-06	Monica L. Poelking
B	Changes in accordance with NOR 5962-R187-94.	94-06-08	Monica L. Poelking
C	Add device type 02. Editorial changes throughout.	96-01-05	Monica L. Poelking
D	Changes in accordance with NOR 5962-R299-97.	97-05-29	Monica L. Poelking
E	Add device type 03. Editorial changes throughout. - tvn	98-06-29	Monica L. Poelking
F	In table IA: Add test conditions for I_{IN}; change the limits for Q_{IDD}; remove the test condition V_{DD} = 4.5 V for all the propagation delay tests; change the limits for t_a and t_i in memory read timing section; change the limits of t_c in DMA timing section; and change the limit of t_a in JTAG timing section. Include pin connections for case outlines X and Z in radiation exposure connections. Editorial changes throughout. - tvn	98-09-18	Monica L. Poelking
G	In table I, change I_{IN} limits; add a footnote to Q_{IDD}; add t_c in power-up master reset timing section. Correct the JTAG timing waveforms. – tvn	99-05-26	Monica L. Poelking

REV	E	E	E	E	E	E	E	E	E	E										
SHEET	35	36	37	38	39	40	41	42	43	44										
REV	E	E	E	E	E	E	E	G	E	G	E	E	E	E	E	F	F	G	E	E
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	G	E	E	E	E	G	G	G	G	G	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Thomas M. Hess

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
93-06-07

REVISION LEVEL
G

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, CMOS, MIL-STD-1553 SERIAL MICROCODED MONOLITHIC MULTI-MODE INTELLIGENT TERMINAL, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-92118**

SHEET 1 OF 44

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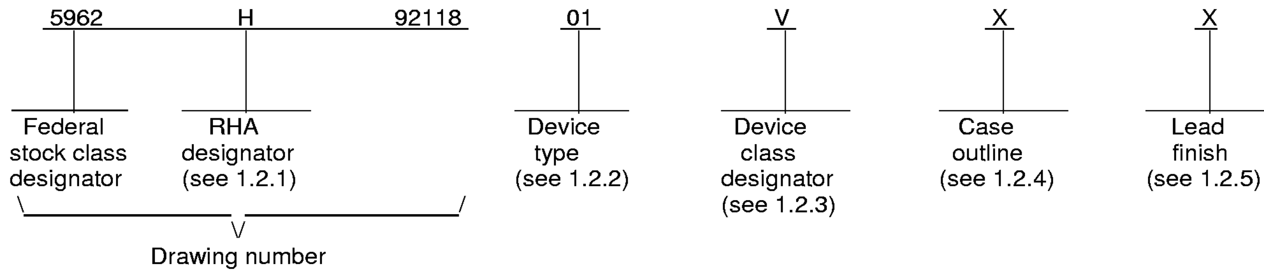
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT69151	MIL-STD-1553 bus controller, remote terminal, monitor interface
02	UT69151E	MIL-STD-1553 bus controller, remote terminal, monitor interface radiation hardened
03	UT69151E	MIL-STD-1553 bus controller, remote terminal, monitor interface

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA3-P84	84	Pin grid array
Y	See figure 1	84	Leaded chip carrier
Z	See figure 1	132	Leaded chip carrier with unformed leads, nonconductive tier bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V dc to +7.0 V dc
Voltage on any pin	-0.3 V dc to V_{CC} + 0.3 V dc
Latchup immunity (I_{LU})	±150 mA
DC input current (I_I)	±10 mA
Maximum power dissipation (P_D)	2.5 W
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	15°C/W
Maximum junction temperature (T_J)	175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
DC input voltage (V_{IN})	0 V dc to V_{DD}
Maximum input voltage (V_{IL})	0.8 V dc
Maximum input voltage, 24 MHz input (V_{ILC})	0.3 V_{DD}
Minimum input voltage (V_{IH})	2.2 V dc
Minimum input voltage, 24 MHz input (V_{IHC})	0.7 V_{DD}
Operating frequency (f_{IN})	24 ±0.01% MHz
Duty cycle (D_C)	50 ±5%
Case operating temperature range (T_C)	-55°C to +125°C
Radiation features:	
Total dose	≥ 1 x 10^6 Rads (Si)
Single event phenomenon (SEP) effective	
LET, no upsets	= 47 MeV/(mg/cm^2)
LET, no latchup	> 136 MeV/(mg/cm^2)
Dose rate upset (20 ns pulse)	2/
Dose rate latchup	2/
Dose rate survivability	2/
Neutron irradiated	2/

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	95.12 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ When characterized as a result of the procuring activities request, the condition will be specified.

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STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational sevices.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

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3.2.4 Boundary scan instruction codes. The boundary scan instruction codes shall be as specified on figure 4.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figures 5 through 13.

3.2.6 Radiation exposure connections. The radiation exposure connecttions shall be as specified on figure 14.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 IEEE 1149.1 compliance. Theses devices shall be compliant with IEEE 1149.1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{DD} \leq 5.5\ V$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Low level input voltage, except TCK input	V_{IL1}			All	1, 2, 3		0.8	V
Low level input voltage, TCK input only	V_{IL2}			01, 02	1, 2, 3		0.8	
				03			0.7	
High level input voltage	V_{IH}			All	1, 2, 3	2.2		
Low level input voltage	V_{ILC}	24 MHz input only		All	1, 2, 3		$0.3V_{DD}$	
High level intput voltage	V_{IHC}			All	1, 2, 3	$0.7V_{DD}$		
Low level output voltage	V_{OL}	Outputs loads	$I_{OL} = 4.0$ mA	All	1, 2, 3		0.4	
			$I_{OL} = 1.0\ \mu A$ 2/				0.05	
High level output voltage	V_{OH}	Outputs loads	$I_{OH} = 4.0$ mA	All	1, 2, 3	2.4		
			$I_{OH} = 1.0\ \mu A$ 2/			V_{DD}-0.05		
Input leakage current	I_{IN}	TTL driven inputs	$V_{IN} = V_{DD}$ or V_{SS}	All	1, 2, 3	-10	+10	µA
		Inputs with pull-up resistors	$V_{IN} = V_{DD}$	All	1, 2, 3	-10	+10	
			$V_{IN} = V_{SS}$	01, 02		-900	-150	
				03		-167	-27	
Three-state output leakage current, TTL loaded outputs	I_{OZ}	Single-drive buffer $V_O = V_{DD}$ or V_{SS}		All	1, 2, 3	-10	+10	µA
Short-circuit output current, output loads	I_{OS} 2/ 3/	Single-drive buffer $V_{DD} = 5.5$ V, $V_O = 0$ V		All	1, 2, 3	-100	+100	mA
Input capacitance	C_{IN}	f = 1 MHz at 0 V See 4.4.1c		All	4		15	pF
Output capacitance	C_{OUT}			All	4		15	
Bidirectional capacitance	C_{IO}			All	4		25	
Quiescent current 4/	Q_{IDD}	f = 1 MHz at 0 V 5/		All	1, 3		35	µA
					2		1	mA
Standby operating current	S_{IDD}	f = 24 MHz		All	1, 2, 3		40	mA
Functional tests		See 4.4.1b		All	7, 8			

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{DD} \leq 5.5 V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Register write timing							
Address setup time 6/	t_a	C_L = 35 pF minimum See figures 5 and 12	All	9, 10, 11	0		ns
Data setup time 6/	t_b		All	9, 10, 11	10		
Data hold time 6/	t_c		All	9, 10, 11	8		
Address hold time 6/	t_d		All	9, 10, 11	8		
$\overline{CS}$ (L) to $\overline{CS}$ (H) 6/	t_e		All	9, 10, 11	105		
Access delay 6/ 7/ 8/	t_f		All	9, 10, 11	85		
RD/ $\overline{WR}$ assertion to $\overline{CS}$ assertion 2/	t_g		All	9, 10, 11	0		
$\overline{CS}$ negation to RD/ $\overline{WR}$ negation 2/	t_h		All	9, 10, 11	0		
$\overline{CS}$ assertion to output enable 6/	t_i		All	9, 10, 11	0	40	
$\overline{CS}$ negation to output three-state 2/	t_j		All	9, 10, 11	5	35	
Register read timing							
Address setup time 6/	t_a	C_L = 35 pF minimum See figures 6 and 12	All	9, 10, 11	0		ns
$\overline{CS}$ assertion to output enable data valid 6/	t_b		All	9, 10, 11		95	
$\overline{CS}$ negation to output disabled 2/	t_c		All	9, 10, 11	5	35	
Address hold time 6/	t_d		All	9, 10, 11	0		
$\overline{CS}$ assertion to output enable data invalid 6/	t_e		All	9, 10, 11	0	40	
Access delay 6/ 7/ 8/	t_f		All	9, 10, 11	45		
$\overline{CS}$ (L) to $\overline{CS}$ (H) 2/	t_g		All	9, 10, 11	105		
Memory write timing							
Address propagation delay	t_a	C_L = 35 pF minimum See figures 7 and 12	01, 02	9, 10, 11	0	18	ns
			03	9, 10, 11	0	21	
Address valid to $\overline{RCS}$, $\overline{RWR}$ assertion 6/	t_b		All	9, 10, 11	15	35	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{DD} \leq 5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Memory write timing - Continued							
$\overline{DTACK}$ setup time 6/	t_c	C_L = 35 pF minimum See figures 7 and 12	All	9, 10, 11	10		ns
$\overline{RCS}$ and $\overline{RWR}$ hold time 6/ 9/	t_d		All	9, 10, 11	20	50	
Data propagation delay 6/	t_e		All	9, 10, 11	20	60	
Address hold time 6/	t_g		All	9, 10, 11	10	30	
$\overline{DTACK}$ hold time 6/	t_h		All	9, 10, 11	10		
$\overline{RWR}$ and $\overline{RCS}$ pulse width ($\overline{DTACK}$ tied to ground)	t_i		01, 02	9, 10, 11	34		
			03	9, 10, 11	32		
$\overline{RWR}$ and $\overline{RCS}$ ↑ to $\overline{DMACK}$ ↑ 2/ 9/	t_j		All	9, 10, 11	15	125	
Data hold time 2/	t_k		All	9, 10, 11	10	40	
Memory read timing							
Address propagation delay	t_a	C_L = 35 pF minimum See figures 8 and 12	01, 02	9, 10, 11	0	18	ns
			03	9, 10, 11	0	21	
Address valid to $\overline{RCS}$, $\overline{RRD}$ assertion 6/	t_b		All	9, 10, 11	15	35	
$\overline{DTACK}$ setup time 6/	t_c		All	9, 10, 11	10		
$\overline{RCS}$ and $\overline{RRD}$ hold time 6/ 9/	t_d		All	9, 10, 11	20	50	
Data setup delay 6/	t_e		01, 02	9, 10, 11	12		
			03	9, 10, 11	10		
Data hold delay	t_f		01, 02	9, 10, 11	0		
			03	9, 10, 11	2		
Address hold time 6/	t_g		All	9, 10, 11	10	30	
$\overline{DTACK}$ hold time	t_h		All	9, 10, 11	10		
$\overline{RRD}$ and $\overline{RCS}$ pulse width ($\overline{DTACK}$ tied to ground)	t_i		01, 02	9, 10, 11	34		
			03	9, 10, 11	32		
$\overline{RRD}$ and $\overline{RCS}$ ↑ to $\overline{DMACK}$ ↑ 2/	t_j		All	9, 10, 11	15	45	

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{DD} ≤ 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
DMA timing							
$\overline{\text{TERACT}}$ assertion to $\overline{\text{DMAR}}$ assertion 2/	t_a	C_L = 35 pF minimum See figures 9 and 12	All	9, 10, 11	5		µs
$\overline{\text{DMAR}}$ assertion to $\overline{\text{DMACK}}$ negation 2/	t_b	Bus controller	01	9, 10, 11		7	
			02, 03	9, 10, 11		16	
		Remote terminal	All	9, 10, 11		7	
		Remote terminal with monitor	All	9, 10, 11		7	
		Monitor	All	9, 10, 11		7	
$\overline{\text{DMAG}}$ assertion to $\overline{\text{DMACK}}$ assertion 6/	t_c		01, 02	9, 10, 11	0	30	ns
			03	9, 10, 11	5	30	
$\overline{\text{DMAG}}$ assertion to $\overline{\text{DMAR}}$ negation 2/	t_d		All	9, 10, 11	0	35	
$\overline{\text{DMACK}}$ assertion to address bus active	t_e		01, 02	9, 10, 11	0	5	
			03	9, 10, 11	-5	5	
$\overline{\text{DMACK}}$ assertion to $\overline{\text{DMAG}}$ negation 6/	t_f		All	9, 10, 11	10		
$\overline{\text{DMACK}}$ negation to $\overline{\text{DMAG}}$ assertion 2/	t_g		All	9, 10, 11	500		
$\overline{\text{DMACK}}$ assertion to RAM control active (negated)	t_h		01, 02	9, 10, 11	0	5	
			03		-5	5	
$\overline{\text{DMACK}}$ negation to address three-state 2/	t_i		All	9, 10, 11		5	
$\overline{\text{DMACK}}$ assertion to RAM control disabled 2/	t_j		All	9, 10, 11		5	
Power-up master reset timing							
$\overline{\text{MRST}}$ pulse width 2/	t_a	C_L = 35 pF minimum See figures 10 and 12	All	9, 10, 11	500		ns
$\overline{\text{MRST}}$ negation to $\overline{\text{ROMEN}}$ assertion 2/	t_b		All	9, 10, 11		5	µs
$\overline{\text{MRST}}$ negation to $\overline{\text{READY}}$ assertion 2/	t_c		All	9, 10, 11		10	µs
$\overline{\text{DMACK}}$ negation to $\overline{\text{ROMEN}}$ negation 2/	t_d		All	9, 10, 11		500	ns

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{DD} ≤ 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Biphase timing							
Biphase output skew	t_a	C_L = 35 pF minimum See figures 11 and 12	All	9, 10, 11		10	ns
Biphase input skew (low to high) 2/	t_b		All	9, 10, 11		250	
Biphase input skew (high to low) 2/	t_c		All	9, 10, 11		250	
Biphase input pulse width 2/	t_d		All	9, 10, 11	250		
JTAG timing							
TCK frequency		See figure 13	All	9, 10, 11		1	MHz
TCK period	t_a		All	9, 10, 11	1000		ns
TCK high time	t_b		All	9, 10, 11	$1/2t_a$		
TCK low time	t_c		All	9, 10, 11	$1/2t_a$		
TCK rise time	t_d		All	9, 10, 11		5	
TCK fall time	t_e		All	9, 10, 11		5	
TDI, TMS setup time	t_f		All	9, 10, 11	250		
TDI, TMS hold time	t_g		All	9, 10, 11	250		
TDO valid delay	t_h		All	9, 10, 11	250		

1/ Device type 02 supplied to this drawing will meet all levels M, D, L, R, F, G and H of irradiation. However, this device is only tested at the 'H' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C. Unless otherwise specified, all testing shall be conducted under worst-case conditions. "GND" may not vary from 0 V dc by more than ±50 mV.

2/ This parameter is guaranteed, but not tested, to the values in table IA herein.

3/ Tested one output at a time for a maximum duration of 1 second.

4/ Post irradiation limit is 1 mA for subgroup 1.

5/ Tested with all inputs tied to V_{DD}.

6/ For device type 03, this parameter is guaranteed, but not tested, to the values in table IA herein.

7/ Minimum pulse width from latter rising edge of RD/$\overline{WR}$ or $\overline{CS}$ to first falling edge.

8/ Read cycle followed by a read cycle - minimum 45 ns.
Read cycle followed by a write cycle - minimum 45 ns.
Write cycle followed by a read cycle - minimum 85 ns.
Write cycle followed by a write cycle - minimum 85 ns.

9/ Pulse width duration is measured with respect to the device's recognition of $\overline{DTACK}$ assertion.

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TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C	V_{DD} = 4.5 V		Bias for latch-up test V_{DD} = 5.5 V no latch-up LET = 3/
		Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section LET = 136	
02	+25°C	= 47	1.6 x 10^{-3} cm^2	> 136

1/ For SEP test conditions, see 4.4.4.4.
2/ Technology characterization and model verfication supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Test at worst case temperature T_A = +125°C.

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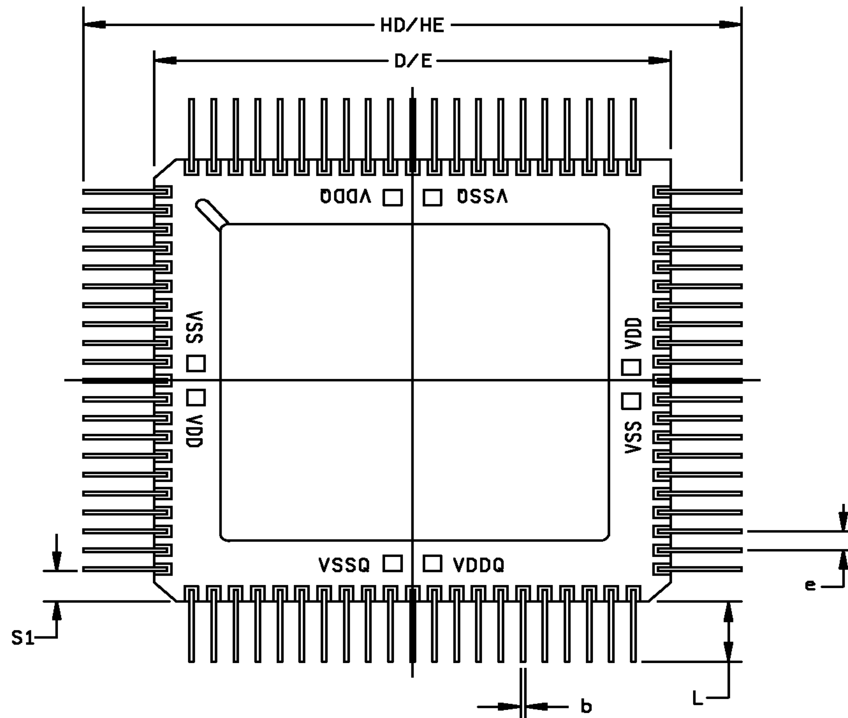
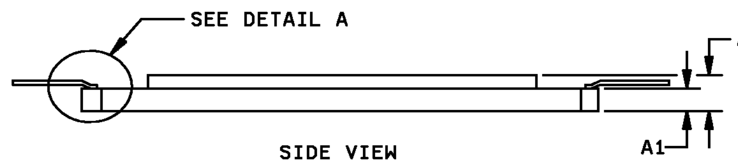
Case Y





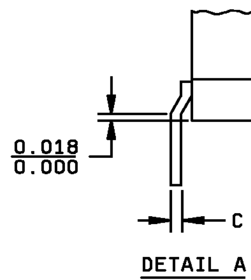


FIGURE 1. Case outline.

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Case Y						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A			3.30			0.130
A1	2.03		2.74	0.080		0.108
b	.36		.46	0.014		0.018
C	.15		.20	0.006		0.008
e		1.27			0.50	
D/E	28.91		29.52	1.138		1.162
HD/HE	45.59		46.36	1.795		1.825
L	.66			0.026		
S1	.13			0.005		
N	84			84		

FIGURE 1. Case outline - Continued.

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Case Z

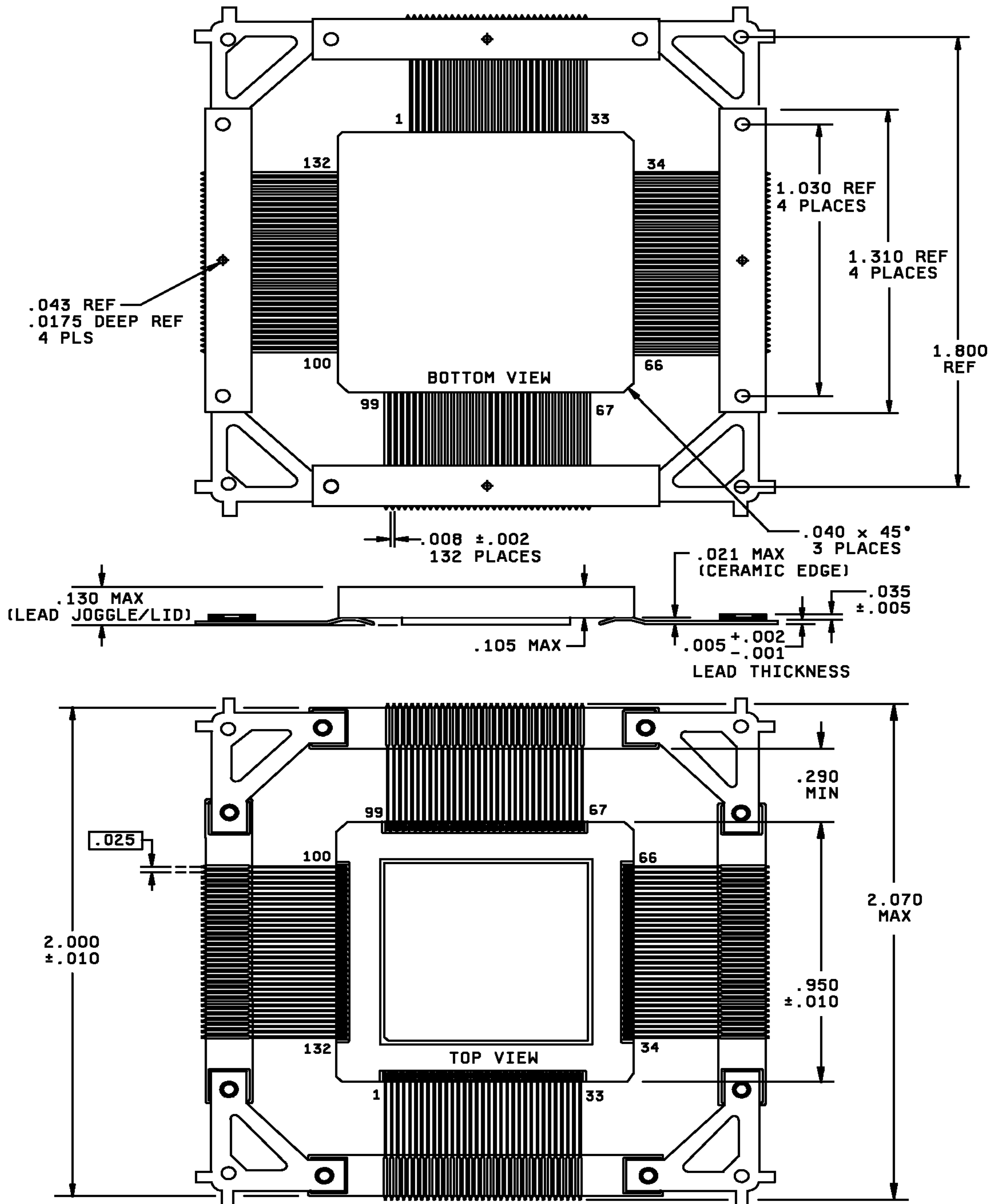

FIGURE 1. Case outline - Continued.

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Device type	All						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	$\overline{RRD}$	B11	$\overline{ROMEN}$	F9	V_{DD}	K2	$\overline{TIMERONA}$
A2	A0	C1	D15	F10	V_{SS}	K3	$\overline{TA}$
A3	A1	C2	TCLK	F11	$\overline{DMACK}$	K4	RA
A4	A3	C5	24 MHz	G1	D8	K5	TB
A5	A6	C6	V_{DD}	G2	D7	K6	$\overline{TB}$
A6	A4	C7	A9	G3	D6	K7	$\overline{READY}$
A7	A7	C10	$\overline{CS}$	G9	TDO	K8	RTA3
A8	A10	C11	$\overline{AUTOEN}$	G10	TDI	K9	RTA0
A9	A12	D1	D13	G11	TMS	K10	$\overline{LOCK}$
A10	A13	D2	D14	H1	D5	K11	MSEL1
A11	RD/ $\overline{WR}$	D10	$\overline{YF_INT}$	H2	D4	L1	D0
B1	$\overline{DTACK}$	D11	$\overline{MSG_INT}$	H10	$\overline{MRST}$	L2	TA
B2	$\overline{RCS}$	E1	D10	H11	$\overline{TRST}$	L3	$\overline{RA}$
B3	$\overline{RWR}$	E2	D11	J1	D3	L4	$\overline{TIMERONB}$
B4	A2	E3	V_{DD}	J2	D1	L5	$\overline{RB}$
B5	A5	E9	TCK	J5	RB	L6	V_{DD}
B6	V_{SS}	E10	$\overline{DMAG}$	J6	V_{SS}	L7	$\overline{TERACT}$
B7	A8	E11	$\overline{DMAR}$	J7	$\overline{SSYSF}$	L8	RTA4
B8	A11	F1	D9	J10	A/ $\overline{B}$ STD	L9	RTA2
B9	A14	F2	D12	J11	MSEL0	L10	RTA1
B10	A15	F3	V_{SS}	K1	D2	L11	RTPTY

FIGURE 2. Terminal connections.

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Device type	All						
Case outline	Y						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{RCS}$	22	$\overline{TIMERONA}$	43	$\overline{LOCK}$	64	A15
2	TCLK	23	$\overline{TA}$	44	A/$\overline{B}$ STD	65	A14
3	$\overline{DTACK}$	24	TA	45	MSEL1	66	A13
4	D15	25	$\overline{RA}$	46	MSEL0	67	A12
5	D14	26	RA	47	$\overline{MRST}$	68	A11
6	D13	27	$\overline{TIMERONB}$	48	$\overline{TRST}$	69	A10
7	D12	28	$\overline{TB}$	49	TDO	70	A9
8	D11	29	TB	50	TDI	71	A8
9	D10	30	$\overline{RB}$	51	TMS	72	A7
10	D9	31	V_{SS}	52	V_{SS}	73	V_{DD}
11	V_{SS}	32	V_{DD}	53	V_{DD}	74	V_{SS}
12	V_{DD}	33	RB	54	TCK	75	24 MHz
13	D8	34	$\overline{TERACT}$	55	$\overline{DMAR}$	76	A6
14	D7	35	$\overline{READY}$	56	$\overline{DMAG}$	77	A5
15	D6	36	$\overline{SSYSF}$	57	$\overline{DMACK}$	78	A4
16	D5	37	RTA4	58	$\overline{MSG_INT}$	79	A3
17	D4	38	RTA3	59	$\overline{YF_INT}$	80	A2
18	D3	39	RTA2	60	$\overline{AUTOEN}$	81	A1
19	D2	40	RTA1	61	$\overline{ROMEN}$	82	A0
20	D1	41	RTA0	62	$\overline{CS}$	83	$\overline{RWR}$
21	D0	42	RTPTY	63	RD/ $\overline{WR}$	84	$\overline{RRD}$

FIGURE 2. Terminal connections - Continued.

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Device type	All								
Case outline	Z								
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{SS}	28	NC	55	NC	82	V_{SS}	109	A9
2	$\overline{RCS}$	29	NC	56	NC	83	V_{DD}	110	A8
3	TCLK	30	D2	57	$\overline{SSYSF}$	84	TCK	111	NC
4	$\overline{DTACK}$	31	D1	58	RTA4	85	$\overline{DMAR}$	112	NC
5	NC	32	D0	59	RTA3	86	$\overline{DMAG}$	113	NC
6	NC	33	V_{SS}	60	RTA2	87	NC	114	A7
7	D15	34	V_{DD}	61	NC	88	NC	115	V_{DD}
8	D14	35	$\overline{TIMERONA}$	62	NC	89	NC	116	V_{SS}
9	D13	36	$\overline{TA}$	63	RTA1	90	$\overline{DMACK}$	117	24 MHz
10	D12	37	TA	64	RTA0	91	$\overline{MSG_INT}$	118	A6
11	D11	38	$\overline{RA}$	65	RTPTY	92	$\overline{YF_INT}$	119	A5
12	NC	39	NC	66	V_{DD}	93	$\overline{AUTOEN}$	120	NC
13	NC	40	NC	67	V_{SS}	94	NC	121	NC
14	NC	41	RA	68	$\overline{LOCK}$	95	NC	122	NC
15	D10	42	$\overline{TIMERONB}$	69	A/$\overline{B}$ STD	96	$\overline{ROMEN}$	123	A4
16	V_{SS}	43	$\overline{TB}$	70	NC	97	$\overline{CS}$	124	A3
17	V_{DD}	44	TB	71	NC	98	RD/$\overline{WR}$	125	A2
18	D9	45	NC	72	NC	99	V_{SS}	126	A1
19	D8	46	NC	73	MSEL1	100	V_{DD}	127	NC
20	D7	47	NC	74	MSEL0	101	A15	128	NC
21	NC	48	$\overline{RB}$	75	$\overline{MRST}$	102	A14	129	A0
22	NC	49	V_{SS}	76	NC	103	A13	130	$\overline{RWR}$
23	NC	50	V_{DD}	77	NC	104	NC	131	$\overline{RRD}$
24	D6	51	RB	78	$\overline{TRST}$	105	NC	132	V_{DD}
25	D5	52	$\overline{TERACT}$	79	TDO	106	A12		
26	D4	53	$\overline{READY}$	80	TDI	107	A11		
27	D3	54	NC	81	TMS	108	A10		

NC = No connection

FIGURE 2. Terminal connections - Continued.

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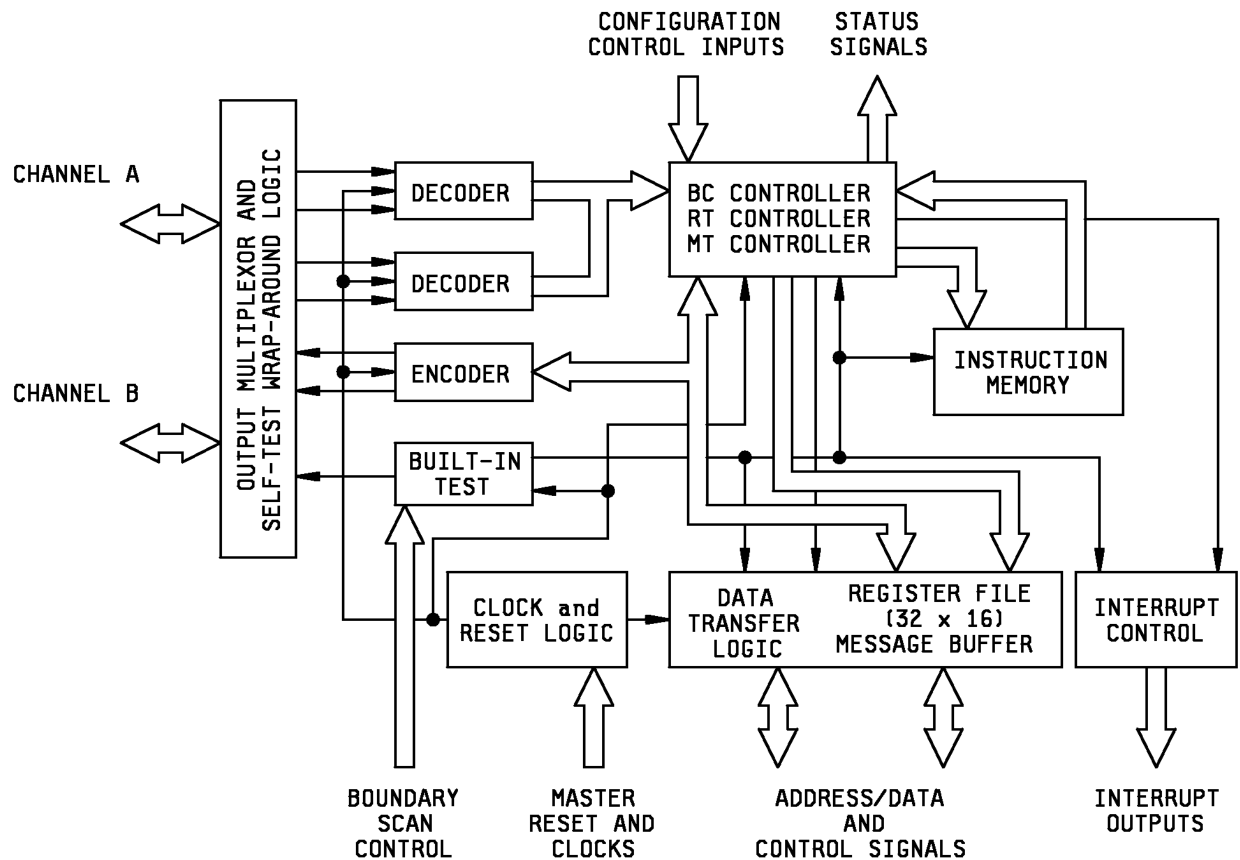

FIGURE 3. Block diagram.

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Device type 02	
Instruction name	Instruction code
BYPASS	1111
SAMPLE/PRELOAD	0010
EXTEST	0000
INTEST	0001
RUNBIST	0111
IDCODE	0100
GL-TRISTATE	0011
INTERNAL-SCAN	0101
PRIVATE	0110
USER-SELECTABLE	1000 $\rightarrow$ 1110

Device type 03	
Instruction name	Instruction code
BYPASS	1111
SAMPLE/PRELOAD	0010
EXTEST	0000

FIGURE 4. Boundary scan instruction codes.

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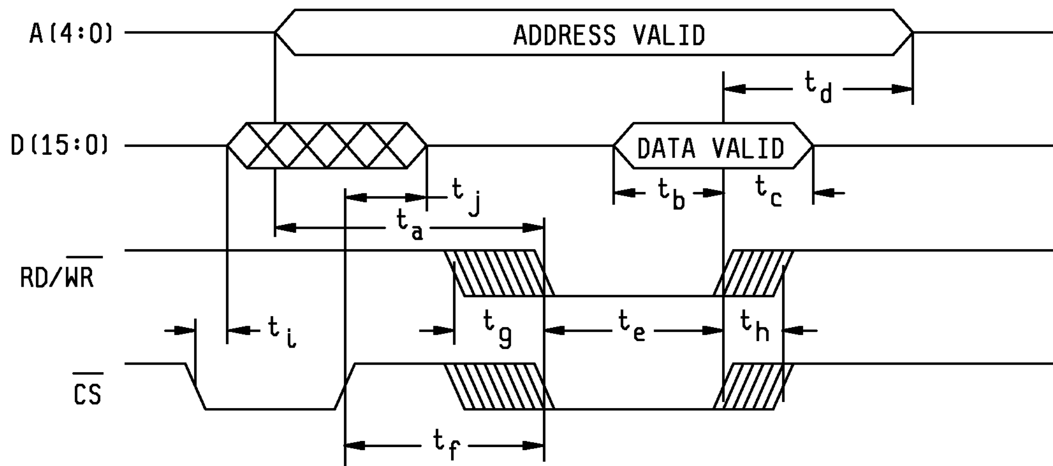

FIGURE 5. Register write.

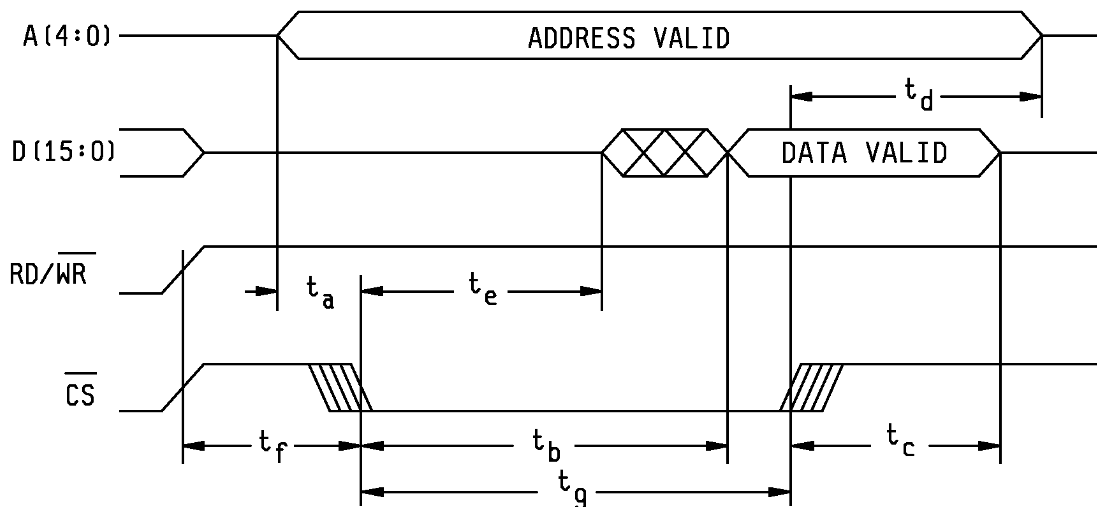

FIGURE 6. Register read.

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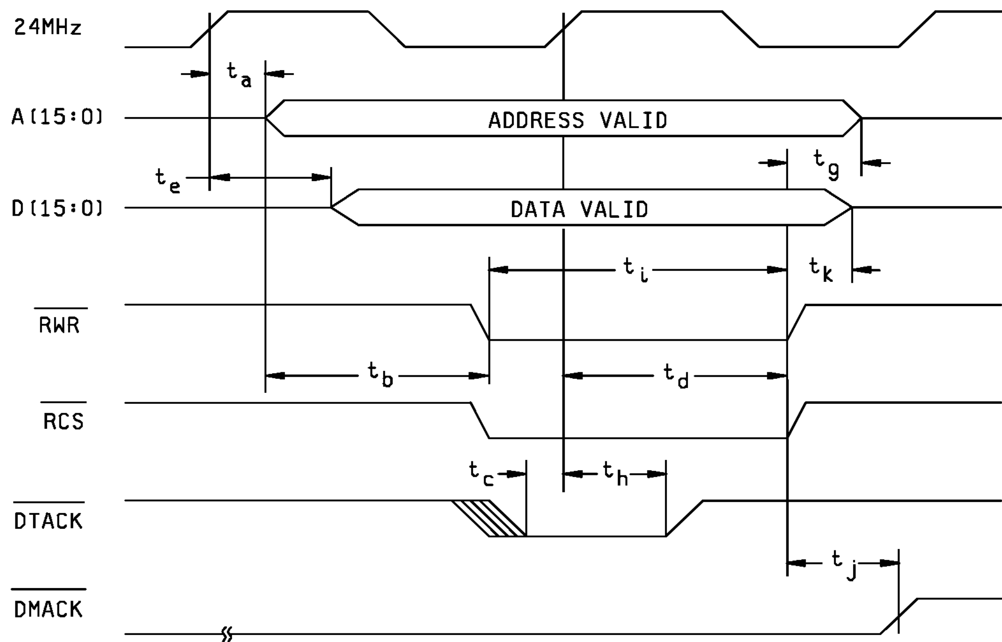

FIGURE 7. Memory write.

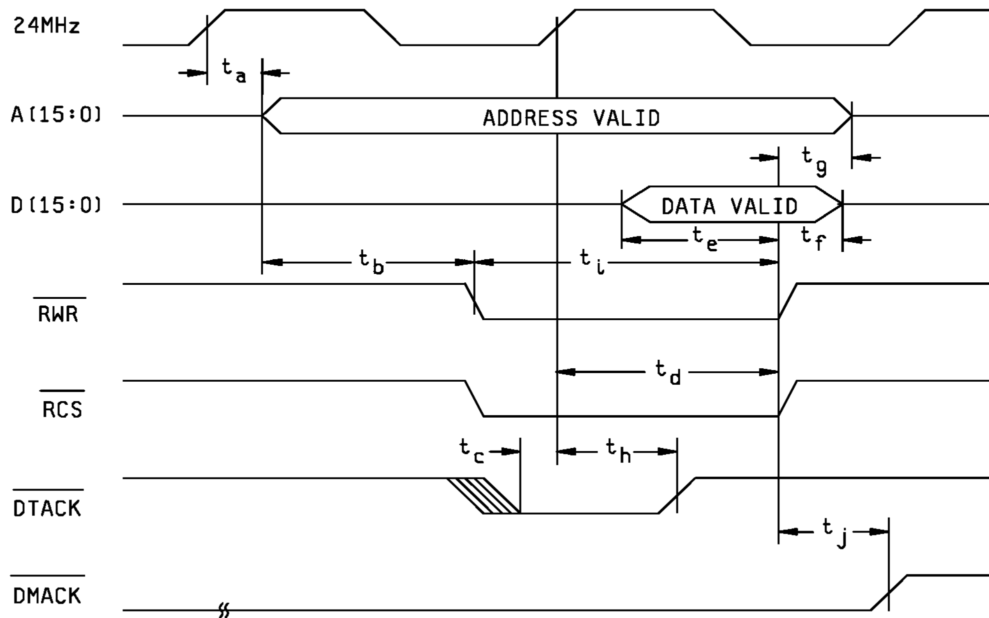

FIGURE 8. Memory read.

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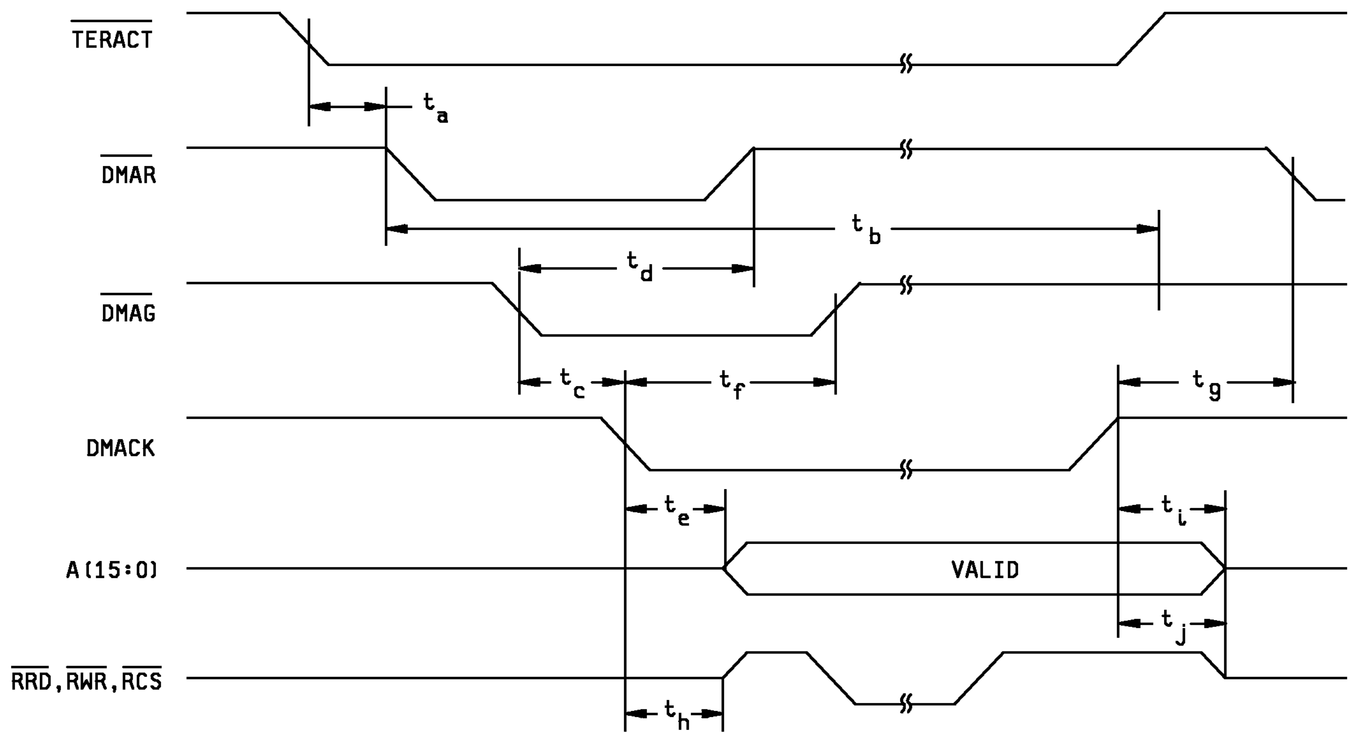

FIGURE 9. DMA timing.

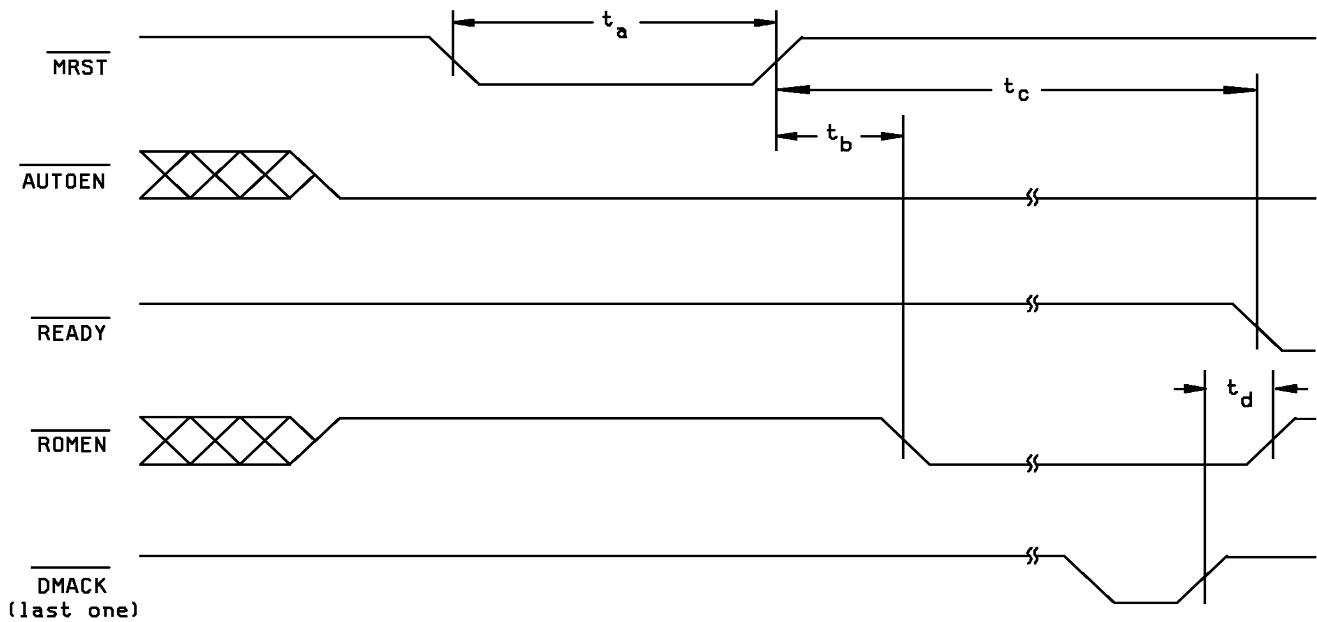

FIGURE 10. Power-up master reset.

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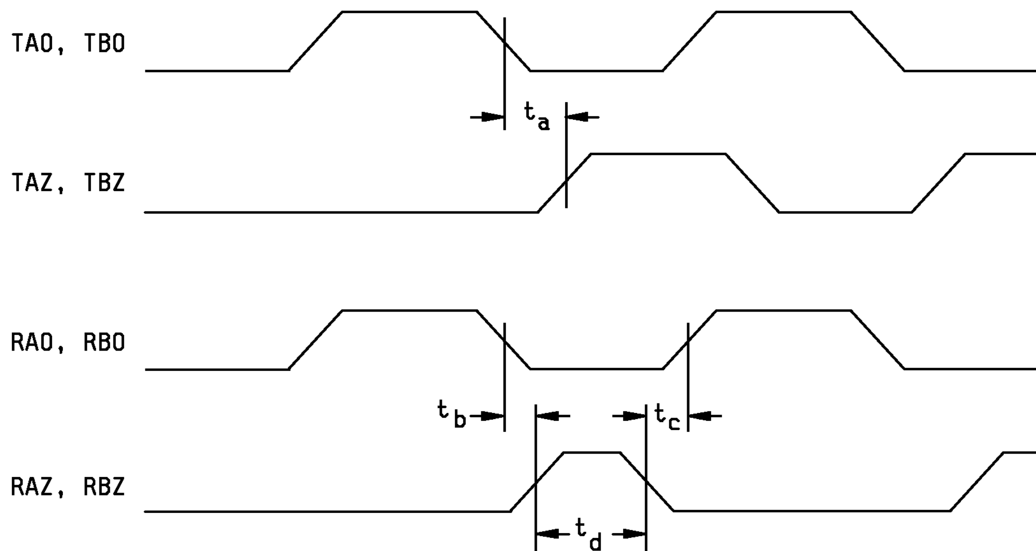
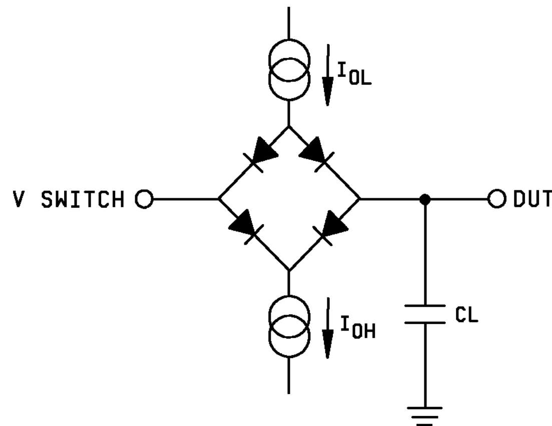


FIGURE 11. Biphase timing.



NOTES: V switch = (V_{OL}max + V_{OL}min)/2
C_L = 35 pF

FIGURE 12. AC test circuit.

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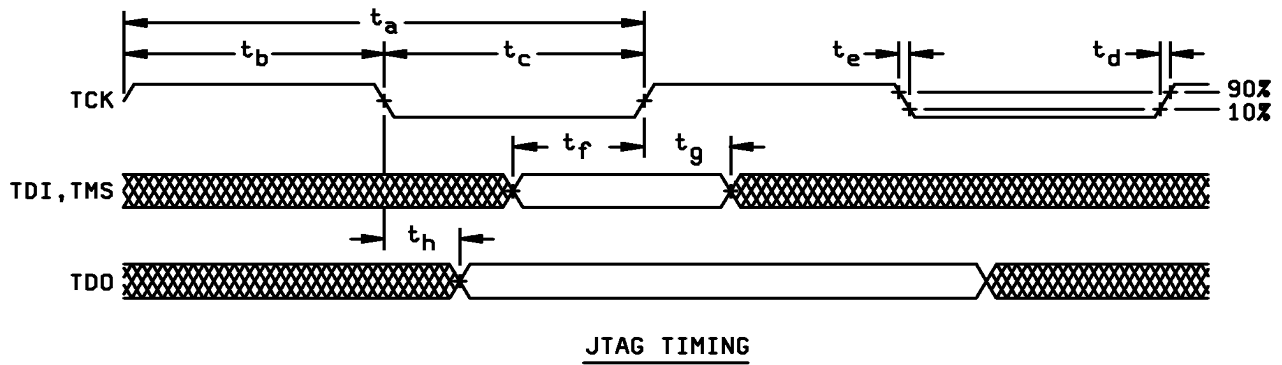

FIGURE 13. JTAG timing waveforms.

Case outline	Open	V_{DD} = 5 V ± 0.5 V	Ground
X	A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, B1, B2, B3, B4, B5, B7, B8, B9, B10, B11, C1, C7, D1, D2, D10, D11, E1, E2, E11, F1, F2, F11, G1, G2, G3, G9, H1, H2, J1, J2, K1, K2, K3, K5, K6, K7, L1, L2, L4, L7	A11, C2, C6, C11, E3, E9, F9, G10, H10, J5, K4, K9, K10, K11, L6, L8, L9	B6, C5, C10, E10, F3, F10, G11, H11, J6, J7, J10, J11, K8, L3, L5, L10, L11
Y	1, 3, 4, 5, 6, 7, 8, 9, 10, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 27, 28, 29, 34, 35, 49, 55, 57, 58, 59, 61, 64, 65, 66, 67, 68, 69, 70, 71, 72, 76, 77, 78, 79, 80, 81, 82, 83, 84	2, 12, 26, 32, 33, 37, 39, 41, 43, 45, 47, 50, 53, 54, 60, 63, 73	11, 25, 30, 31, 36, 38, 40, 42, 44, 46, 48, 51, 52, 56, 62, 74, 75
Z	2, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 35, 36, 37, 39, 40, 42, 43, 44, 45, 46, 47, 52, 53, 54, 55, 56, 61, 62, 70, 71, 72, 76, 77, 79, 85, 87, 88, 89, 90, 91, 92, 94, 95, 96, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131	3, 17, 34, 41, 50, 51, 58, 60, 64, 66, 68, 73, 75, 80, 83, 84, 93, 98, 100, 115, 132	1, 16, 33, 38, 48, 49, 57, 59, 63, 65, 67, 69, 74, 78, 81, 82, 86, 97, 99, 116, 117

NOTE: Each pin except B6, C6, E3, F3, F9, F10, J6, and L6 for case outline X (11, 12, 31, 32, 52, 53, 73, and 74 for case outline Y; and 1, 16, 17, 33, 34, 49, 50, 66, 67, 82, 83, 99, 100, 115, 116, and 132 for case outline Z) will have a resistor of 2.49 kΩ ± 5% for irradiation testing.

FIGURE 14. Radiation exposure connections.

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4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 5 devices with zero failures shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits, as specified in table IIB herein, shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter	Symbol	Delta limits
Quiescent current	Q_{IDD}	±10% of measured values or 35 µA whichever is greater

NOTE: If the device is tested at or below 35 µA, no deltas are required.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (See 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

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TABLE III. Pin descriptions.

Name	Type 1/	Active 2/	Description
Data bus			
D0	TTB	--	Bit 0 (LSB) of the bidirectional Data bus.
D1	TTB	--	Bit 1 of the bidirectional Data bus.
D2	TTB	--	Bit 2 of the bidirectional Data bus.
D3	TTB	--	Bit 3 of the bidirectional Data bus.
D4	TTB	--	Bit 4 of the bidirectional Data bus.
D5	TTB	--	Bit 5 of the bidirectional Data bus.
D6	TTB	--	Bit 6 of the bidirectional Data bus.
D7	TTB	--	Bit 7 of the bidirectional Data bus.
D8	TTB	--	Bit 8 of the bidirectional Data bus.
D9	TTB	--	Bit 9 of the bidirectional Data bus.
D10	TTB	--	Bit 10 of the bidirectional Data bus.
D11	TTB	--	Bit 11 of the bidirectional Data bus.
D12	TTB	--	Bit 12 of the bidirectional Data bus.
D13	TTB	--	Bit 13 of the bidirectional Data bus.
D14	TTB	--	Bit 14 of the bidirectional Data bus.
D15	TTB	--	Bit 15 (MSB) of the bidirectional Data bus.
Address bus			
A0	TTB	--	Bit 0 (LSB) of the bidirectional Address bus.
A1	TTB	--	Bit 1 of the bidirectional Address bus.
A2	TTB	--	Bit 2 of the bidirectional Address bus.
A3	TTB	--	Bit 3 of the bidirectional Address bus.
A4	TTB	--	Bit 4 of the bidirectional Address bus.
A5	TTB	--	Bit 5 of the bidirectional Address bus.
A6	TTB	--	Bit 6 of the bidirectional Address bus.
A7	TTB	--	Bit 7 of the bidirectional Address bus.
A8	TTB	--	Bit 8 of the bidirectional Address bus.
A9	TTB	--	Bit 9 of the bidirectional Address bus.
A10	TTB	--	Bit 10 of the bidirectional Address bus.
A11	TTB	--	Bit 11 of the bidirectional Address bus.
A12	TTB	--	Bit 12 of the bidirectional Address bus.
A13	TTB	--	Bit 13 of the bidirectional Address bus.
A14	TTB	--	Bit 14 of the bidirectional Address bus.
A15	TTB	--	Bit 15 (MSB) of the bidirectional Address bus.

See footnotes at end of table.

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TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
Remote terminal address inputs			
RTA0	TUI	--	Remote Terminal Address bit 0. This is bit 0 of the RT address. This is the least significant bit for the RT address.
RTA1	TUI	--	Remote Terminal Address bit 1. This is bit 1 of the RT address.
RTA2	TUI	--	Remote Terminal Address bit 2. This is bit 2 of the RT address.
RTA3	TUI	--	Remote Terminal Address bit 3. This is bit 3 of the RT address.
RTA4	TUI	--	Remote Terminal Address bit 4. This is the most significant bit of the RT address.
RTPTY	TUI	--	Remote Terminal Parity. This is an odd parity input for the RT address.
JTAG testability pins			
TDO	TTO	--	TDO. This output performs the operation of Test Data Output as defined in the IEEE Standard 1149.1. This cell provides the output signal for the Test Access Port (TAP). This noninverfting output buffer is optimized for driving TTL loads.
TCK	TUI	--	TCK. This input performs the operation of Test Clock input as defined in the IEEE Standard 1149.1. This noninverting input buffer is optimized for driving TTL input levels.
TMS	TUI	--	TMS. This input performs the operation of Test Mode Select as defined in the IEEE Standard 1149.1. This cell provides the input signal for the Test Access Port (TAP). This noninverting input buffer is optimized for driving TTL input levels.
TDI	TUI	--	TDI. This input performs the operation of Test Data In as defined in the IEEE Standard 1149.1. This cell provides the input signal for the Test Access Port (TAP). This noninverting input buffer is optimized for driving TTL input levels.
$\overline{TRST}$	TUI	--	$\overline{TRST}$. This input provides the reset to the TAP controller as defined in the IEEE Standard 1149.1. This non-inverting input buffer is optimized for driving TTL input levels. When not exercising JTAG, tie $\overline{TRST}$ to a logical 0.
Biphase inputs			
RA	TI	--	Receive Channel A (true). This is the Manchester-encoded true signal input for channel A. (Quiescent low).
$\overline{RA}$	TI	--	Receive Channel A (complement). This is the Manchester-encoded complement signal input for channel A. (Quiescent low).
RB	TI	--	Receive Channel B (true). This is the Manchester-encoded true signal input for channel B. (Quiescent low).
$\overline{RB}$	TI	--	Receive Channel B (complement). This is the Manchester-encoded complement signal input for channel B. (Quiescent low).
Biphase outputs			
TA	TO	--	Transmit Channel A (true). This is the Manchester-encoded true signal output for channel A. The signal is idle low. (Quiescent low).
$\overline{TA}$	TO	--	Transmit Channel A (complement). This is the Manchester-encoded complement signal output for channel A. The signal is idle low. (Quiescent low).
TB	TO	--	Transmit Channel B (true). This is the Manchester-encoded true signal output for channel B. The signal is idle low. (Quiescent low).
$\overline{TB}$	TO	--	Transmit Channel B (complement). This is the Manchester-encoded complement signal output for channel B. The signal is idle low. (Quiescent low).

See footnotes at end of table.

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TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
DMA signals			
$\overline{DMAR}$	TTO 3/	AL	DMA Request. This signal is asserted when access to RAM is required. It goes inactive upon receipt of the $\overline{DMAG}$ signal.
$\overline{DMAG}$	TI	AL	DMA Grant. Once this input is received, the device is allowed to access RAM.
$\overline{DMACK}$	TTO 3/	AL	DMA Acknowledge. This signal is asserted by the device to indicate the receipt of $\overline{DMAG}$. The signal remains active until all RAM bus activity is completed.
$\overline{DTACK}$	TI	AL	Data Transfer Acknowledge. This pin indicates that a data transfer is to occur and that the device may complete the memory cycle.
Control signals			
RD/ $\overline{WR}$	TI	--	Read/Write. This indicates the direction of data flow with respect to the host. A logic high signal means the host is trying to read data from the device, and a logic low signal means the host is trying to write data to the device.
$\overline{CS}$	TI	AL	Chip Select. This pin selects the device when accessing the internal registers.
$\overline{RRD}$	TTO	AL	RAM Read. This signal is generated by the device to read data from RAM.
$\overline{RWR}$	TTO	AL	RAM Write. This signal is generated by the device to write data to RAM.
$\overline{RCS}$	TTO	AL	RAM Chip Select. This signal is used in conjunction with the $\overline{RRD}$ / $\overline{RWR}$ signals to access RAM.
$\overline{AUTOEN}$	TUI	AL	Auto Enable. This pin, when active, enables automatic initialization applications.
$\overline{ROMEN}$	TTO 3/	AL	ROM Enable. This pin, when active, enables the ROM for automatic initialization applications.
$\overline{SSYSF}$	TUI	AL	Subsystem Fail. Upon receipt, this signal propagates directly to the RT 1553 Status word.
24 MHz	CI	--	24 MHz Clock. This 24 MHz input clock requires a 50% ±10% duty cycle with an accuracy of ±0.01%.
$\overline{MRST}$	TUI	AL	Master Reset. This input pin resets the internal encoders, decoders, all register, and associated logic.
MSEL1	TI	--	Mode Select 1. This pin is the most significant bit for the mode select. For proper mode selection, see below: MSEL1 / MSEL0 / Mode of Operation 0 / 0 / Bus Controller = SBC 0 / 1 / Remote Terminal = SRT 1 / 0 / Monitor Terminal = SMT 1 / 1 / SMT/SRT
MSEL0	TI	--	Mode Select 0. This pin is the least significant bit for the mode select. (See MSEL1 for proper logic states.)

See footnotes at end of table.

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TABLE III. Pin descriptions - Continued.

Name	Type 1/	Active 2/	Description
Control signals - Continued.			
TCLK	TI	--	Timer Clock. This internal timer is a 16-bit counter with a 64 µs resolution when using the 24 MHz input clock. For different applications, the user may input a clock (0-60 MHz) to establish the timer resolution. (Duty Cycle = 50% ±10%).
$A/\overline{B}$ STD	TUI	--	Military Standard A or B. This pin defines whether the device will be used a MIL-STD-1553A or 1553B mode of operation.
$\overline{LOCK}$	TUI	AL	Lock. This pin, when set active, prevents software changes to both the RT address, $A/\overline{B}$ STD, and mode select.
Status signals			
$\overline{TERACT}$	TO	AL	Terminal Active. This output pin indicates that the terminal is actively processing a 1553 command.
$\overline{TIMERONA}$	TO	AL	Timer On A. This is a 800 µs fail-safe transmitter enable timer for channel A. This ouput is reset on receipt of a new command or after 760 µs.
$\overline{TIMERONB}$	TO	AL	Timer On B. This is a 800 µs fail-safe transmitter enable timer for channel B. This ouput is reset on receipt of a new command or after 760 µs.
$\overline{MSG_INT}$	TTO 3/	AL	Message Interrupt. This pin is active for three clock cycles (i. e., 125 ns pulse) upon the occurrence of interrupt events which are enabled.
$\overline{YF_INT}$	TTO 3/	AL	YOU Failed Interrupt. This pin is active for three clock cycles (i. e., 125 ns pulse) upon the occurrence of interrupt events which are enabled.
$\overline{READY}$	TO	AL	Ready. This signal indicates the device has completeed initialization or BIT, and regular execution may begin.
Power/Ground			
V_{DD}	--	--	+5 Volt Power (± 10%)
V_{SS}	--	--	Digital ground.

1/ TO = TTL output
TTB = Three-state TTL bidirectional
CI = CMOS input
TUI = TTL input (internally pulled high)
TI = TTL input
TTO = Three-state TTL output

2/ AH = Active high
AL = Active low

3/ High impedance and active low.

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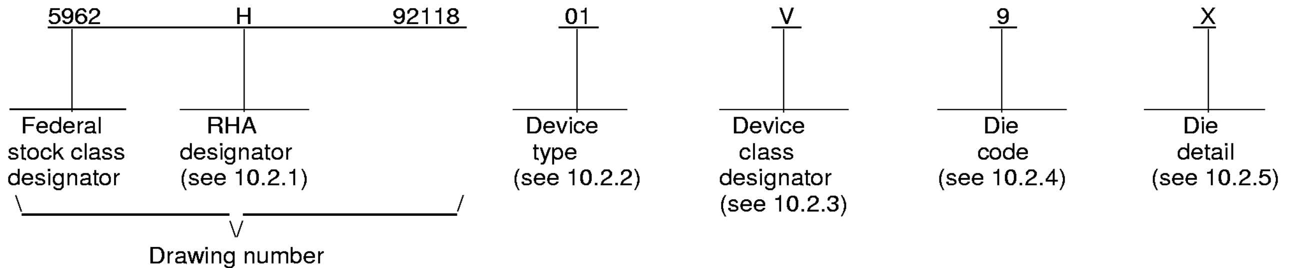
Appendix A

APPENDIX A FORMS A PART OF SMD 5962-92118

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type 1/	Generic number	Circuit function
01	UT69151	MIL-STD-1553 bus controller, remote terminal, monitor interface
02	UT69151E	MIL-STD-1553 bus controller, remote terminal, monitor interface radiation hardened
03	UT69151E	MIL-STD-1553 bus controller, remote terminal, monitor interface

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

10.2.5. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.5.1 Die physical dimensions.

Die type	Figure number
02	A-1

1/ Device types 01and 03 are not available as QML die only.

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10.2.5.2 Die bonding pad locations and electrical functions.

Die type	Figure number
02	A-1

10.2.5.3 Interface materials.

Die type	Figure number
02	A-1

10.2.5.4 Assembly related information.

Die type	Figure number
02	A-1

10.3. Absolute maximum ratings.

See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.

See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

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20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.5.1 and on figure A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.5.2 and on figure A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.5.3 and on figure A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.5.4 and figure A-1.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

30.4 Electrical test requirements. The test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4).

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c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein.

50. Die carrier

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60. NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614) 692-0674.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 495 mils x 495 mils.
Die thickness: 17.5 ±1 mils.

Interface materials.
Top metallization: Si Al Cu 9 kA-12.5 kA
Backside metallization: None: Backgrind

Glassivation.
Type: PSG
Thickness: 9 kA / ±11 kA

Substrate: EPI on single crystal silicon
Substrate potential: Tied to V_{DD}
Special assembly instructions: None

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Appendix A

APPENDIX A FORMS A PART OF SMD 5962-92118

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
1	0.2173	0.2406	V_{DD}
2	0.2110	0.2406	V_{SS}
3	0.2047	0.2406	No connect
4	0.1984	0.2406	$\overline{RCS}$
5	0.1921	0.2406	No connect
6	0.1858	0.2406	TCLK
7	0.1795	0.2406	No connect
8	0.1732	0.2406	$\overline{DTACK}$
9	0.1669	0.2406	No connect
10	0.1606	0.2406	No connect
11	0.1543	0.2406	D15
12	0.1480	0.2406	No connect
13	0.1417	0.2406	D14
14	0.1354	0.2406	No connect
15	0.1291	0.2406	D13
16	0.1228	0.2406	No connect
17	0.1165	0.2406	V_{DDQ}
18	0.1102	0.2406	V_{SSQ}
19	0.1039	0.2406	V_{DD}
20	0.0976	0.2406	V_{SS}
21	0.0913	0.2406	No connect
22	0.0850	0.2406	D12
23	0.0787	0.2406	No coonect
24	0.0724	0.2406	D11
25	0.0661	0.2406	No connect
26	0.0598	0.2406	No connect
27	0.0535	0.2406	No connect
28	0.0472	0.2406	No connect
29	0.0410	0.2406	No connect
30	0.0347	0.2406	D10
31	0.0284	0.2406	No connect
32	0.0221	0.2406	D9
33	0.0158	0.2406	No connect
34	0.0095	0.2406	V_{SSQ}
35	0.0031	0.2406	V_{SS}
36	-0.0032	0.2406	V_{DD}
37	-0.0095	0.2406	V_{DDQ}
38	-0.0158	0.2406	No connect
39	-0.0221	0.2406	D8
40	-0.0284	0.2406	No connect

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1

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Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
41	-0.0346	0.2406	D7
42	-0.0409	0.2406	No connect
43	-0.0472	0.2406	No connect
44	-0.0535	0.2406	No connect
45	-0.0598	0.2406	No connect
46	-0.0661	0.2406	No connect
47	-0.0724	0.2406	D6
48	-0.0787	0.2406	No connect
49	-0.0850	0.2406	D5
50	-0.0913	0.2406	No connect
51	-0.0976	0.2406	V_{SS}
52	-0.1039	0.2406	V_{DD}
53	-0.1102	0.2406	V_{SSQ}
54	-0.1165	0.2406	V_{DDQ}
55	-0.1228	0.2406	No connect
56	-0.1291	0.2406	D4
57	-0.1354	0.2406	No connect
58	-0.1417	0.2406	D3
59	-0.1480	0.2406	No connect
60	-0.1543	0.2406	No connect
61	-0.1606	0.2406	No connect
62	-0.1669	0.2406	No connect
63	-0.1732	0.2406	No connect
64	-0.1795	0.2406	D2
65	-0.1858	0.2406	No connect
66	-0.1921	0.2406	D1
67	-0.1984	0.2406	No connect
68	-0.2047	0.2406	D0
69	-0.2110	0.2406	V_{SS}
70	-0.2173	0.2406	V_{DD}
71	-0.2349	0.2173	V_{SSQ}
72	-0.2349	0.2110	V_{DDQ}
73	-0.2349	0.2047	$\overline{\text{TIMERONA}}$
74	-0.2349	0.1984	No connect
75	-0.2349	0.1921	$\overline{\text{TA}}$
76	-0.2349	0.1858	No connect
77	-0.2349	0.1795	TA
78	-0.2349	0.1732	No connect
79	-0.2349	0.1669	$\overline{\text{RA}}$
80	-0.2349	0.1606	No connect

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1

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APPENDIX A FORMS A PART OF SMD 5962-92118

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
81	-0.2349	0.1543	No connect
82	-0.2349	0.1480	No connect
83	-0.2349	0.1417	RA
84	-0.2349	0.1354	No connect
85	-0.2349	0.1291	$\overline{TIMERONB}$
86	-0.2349	0.1228	No connect
87	-0.2349	0.1165	V_{SS}
88	-0.2349	0.1102	V_{DD}
89	-0.2349	0.1039	V_{SSQ}
90	-0.2349	0.0976	V_{DDQ}
91	-0.2349	0.0913	No connect
92	-0.2349	0.0850	$\overline{TB}$
93	-0.2349	0.0787	No connect
94	-0.2349	0.0724	TB
95	-0.2349	0.0661	No connect
96	-0.2349	0.0598	No connect
97	-0.2349	0.0535	No connect
98	-0.2349	0.0472	No connect
99	-0.2349	0.0409	No connect
100	-0.2349	0.0347	$\overline{RB}$
101	-0.2349	0.0284	No connect
102	-0.2349	0.0221	RB
103	-0.2349	0.0158	No connect
104	-0.2349	0.0095	V_{SSQ}
105	-0.2349	0.0032	V_{SS}
106	-0.2349	-0.0032	V_{DD}
107	-0.2349	-0.0095	V_{DDQ}
108	-0.2349	-0.0158	No connect
109	-0.2349	-0.0221	$\overline{TERACT}$
110	-0.2349	-0.0284	No connect
111	-0.2349	-0.0374	$\overline{READY}$
112	-0.2349	-0.0409	No connect
113	-0.2349	-0.0472	No connect
114	-0.2349	-0.0535	No connect
115	-0.2349	-0.0598	No connect
116	-0.2349	-0.0661	No connect
117	-0.2349	-0.0724	$\overline{SSYSF}$
118	-0.2349	-0.0787	No connect
119	-0.2349	-0.0850	RTA4
120	-0.2349	-0.0913	No connect

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1

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Appendix A

APPENDIX A FORMS A PART OF SMD 5962-92118

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
121	-0.2349	-0.0976	V_{DDQ}
122	-0.2349	-0.1039	V_{SSQ}
123	-0.2349	-0.1102	V_{DD}
124	-0.2349	-0.1165	V_{SS}
125	-0.2349	-0.1228	No connect
126	-0.2349	-0.1291	RTA3
127	-0.2349	-0.1354	No connect
128	-0.2349	-0.1417	RTA2
129	-0.2349	-0.1480	No connect
130	-0.2349	-0.1543	No connect
131	-0.2349	-0.1606	No connect
132	-0.2349	-0.1669	No connect
133	-0.2349	-0.1732	No connect
134	-0.2349	-0.1795	RTA1
135	-0.2349	-0.1858	No connect
136	-0.2349	-0.1921	RTA0
137	-0.2349	-0.1984	No connect
138	-0.2349	-0.2047	RTPTY
139	-0.2349	-0.2110	V_{DDQ}
140	-0.2349	-0.2173	V_{SSQ}
141	-0.2173	-0.2406	V_{DD}
142	-0.2110	-0.2406	V_{SS}
143	-0.2047	-0.2406	$\overline{\text{LOCK}}$
144	-0.1984	-0.2406	No connect
145	-0.1921	-0.2406	A/$\overline{\text{B}}$ STD
146	-0.1858	-0.2406	No connect
147	-0.1795	-0.2406	No connect
148	-0.1732	-0.2406	No connect
149	-0.1669	-0.2406	No connect
150	-0.1606	-0.2406	No connect
151	-0.1543	-0.2406	MSEL1
152	-0.1480	-0.2406	No connect
153	-0.1417	-0.2406	MSEL0
154	-0.1354	-0.2406	No connect
155	-0.1291	-0.2406	$\overline{\text{MRST}}$
156	-0.1228	-0.2406	No connect
157	-0.1165	-0.2406	V_{DDQ}
158	-0.1102	-0.2406	V_{SSQ}
159	-0.1039	-0.2406	V_{DD}
160	-0.0976	-0.2406	V_{SS}

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1

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Appendix A

APPENDIX A FORMS A PART OF SMD 5962-92118

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
161	-0.0913	-0.2406	No connect
162	-0.0850	-0.2406	No connect
163	-0.0787	-0.2406	No connect
164	-0.0724	-0.2406	No connect
165	-0.0661	-0.2406	No connect
166	-0.0598	-0.2406	No connect
167	-0.0535	-0.2406	No connect
168	-0.0472	-0.2406	No connect
169	-0.0409	-0.2406	TRS
170	-0.0347	-0.2406	TDO
171	-0.0284	-0.2406	TDI
172	-0.0221	-0.2406	TMS
173	-0.0158	-0.2406	TCK
174	-0.0095	-0.2406	V_{DDQ}
175	-0.0032	-0.2406	V_{DD}
176	0.0032	-0.2406	V_{SS}
177	0.0095	-0.2406	V_{SSQ}
178	0.0158	-0.2406	No connect
179	0.0221	-0.2406	$\overline{DMAR}$
180	0.0284	-0.2406	No connect
181	0.0347	-0.2406	$\overline{DMAG}$
182	0.0409	-0.2406	No connect
183	0.0472	-0.2406	No connect
184	0.0535	-0.2406	No connect
185	0.0598	-0.2406	No connect
186	0.0661	-0.2406	No connect
187	0.0724	-0.2406	$\overline{DMACK}$
188	0.0787	-0.2406	No connect
189	0.0850	-0.2406	$\overline{MSG_INT}$
190	0.0913	-0.2406	No connect
191	0.0976	-0.2406	V_{SS}
192	0.1039	-0.2406	V_{DD}
193	0.1102	-0.2406	V_{SSQ}
194	0.1165	-0.2406	V_{DDQ}
195	0.1228	-0.2406	No connect
196	0.1291	-0.2406	$\overline{YF_INT}$
197	0.1354	-0.2406	No connect
198	0.1417	-0.2406	$\overline{AUTOEN}$
199	0.1480	-0.2406	No connect
200	0.1543	-0.2406	No connect

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1

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Appendix A

APPENDIX A FORMS A PART OF SMD 5962-92118

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
201	0.1606	-0.2406	No connect
202	0.1669	-0.2406	No connect
203	0.1732	-0.2406	No connect
204	0.1795	-0.2406	$\overline{ROMEN}$
205	0.1858	-0.2406	No connect
206	0.1921	-0.2406	$\overline{CS}$
207	0.1984	-0.2406	No connect
208	0.2047	-0.2406	RD/ $\overline{WR}$
209	0.2110	-0.2406	V_{SS}
210	0.2173	-0.2406	V_{DD}
211	0.2349	-0.2173	V_{SSQ}
212	0.2349	-0.2110	V_{DDQ}
213	0.2349	-0.2047	A15
214	0.2349	-0.1984	No connect
215	0.2349	-0.1921	A14
216	0.2349	-0.1858	No connect
217	0.2349	-0.1795	A13
218	0.2349	-0.1732	No connect
219	0.2349	-0.1669	No connect
220	0.2349	-0.1606	No connect
221	0.2349	-0.1543	A12
222	0.2349	-0.1480	No connect
223	0.2349	-0.1417	A11
224	0.2349	-0.1354	No connect
225	0.2349	-0.1291	A10
226	0.2349	-0.1228	No connect
227	0.2349	-0.1165	V_{SS}
228	0.2349	-0.1102	V_{DD}
229	0.2349	-0.1039	V_{SSQ}
230	0.2349	-0.0976	V_{DDQ}
231	0.2349	-0.0913	No connect
232	0.2349	-0.0850	A9
233	0.2349	-0.0787	No connect
234	0.2349	-0.0724	A8
235	0.2349	-0.0661	No connect
236	0.2349	-0.0598	No connect
237	0.2349	-0.0535	No connect
238	0.2349	-0.0472	No connect
239	0.2349	-0.0409	No connect
240	0.2349	-0.0347	A7

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1

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Appendix A

APPENDIX A FORMS A PART OF SMD 5962-92118

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
241	0.2349	-0.0284	No connect
242	0.2349	-0.0221	MHz24
243	0.2349	-0.0158	No connect
244	0.2349	-0.0095	V_{DDQ}
245	0.2349	-0.0032	V_{DD}
246	0.2349	0.0032	V_{SS}
247	0.2349	0.0095	V_{SSQ}
248	0.2349	0.0158	No connect
249	0.2349	0.0221	A6
250	0.2349	0.0284	No connect
251	0.2349	0.0347	A5
252	0.2349	0.0409	No connect
253	0.2349	0.0472	No connect
254	0.2349	0.0535	No connect
255	0.2349	0.0598	No connect
256	0.2349	0.0661	No connect
257	0.2349	0.0724	A4
258	0.2349	0.0787	No connect
259	0.2349	0.0850	A3
260	0.2349	0.0913	No connect
261	0.2349	0.0976	V_{DDQ}
262	0.2349	0.1039	V_{SSQ}
263	0.2349	0.1102	V_{DD}
264	0.2349	0.1165	V_{SS}
265	0.2349	0.1228	No connect
266	0.2349	0.1291	A2
267	0.2349	0.1354	No connect
268	0.2349	0.1417	A1
269	0.2349	0.1480	No connect
270	0.2349	0.1543	No connect
271	0.2349	0.1606	No connect
272	0.2349	0.1669	No connect
273	0.2349	0.1732	No connect
274	0.2349	0.1795	A0
275	0.2349	0.1858	No connect
276	0.2349	0.1921	$\overline{RWR}$
277	0.2349	0.1984	No connect
278	0.2349	0.2047	$\overline{RRD}$
279	0.2349	0.2110	V_{DDQ}
280	0.2349	0.2173	V_{SSQ}

NOTE: The die center is the coordinate origin (0,0).

FIGURE A-1

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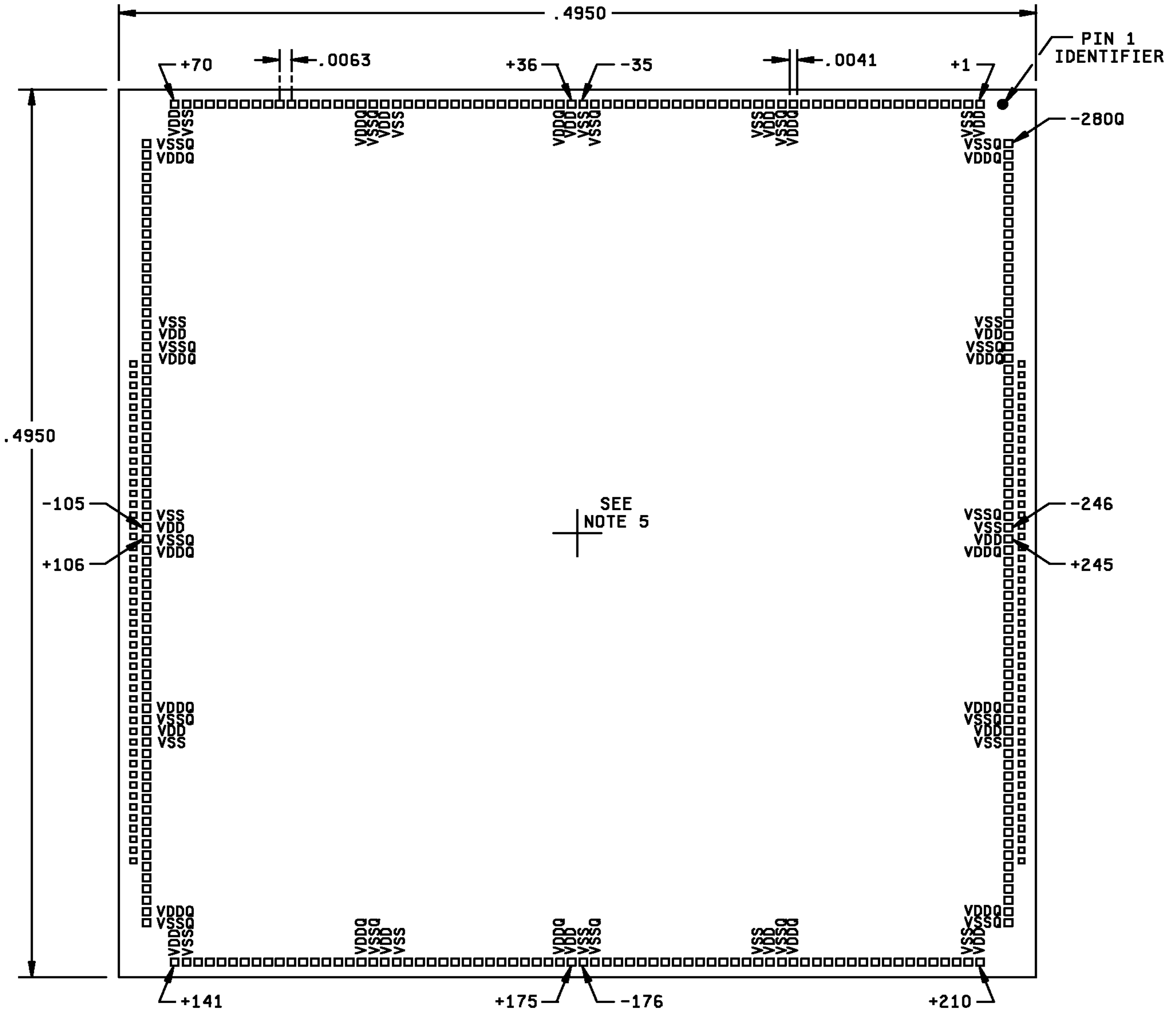

NOTES:
1. Die bondpad numbers are for reference only.
2. Dimensions are in inches and are basic.
3. Die thickness is 0.0175 ±0.001.
4. Die backside is as lapped.
5. The die center is the coordinate origin (0,0).
6. Backside bias is V_{DD}.

FIGURE A-1

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-05-26

Approved sources of supply for SMD 5962-92118 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and/or QML-38535 during the next revision. MIL-HDBK-103 and/or QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and/or QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9211801MXA	3/	
5962-9211801MXC	3/	
5962-9211801MYA	3/	
5962-9211801MYC	3/	
5962H9211802QXA	65342	UT69151EGBAH
5962H9211802QXC	65342	UT69151EGBCH
5962H9211802QYA	65342	UT69151EWBAH
5962H9211802QYC	65342	UT69151EWBCH
5962H9211802QZA	65342	UT69151EFBAH
5962H9211802QZC	65342	UT69151EFBCH
5962H9211802VXA	65342	UT69151EGSAH
5962H9211802VXC	65342	UT69151EGSCH
5962H9211802VYA	65342	UT69151EWSAH
5962H9211802VYC	65342	UT69151EWSCH
5962H9211802VZA	65342	UT69151EFSAH
5962H9211802VZC	65342	UT69151EFSCH
5962H9211802Q9A	65342	UT69151E-Q DIE
5962H9211802V9A	65342	UT69151E-V DIE
5962-9211803QXA	65342	UT69151EGBA
5962-9211803QXC	65342	UT69151EGBC
5962-9211803QYA	65342	UT69151EWBA
5962-9211803QYC	65342	UT69151EWBC

See footnotes at end of table.

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9211803QZA	65342	UT69151EFBA
5962-9211803QZC	65342	UT69151EFBC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronics System Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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