VP1394

VIDCLOCK

The VIDCLOCK VP1394 user programmable clock generation circuit combines a Voltage Controlled Oscillator (VCO), Programmable Divider and Phase Detector to develop Phase Locked Loop (PLL) systems for controlling video clocking of graphics and video systems in an integrated environment. The VIDCLOCK VP1394 allows the designer to eliminate multiple crystal solutions. Lock with external video sources can be generated by digitally switching between the local oscillator and a dedicated video sync pulse. The VIDCLOCK VP1394 accommodates the special requirements that multimedia applications have for quickly switching from one lock to another.

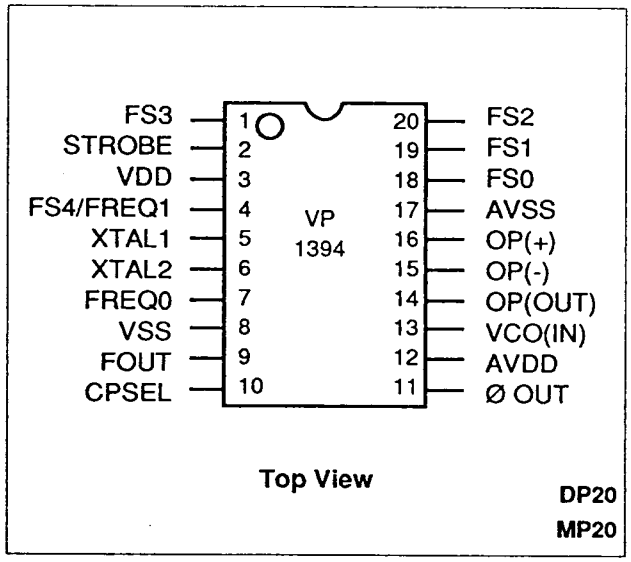


Fig.1 Device Pinout

FEATURES

- On-board Voltage Controlled Oscillator
- 32 programmable frequencies
- On chip voltage reference
- Low jitter phase detector design
- On chip clock conditioning circuitry
- CMOS for low dynamic power
- Dual input reference for genlock applications
- Fast frequency acquisition
- Surface mount packaging

APPLICATIONS

- Videographics Boards
- Multimedia
- EGA-VGA-Super VGA
- High Resolution MAC II Displays
- 8514A - XGA

ORDERING INFORMATION

VP1394A/CG/DPAS ROM Option A, DP20
VP1394A/CG/MPES ROM Option A, MP20
VP1394B/CG/DPAS ROM Option B, DP20
VP1394B/CG/MPES ROM Option B, MP20

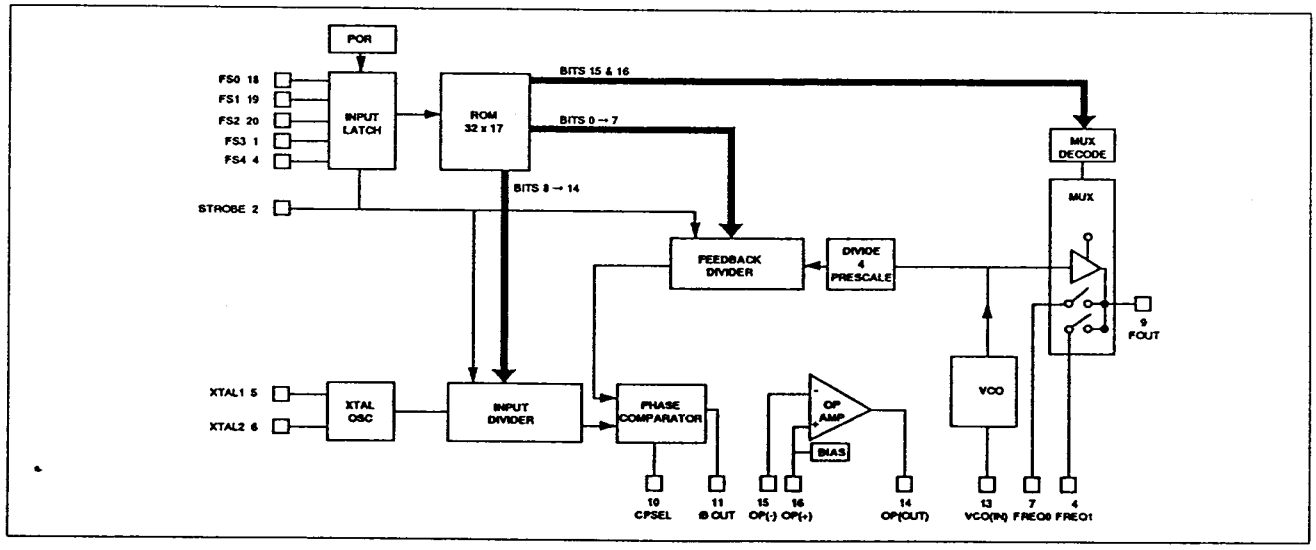


Fig.2 Block Diagram

CIRCUIT DESCRIPTION

The circuit consists of a crystal oscillator, a phase-locked loop and the associated digital control circuitry. It is designed to take a stable crystal derived frequency and generate a digitally controlled set of output frequencies. The output frequency set consists of 32 selections made through a 5 bit input word (FS4 : 0).

CRYSTAL OSCILLATOR

The crystal oscillator is a Pierce design where all the components except the crystal have been integrated. It will oscillate with crystals with nominal resonant frequencies between 10MHz and 20MHz. If the chip is used on a board where another stable frequency source is available, this frequency can be used by capacitively coupling to the oscillator input (pin 5). In this case, the oscillator output (pin 6) is left open. Finally, the crystal output can be used as a clock source for other chips, provided that a buffer is used to prevent excessive loading.

PHASED-LOCKED LOOP

The phase-locked loop consists of a phase comparator, charge pump, op amp filter, and VCO. The op amp can be configured as an inverting filter to provide the loop filter function. If desired, the charge pump polarity can be inverted by tying CPSEL (pin 10) to AVSS and a non inverting passive filter used.

DIGITAL CONTROL

The overall operation of the chip is determined by the digital inputs. The input latch used to select a ROM word, becomes transparent when the strobe pin is taken to logic 1. The contents of the selected ROM address are presented to the two dividers and the mux decode. The dividers are loaded with the ROM data on the first clock edge subsequent to the strobe going low (the minimum strobe high time is one clock cycle). The device may be ordered with the strobe feature disabled, in which case the latch is permanently transparent. (See the "User definable options" section). With this option, a delay will occur when a new frequency is selected whilst the dividers complete their current clock count.

The phase comparator can be used with inverting filter configurations by tying pin CPSEL high. An internal pull-up resistor is provided on CSPEL for this purpose. This causes the output of the phase comparator (Øout) to be inverted with respect to VCOIN. Non-inverting filters can be implemented by tying CSPEL low.

ROM CODING

Two standard factory coded ROM options (ROM options "A" and "B") are available - the frequency tables for each option are given on pages 4 and 5 respectively.

However, the user may also define a different frequency set by completing (and returning to GPS for review) the table contained in the "User Defined Options" section of this data sheet. Each of the 32 ROM locations store the associated feedback divider, input divider and output mux control values. The programmed frequency is generated according to the formula:-

$$FOUT = \frac{FEEDBACK\_DIVIDER \times 4 \times CRYSTAL\_FREQ}{INPUT\_DIVIDER}$$

Where FEEDBACK_DIVIDER is an integer value between 1 and 256 and INPUT_DIVIDER is an integer value between 1 and 128. As the output frequency (FOUT) is determined by the ratio of 2 integer values, not all frequencies can be programmed exactly. However, the vast majority of frequencies can be programmed within +/- 0.05%.

On receipt of the completed 'option table', the nearest attainable VCO frequencies are calculated by GPS, and the options table is returned for approval.

OUTPUT MUX

The output mux allows either one or two external signals, connected to FREQ0 (pin 7) and, if required, FS4/FREQ1 (pin 4) to be switched to FOUT. The signals are internally multiplexed, together with the internal locked frequency from the PLL, using analog switches. Output muxing is controlled by the internal ROM codes. If switching of two external frequencies is required, the number of ROM locations is restricted to 16 because the upper bit of the digital control word (FS4) is used as an input pin for FREQ1. When an external frequency (FREQ0 or FREQ1) is selected the internal PLL remains locked to a user defined frequency.

POWER ON RESET

On power up, the input latch is reset to zeros by the POR circuit. No other circuitry is cleared. In particular, the dividers will count from a random state, reloading either when completing their initial count or when a strobe pulse is issued.

TYPICAL OPERATING CHARACTERISTICS

Operating Temperature: Top = 0°C to 70°C, V_{DD} = 5V +/- 10%

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	DV_{DD}, AV_{DD}	4.5	5	5.5	Volts
Digital Supply Current (FOUT = 50MHz, int. osc.)	DI_{DD}		11	2.5	Milliamps
Digital Supply Current (FOUT = 50MHz, ext. clock)	DI_{DD}		10		Milliamps
Analog Supply Current (FOUT = 50MHz)	AI_{DD}		3.2	4.5	Milliamps
Digital Supply Current (FOUT = 120MHz)	DI_{DD}		20	30	Milliamps
Analog Supply Current (FOUT = 120MHz)	AI_{DD}		9.6	15	Milliamps
Ouput Impedance	Z_{OUT}		33	100	Ohms
Ouput Drive Current	ISOURCE, ISINK		4		Milliamps
Op Amp Characteristics					
Output Swing (Open circuit)		AV_{SS}		AV_{DD}	Volts
Gain-Bandwidth Product	V_{GBW}		8		MHz
Phase Comparator					
Gain Constant	Kø		0.4		Volts/Rad
Bus Timing					
Setup Time (FS0-FS3 relative to STROBE)	T_{SETUP}	10			nS
Hold Time (FS0-FS3 relative to STROBE)	T_{HOLD}	10			nS
VCO					
Max operating freq.	F_{MAX}			110	MHz
Min operating freq.	F_{MIN}	20			MHz

ABSOLUTE MAXIMUM RATING

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD} +0.5V
Output Voltage	V_{OUT}	-0.5V to V_{DD} + 0.5V
Clamp Diode Current	I_{IK} & I_{OK}	+/- 30mA
Output Current per Pin	I_{OUT}	+/- 50mA
Storage Temperature	T_s	-55°C to +125°C

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltage or electric fields; however it is advised that normal precautions be taken to aviod applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to >= V_{SS} and <= V_{DD}

OUTPUT FREQUENCY TABLE (ROM OPTION A)

Input Frequency = 14.31818MHz
Input Latch = Transparent

Location	FOUT Frequency (MHz)
00	25.175
01	28.322
02	40.000
03	32.506
04	50.331
05	65.012
06	37.998
07	44.889
08	See Address 00
09	See Address 01
0A	See Address 02
0B	See Address 03
0C	49.983
0D	See Address 05
0E	31.500
0F	36.000
10	See Address 00
11	See Address 01
12	30.000
13	See Address 0E
14	See Address 03
15	See Address 0F
16	See Address 06
17	See Address 02
18	See Address 07
19	47.985
1A	See Address 0C
1B	50.000
1C	64.091
1D	65.012
1E	74.975
1F	80.000

OUTPUT FREQUENCY TABLE (ROM OPTION B)

Input Frequency = 14.31818MHz
Input Latch = Transparent

Location	Actual Frequency
00	FREQ0
01	FREQ0
02	FREQ0
03	FREQ0
04	FREQ0
05	FREQ0
06	FREQ0
07	FREQ0
08	FREQ0
09	FREQ0
0A	FREQ0
0B	FREQ0
0C	FREQ0
0D	FREQ0
0E	FREQ0
0F	FREQ0
10	25.175
11	28.322
12	30.000
13	31.500
14	32.506
15	36.000
16	37.998
17	40.000
18	44.890
19	47.985
1A	49.983
1B	60.000
1C	64.091
1D	65.012
1E	74.975
1F	80.000

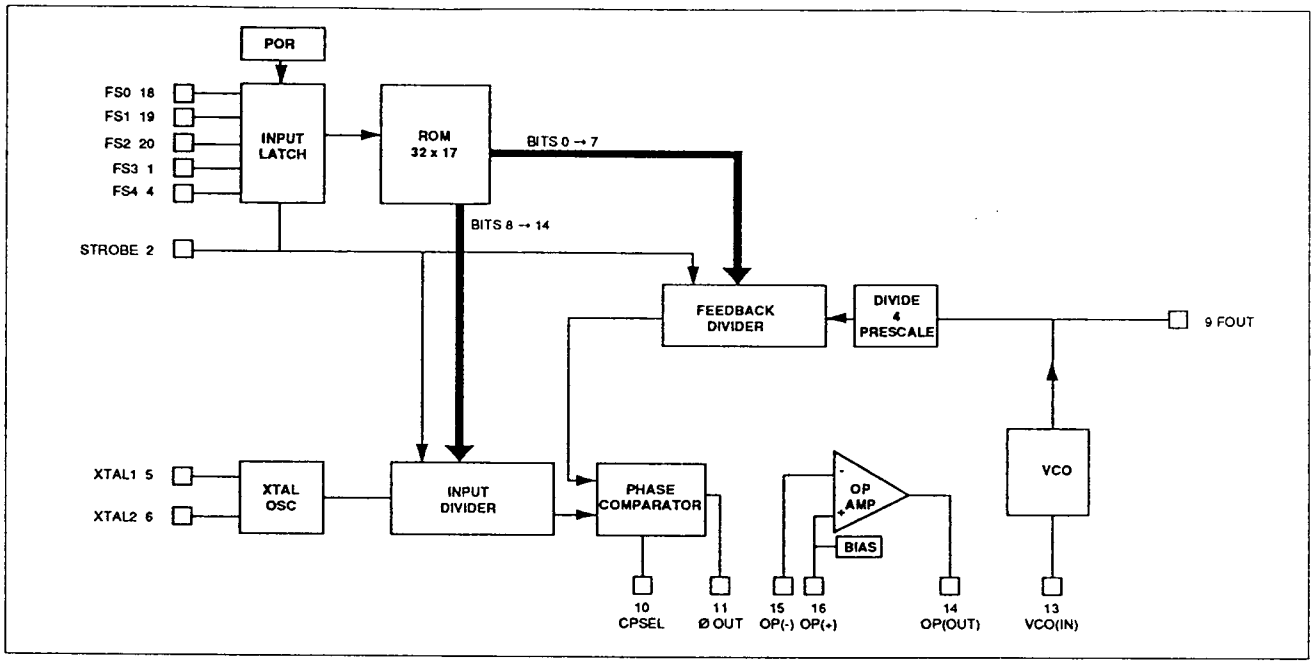


Fig.3 ROM Option A Block Diagram

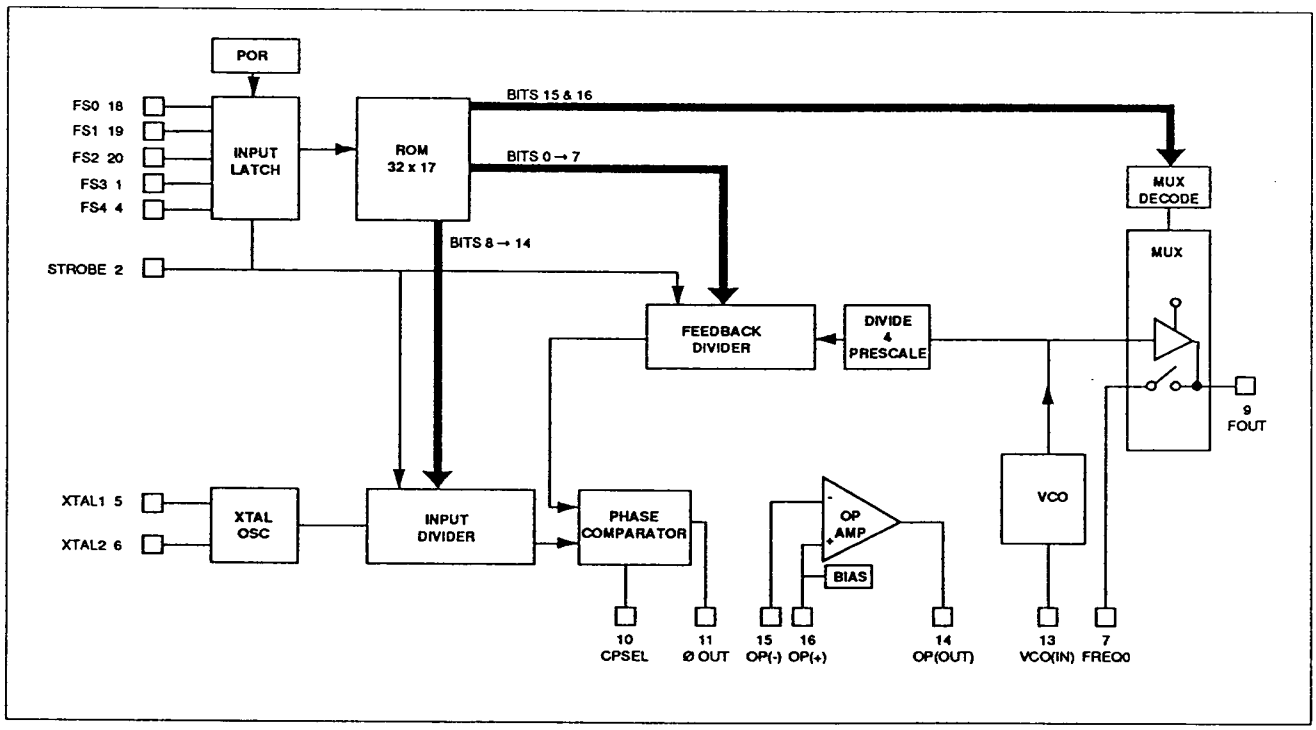


Fig.4 ROM Option B Block Diagram

USER DEFINABLE OPTIONS FOR THE VP1394

PROGRAMMABLE FREQUENCIES -
Each location in the table below requires the required VCO FREQ to be defined along with the selected MUX option (tick one from VCO, FREQ0 or FREQ1).

LOCATION	MUX OPTION			REQUIRED VCO FREQ (MHZ)	GPS USE ONLY ACTUAL VCO FREQ (MHz)
	VCO	FO	F1*		
00					
01					
02					
03					
04					
05					
06					
07					
08					
09					
0A					
0B					
0C					
0D					
0E					
0F					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
1A					
1B					
1C					
1D					
1E					
1F					

* Selecting FREQ1, reduces available ROM locations from 32 to 16.

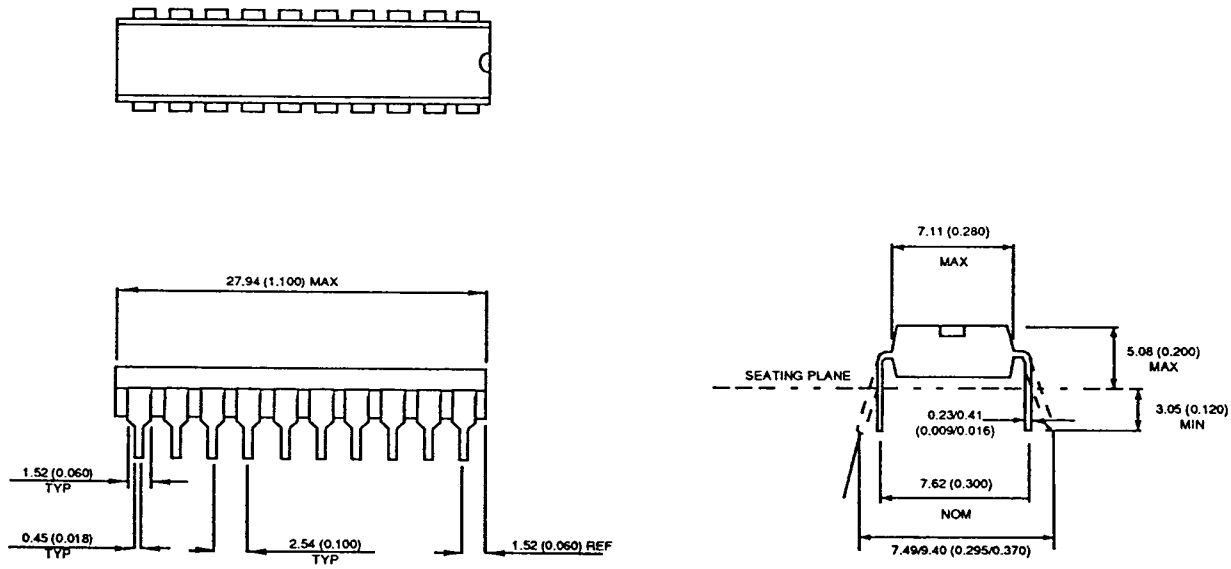
STROBE OPTION - (TICK REQUIRED OPTION) ACTIVE [ ] NOT ACTIVE [ ]
If strobe option 'ACTIVE' is selected, the input latch becomes transparent when strobe is taken high; The dividers load the selected ROM data when strobe returns low. 'NOT ACTIVE', defines the input to be permanently transparent. The dividers under this option, complete their previous count prior to loading the new ROM data.

MUX OPTION - (TICK REQUIRED OPTION) FREQ0 &FREQ1 [ ] FREQ0 ONLY [ ]
If 'FREQ0' is selected, just one pin is available (Pin7) for selecting external frequencies. Under this option, all 32 RAM locations require specification above if option 'FREQ0 & FREQ1' is selected, two pins (7 and 4) are defined as external frequency select pins. Under this option, only the first 16 locations require specification.

CRYSTAL FREQUENCY - (DEFINE FREQUENCY) XTAL = [ ] MHz
Please define, to allow computation of the feedback and input divider values to be stored in ROM.

When complete, please return to your GEC Plessey Semiconductors representative for review.

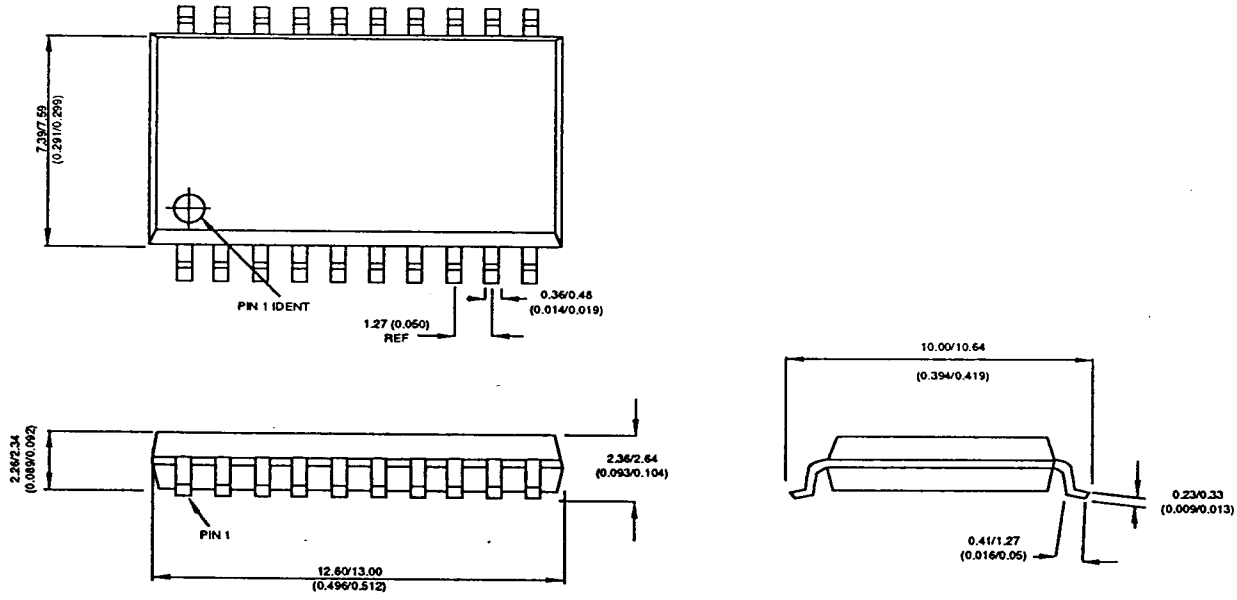
PACKAGE OPTIONS



20 LEAD PLASTIC DIL - DP20

PACKAGE OPTIONS

Dimensions are shown thus: mm (in).



20-LEAD MINIATURE PLASTIC DIL - MP20

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