8-BIT SINGLE-CHIP MICROCONTROLLER

The µPD789800 is a 78K/0S series product designed for a USB keyboard (for ASSP).

The µPD789800 has on-chip hardware compatible with a USB keyboard, including USB (Universal Serial Bus) functions, a regulator which powers a USB driver/receiver, and a key return signal detection circuit.

The µPD78F9801, a product with on-chip flash memory which can operate on the same supply voltage as for masked ROM products and various development tools are also available.

Detailed descriptions of its functions, etc., are given in the following user's manuals. Be sure to read them for design purposes.

µPD789800 Sub-Series User's Manual : U12978E

78K/0S Series User's Manual, Instruction : U11047E

FEATURES

- On-chip USB functions
  - Implements a USB (Universal Serial Bus) by connecting to Hub and Host.
  - Transfer speed: 1.5 Mbps (when the system clock operates at 6.0 MHz)
- On-chip regulator
  - Controls the USB port voltage by using a bus power supply (V_{REG} = 3.3 ±0.3 V) dedicated to the USB driver/receiver.
- On-chip ROM and RAM
  - Internal ROM : 8K bytes
  - Internal high-speed RAM : 256 bytes
- Minimum instruction execution time can be switched between high speed (0.33 µs) and low speed (1.33 µs) (when the system clock operates at 6.0 MHz).
- I/O port: 31
- Serial interface: 2 channels
  - USB function : 1 channel
  - Three-wire serial I/O mode : 1 channel
- Timer: 3 channels
  - 8-bit timer : 1 channel
  - 8-bit timer/event counter : 1 channel
  - Watchdog timer : 1 channel
- On-chip key return signal detection circuit
- Supply voltage: V_{DD} = 4.0 to 5.5 V
- Operating ambient temperature : T_A = -40°C to +85°C (when the USB is not operating)
  T_A = 0°C to +70°C (when the USB is operating)

The mark ★ shows major revised points.

APPLICATIONS

USB keyboards, etc.

ORDERING INFORMATION

Part number	Package
μPD789800GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10)
μPD789800GB-×××-8ES	44-pin plastic LQFP (10 × 10)

Remark ××× indicates ROM code suffix.

★ **78K/0S SERIES DEVELOPMENT**

The 78K/0S series products are shown below. The sub-series names are indicated in frames.

Products in mass production

Products under development
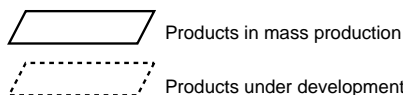
Y subseries supports SMB.

Small-scale package, general-purpose applications

Pin	Product	Description
44-pin	μPD789046	μPD789074 with subsystem clock
42-/44-pin	μPD789026	μPD789014 with enhanced timer function and expanded ROM and RAM
30-pin	μPD789074	μPD789026 with enhanced timer function
28-pin	μPD789014	On-chip UART and capable of low-voltage (1.8 V) operation

Small-scale package, general-purpose applications and A/D function

Pin	Product		Description
44-pin	μPD789177	μPD789177Y	μPD789167 with enhanced A/D converter
44-pin	μPD789167	μPD789167Y	μPD789104A with enhanced timer
30-pin	μPD789156		μPD789146 with enhanced A/D converter
30-pin	μPD789146		μPD789104A with EEPROM™ added
30-pin	μPD789134A		μPD789124A with enhanced A/D
30-pin	μPD789124A		RC oscillation version of μPD789104A
30-pin	μPD789114A		μPD789104A with enhanced A/D converter
30-pin	μPD789104A		μPD789026 with A/D converter and multiplier

Inverter control

Pin	Product	Description
44-pin	μPD789842	On-chip inverter controller and UART

78K/0S Series

VFD drive

Pin	Product	Description
52-pin	μPD789871	Total of display outputs: 25

LCD drive

Pin	Product	Description
80-pin	μPD789488	A/D converter and internal voltage boosting method LCD (28 × 4)
80-pin	μPD789417A	μPD789407A with enhanced A/D converter
80-pin	μPD789407A	A/D converter and resistance division method LCD (28 × 4)
64-pin	μPD789456	μPD789446 with enhanced A/D converter
64-pin	μPD789446	A/D converter and internal voltage boosting method LCD (15 × 4)
64-pin	μPD789436	μPD789426 with enhanced A/D converter
64-pin	μPD789426	A/D converter and internal voltage boosting method LCD (5 × 4)
64-pin	μPD789316	RC oscillation version of μPD789306
64-pin	μPD789306	Internal voltage boosting method LCD (24 × 4)

Dot LCD drive

Pin	Product	Description
144-pin	μPD789835	Segment/common outputs: 96 pins
88-pin	μPD789830	Segment: 40 pins, common: 16 pins

ASSP

Pin	Product	Description
80-pin	μPD789477	μPD789488 with remote controller receive circuit added and resistance division method LCD
52-pin	μPD789467	For remote controller. On-chip A/D converter and internal voltage boosting method LCD
52-pin	μPD789327	For remote controller. On-chip SIO and resistance division method LCD
44-pin	μPD789800	For PC keyboard. On-chip USB function
44-pin	μPD789840	For key pad. On-chip POC
20-pin	μPD789861	RC oscillation version of μPD789860
20-pin	μPD789860	For keyless entry. On-chip POC and key return circuit

The major functional differences among the subseries are listed below.

Function / Subseries Name		ROM Capacity	8-Bit	16-Bit	Watch	WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	VDD MIN Value	Remark
Small scale, general-purpose applications	µPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	µPD789026	4 K to 16 K		–								
	µPD789074	2 K to 8 K								24		
	µPD789014	2 K to 4 K	2 ch	–						22		
Small-scale, general-purpose applications + A/D function	µPD789177	16 K to 24 K	3 ch	1 ch	1 ch		–	8 ch	1 ch (UART: 1 ch)	31		–
	µPD789167						8 ch	–				
	µPD789156	8 K to 16 K	1 ch			–	–	4 ch		20		On-chip EEPROM
	µPD789146						4 ch	–				
	µPD789134A	2 K to 8 K						4 ch				RC oscillation version
	µPD789124A						4 ch	–				
	µPD789114A						–	4 ch				–
	µPD789104A						4 ch	–				
Inverter control	µPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
VFD drive	µPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
LCD drive	µPD789488	32 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	µPD789417A	12 K to 24 K						7 ch	1 ch (UART: 1 ch)	43		
	µPD789407A						7 ch	–				
	µPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	µPD789446						6 ch	–				
	µPD789436						–	6 ch		40		
	µPD789426						6 ch	–				
	µPD789316	8 K to 16 K						–	2 ch (UART: 1 ch)	23		RC oscillation version
	µPD789306											–
Dot LCD drive	µPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28	1.8 V	–
	µPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
ASSP	µPD789477	24 K	3 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch (UART: 1 ch)	45	1.8 V	On-chip LCD
	µPD789467	4 K to 24 K	2 ch	–			1 ch		–	18		
	µPD789327						–		1 ch	21		
	µPD789800	8 K			–				2 ch (USB: 1 ch)	31	4.0 V	–
	µPD789840						4 ch		1 ch	29	2.8 V	
	µPD789861	4 K					–		–	14	1.8 V	RC oscillation version, on-chip EEPROM
	µPD789860											On-chip EEPROM

Note   10-bit timer: 1 channel

FUNCTIONS

Item		Function
Internal memory	ROM	8K bytes
	High-speed RAM	256 bytes
Minimum instruction execution time		0.33 μs/1.33 μs (when the system clock operates at 6.0 MHz)
General-purpose register		8 bits $\times$ 8 registers
Instruction set		• 16-bit operation • Bit manipulation (set, reset, and test) etc.
I/O ports		CMOS I/O: 31 pins (Of these, 18 pins can be switched to N-ch open-drain I/O pins.)
Serial interface		• USB (Universal Serial Bus) function : 1 channel • Three-wire serial I/O mode : 1 channel
Timer		• 8-bit timer : 1 channel • 8-bit timer/event counter : 1 channel • Watchdog timer : 1 channel
Regulator		Incorporated (V$_{REG}$ = 3.3 $\pm$0.3 V)
Vector interrupt source	Maskable	Internal: 9, external: 2
	Nonmaskable	Internal: 1
Power supply voltage		V$_{DD}$ = 4.0 to 5.5 V
Operating ambient temperature		• T$_A$ = -40°C to +85°C (when the USB is not operating) • T$_A$ = 0°C to +70°C (when the USB is operating)
Package		• 44-pin plastic QFP (10 $\times$ 10) • 44-pin plastic LQFP (10 $\times$ 10)

CONTENTS

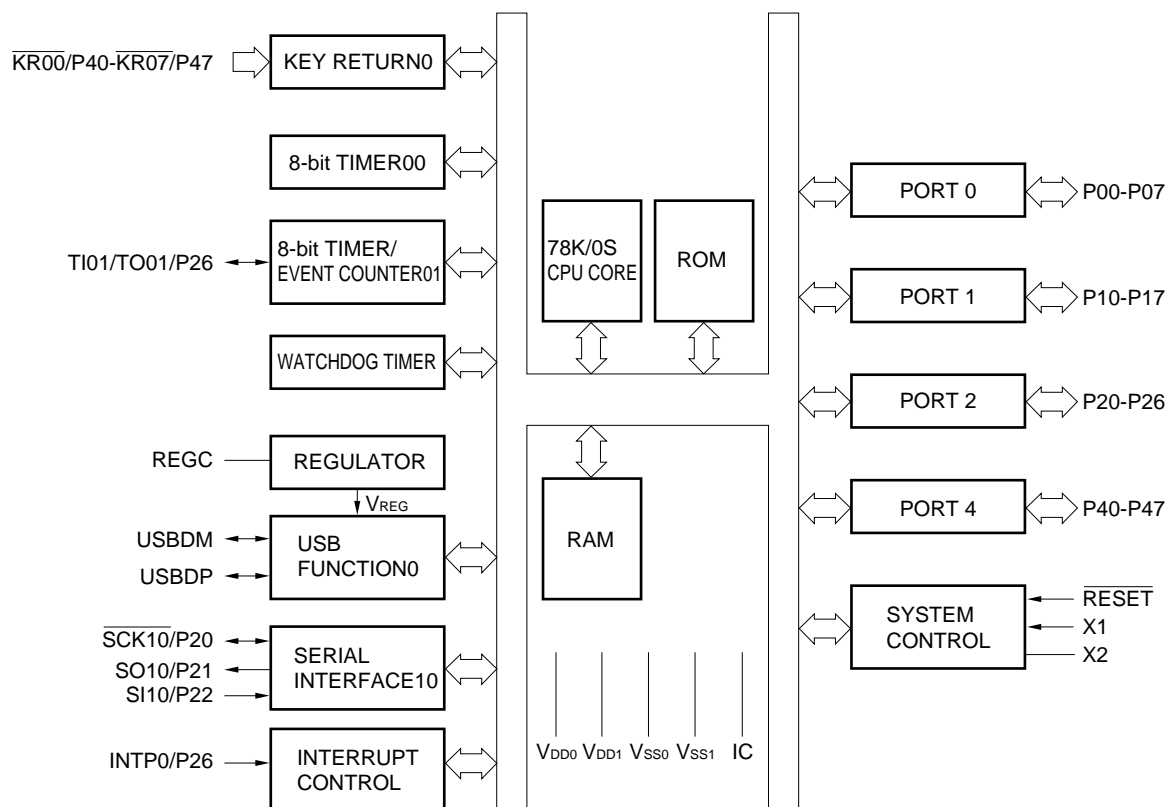## 1. PIN CONFIGURATION (TOP VIEW)

- 44-pin plastic QFP (10 × 10)
  µPD789800GB-×××-3BS-MTX
- 44-pin plastic LQFP (10 × 10)
  µPD789800GB-×××-8ES
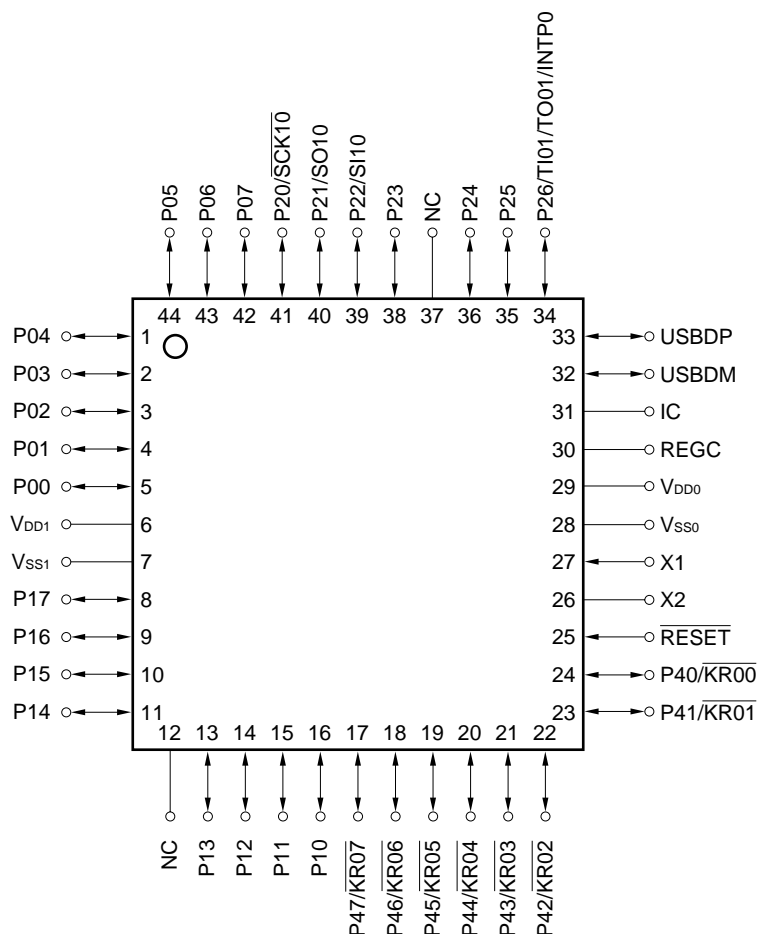
Caution   Connect the IC (Internally Connected) pin directly to the V_{SS0} or V_{SS1} pin.

IC	: Internally connected	$\overline{SCK10}$	: Serial clock input/output
INTP0	: Interrupt from peripherals	SI10	: Serial data input
$\overline{KR00}$ - $\overline{KR07}$	: Key return	SO10	: Serial data output
NC	: No connection	TI01	: Timer input
P00-P07	: Port 0	TO01	: Timer output
P10-P17	: Port 1	USBDM, USBDP	: Universal serial bus data
P20-P26	: Port 2	V_{DD0}, V_{DD1}	: Power supply
P40-P47	: Port 4	V_{SS0}, V_{SS1}	: Ground
$\overline{RESET}$	: Reset	X1, X2	: Crystal
REGC	: Voltage regulator for USB function		

2. BLOCK DIAGRAM

3. PIN FUNCTIONS

3.1 Port Pins

Pin name	I/O	Function	When reset	Also used as
P00-P07	I/O	Port 0 8-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software. CMOS output or N-ch open-drain output is specifiable in 8-bit units.	Input	-
P10-P17	I/O	Port 1 8-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software. CMOS output or N-ch open-drain output is specifiable in 8-bit units.	Input	-
P20	I/O	Port 2 7-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software. Only for P25 and P26, CMOS output or N-ch open-drain output is specifiable bit by bit.	Input	$\overline{\text{SCK10}}$
P21				SO10
P22				SI10
P23-P25				-
P26				INTP0/TI01/TO01
P40-P47	I/O	Port 4 8-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software.	Input	$\overline{\text{KR00}}$ - $\overline{\text{KR07}}$

3.2 Non-Port Pins

Pin name	I/O	Function	When reset	Also used as
INTP0	Input	External interrupt request input for which effective edges (rising and/or falling edges) can be specified	Input	P26/TI01/TO01
$\overline{\text{KR00}}$ - $\overline{\text{KR07}}$	Input	Input for detecting key return signals	Input	P40-P47
★ REGC	-	Internally generated power supply for driving USB driver/receiver. Connect this pin to Vss through a 220-Ω resistor and a 0.1-μF capacitor.	-	-
$\overline{\text{RESET}}$	Input	System reset input	Input	-
$\overline{\text{SCK10}}$	I/O	Serial clock input/output for serial interface	Input	P20
SI10	Input	Serial data input for serial interface	Input	P22
SO10	Output	Serial data output for serial interface	Input	P21
TI01	Input	External count clock input to 8-bit timer/event counter 01	Input	P26/INTP0/TO01
TO01	Output	Timer output from 8-bit timer/event counter 01	Input	P26/INTP0/TI01
USBDM	I/O	Serial data input/output (negative side) for USB function. The pull-up resistor (1.5 kΩ) for the USBDM pin must be connected to the REGC pin.	Input	-
USBDP	I/O	Serial data input/output (positive side) for USB function	Input	-
X1	Input	Connected to crystal for system clock oscillator	Input	-
X2	-		-	
V$_{DD0}$	-	Positive supply voltage for ports	-	-
V$_{DD1}$	-	Positive supply voltage for circuits other than ports	-	-
V$_{SS0}$	-	Ground potential for ports	-	-
V$_{SS1}$	-	Ground potential for circuits other than ports	-	-
IC	-	Internally connected. Connect this pin directly to V$_{SS0}$.	-	-
NC	-	Not internally connected. Leave this pin open.	-	-

### 3.3 Pin Input/Output Circuits and Handling of Unused Pins

Table 3-1 lists the types of input/output circuits for each pin and explains how unused pins are handled.

Figure 3-1 shows the configuration of each type of input/output circuit.

Table 3-1. Type of Input/Output Circuit for Each Pin

| Pin name	I/O circuit type	I/O	Recommended connection of unused pins
P00-P07	5-R	I/O	Input : Connect these pins separately to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via respective resistors.
P10-P17			Output : Leave these pins open.
P20/$\overline{SCK10}$	8-C		
P21/SO10			
P22/SI10			
P23, P24			
P25	8-F		
P26/INTP0/TI01/TO01			
P40/$\overline{KR00}$ -P47/$\overline{KR07}$	8-C		
USBDM	24-A		Connect this pin to the REGC pin.
USBDP			Connect this pin to V_{SS0} or V_{SS1} via resistors.
$\overline{RESET}$	2	Input	-
IC	-	-	Connect this pin directly to V_{SS0} or V_{SS1}.
NC	-	-	Leave this pin open.
REGC	-	-	Connect this pin to the USBDM pin.

Figure 3-1. Pin Input/Output Circuits
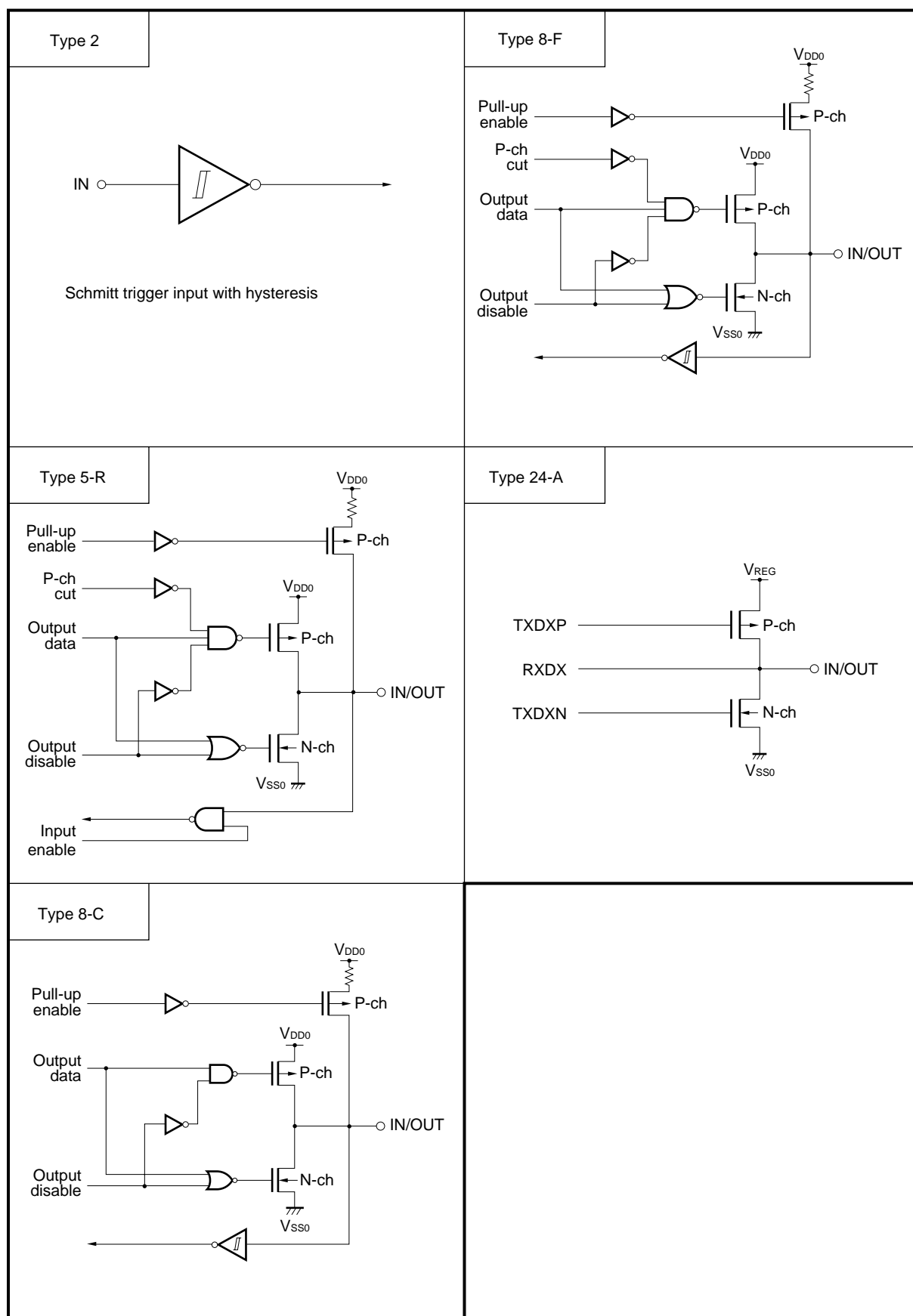
4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD789800.

Figure 4-1. Memory Map
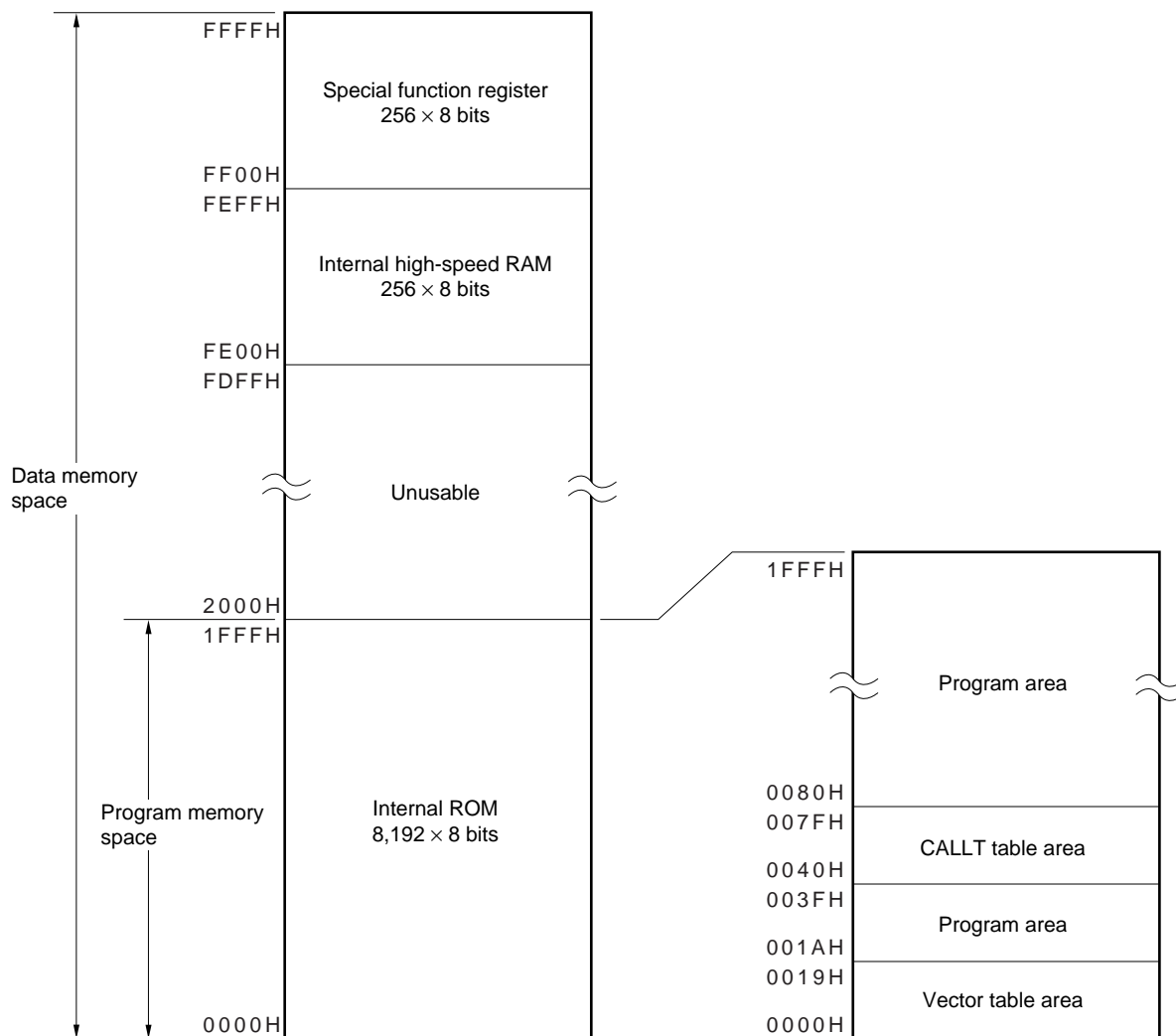
5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

I/O ports are listed below.

- CMOS input/output ports (ports 0 to 2 and port 4): 31 pins
  Of these, 18 pins (pins of ports 0 and 1, P25, and P26) can be switched to N-ch open-drain input/output pins.

Table 5-1. Port Functions

| Name	Pin name	Function
Port 0	P00-P07	Input/output port. Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software. CMOS output or N-ch open-drain output is specifiable in 8-bit units.
Port 1	P10-P17	Input/output port. Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software. CMOS output or N-ch open-drain output is specifiable in 8-bit units.
Port 2	P20-P24	Input/output port. Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software.
	P25, P26	Input/output port. Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software. Only for P25 and P26, CMOS output or N-ch open-drain output is specifiable.
Port 4	P40-P47	Input/output port. Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software.

5.2 Clock Generator

The *µ*PD789800 has an on-chip system clock generator.
It is possible to change the minimum instruction execution time.

- 0.33 *µ*s/ 1.33 *µ*s (when the system clock operates at 6.0 MHz)

Figure 5-1. Block Diagram of Clock Generator
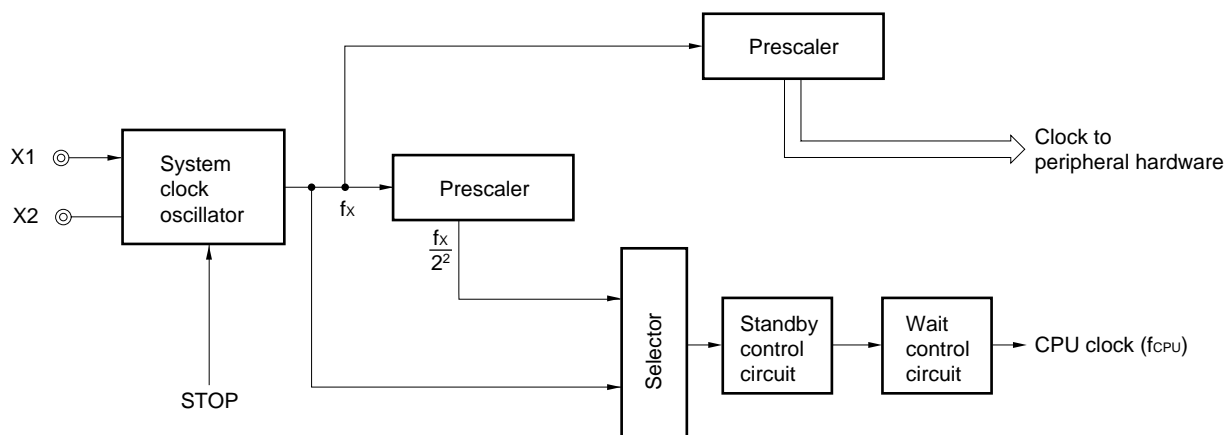
5.3 Timer

The μPD789800 has three on-chip timers.

- 8-bit timer 00 : 1 channel
- 8-bit timer/event counter 01 : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Timer Operation

		8-bit timer 00	8-bit timer/event counter 01	Watchdog timer
Operation mode	Interval timer	1 channel	1 channel	1 channel
	External event counter	-	1 channel	-
Function	Timer output	-	1 output	-
	Square wave output	-	1 output	-
	Interrupt request	1	1	1

Figure 5-2. Block Diagram of 8-Bit Timer 00

Internal bus

8-bit compare register 00 (CR00)

Match

INTTM00

$f_X/2^6$

$f_X/2^9$

Selector

8-bit timer counter 00 (TM00)

Clear

Internal bus
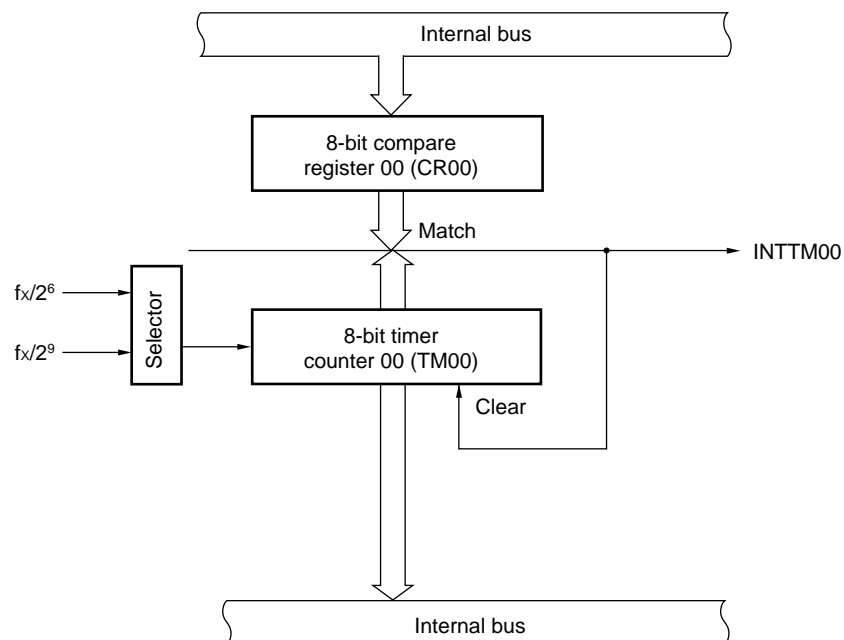
Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 01
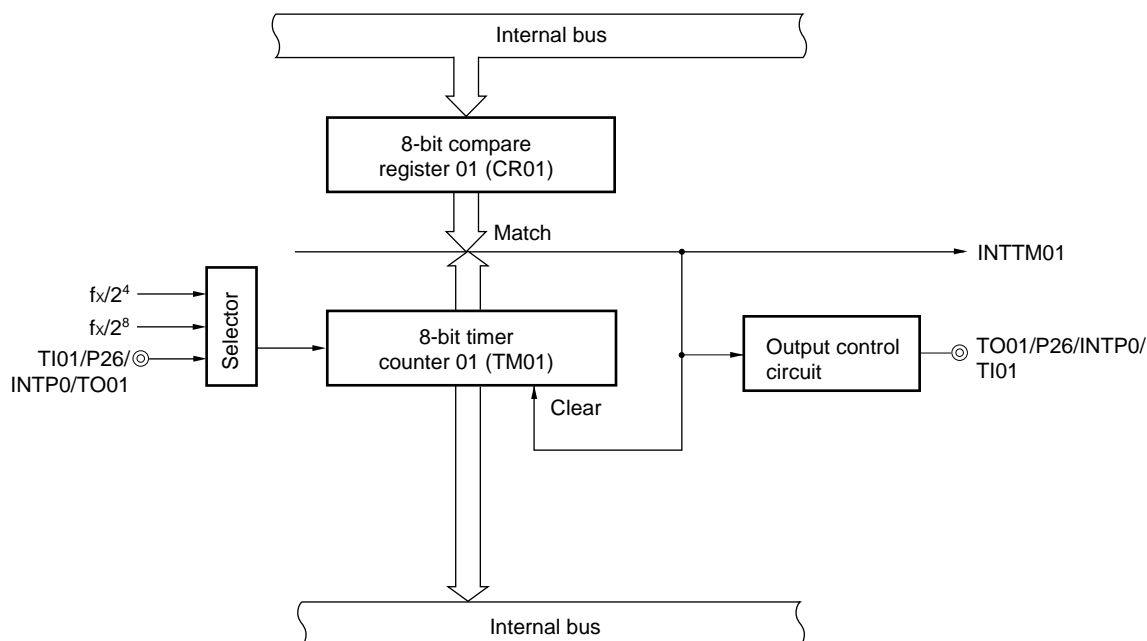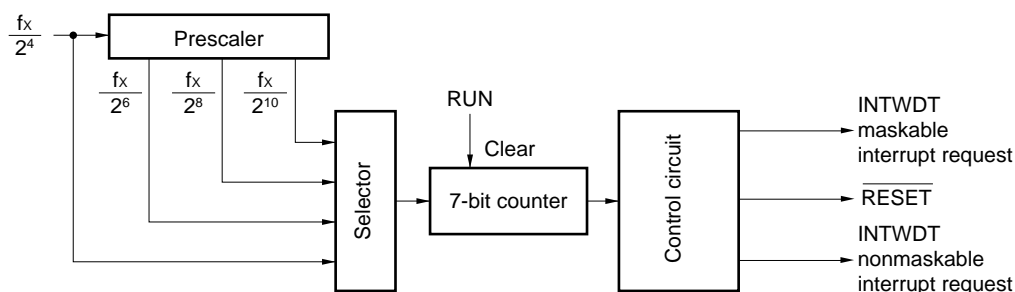

Figure 5-4. Block Diagram of Watchdog Timer

5.4 Serial Interface

Two channels of serial interface are on chip.

- **USB function**

    The μPD789800 supports 1.5 Mbps transfer speed with the system clock of 6.0 MHz and incorporates an NRZI (Non Return Zero Invert) decode/encode function, bit stuffing function, and CRC (Cyclic Redundancy Check) function specified by the USB (Universal Serial Bus) communication protocol.

    Figure 5-5 shows a block diagram.

- **Serial interface 10 (SIO10)**

    SIO10 has the following two modes:

    - Operation stop mode
    - Three-wire serial I/O mode (The first bit can be switched between the MSB and LSB.)

    Figure 5-6 shows a block diagram.
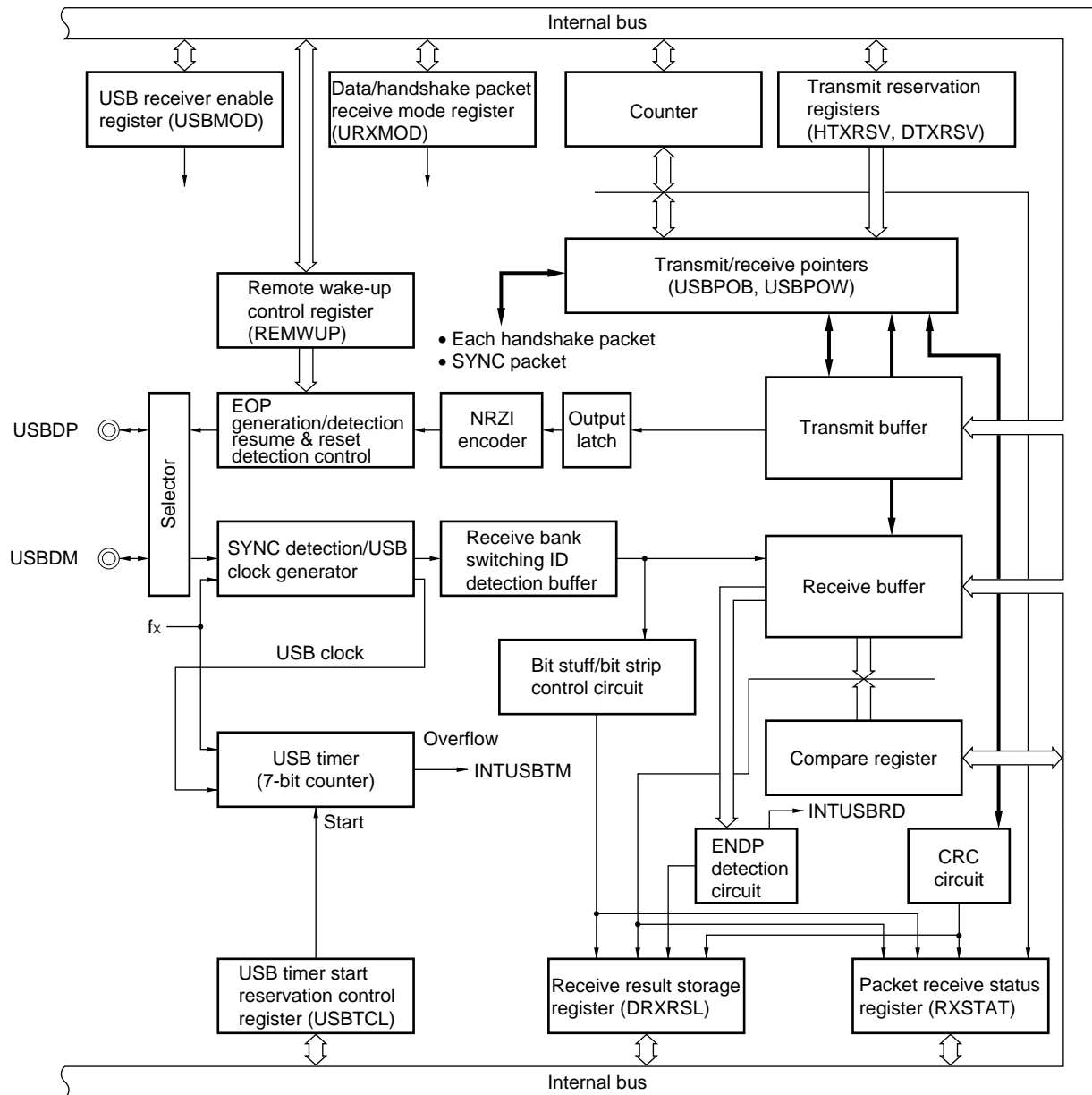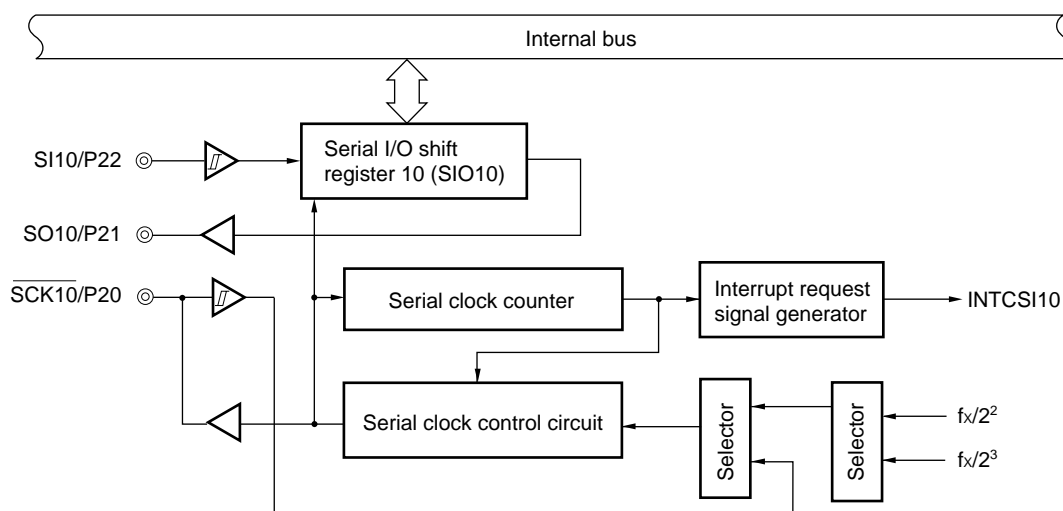
Figure 5-5. Block Diagram of USB Function

**Figure 5-6. Block Diagram of Serial Interface 10**

5.5 Regulator

The μPD789800 incorporates a regulator which powers the USB driver/receiver. The features are as follows:

- Generates V_{REG} (3.3 ±0.3 V) from V_{DD0} and V_{DD1} (4.0 to 5.5 V) and outputs it to the REGC pin.
- Supports power-saving mode, reducing current dissipation during STOP mode.

Figure 5-7. Block Diagram of the Regulator and USB Driver/Receiver
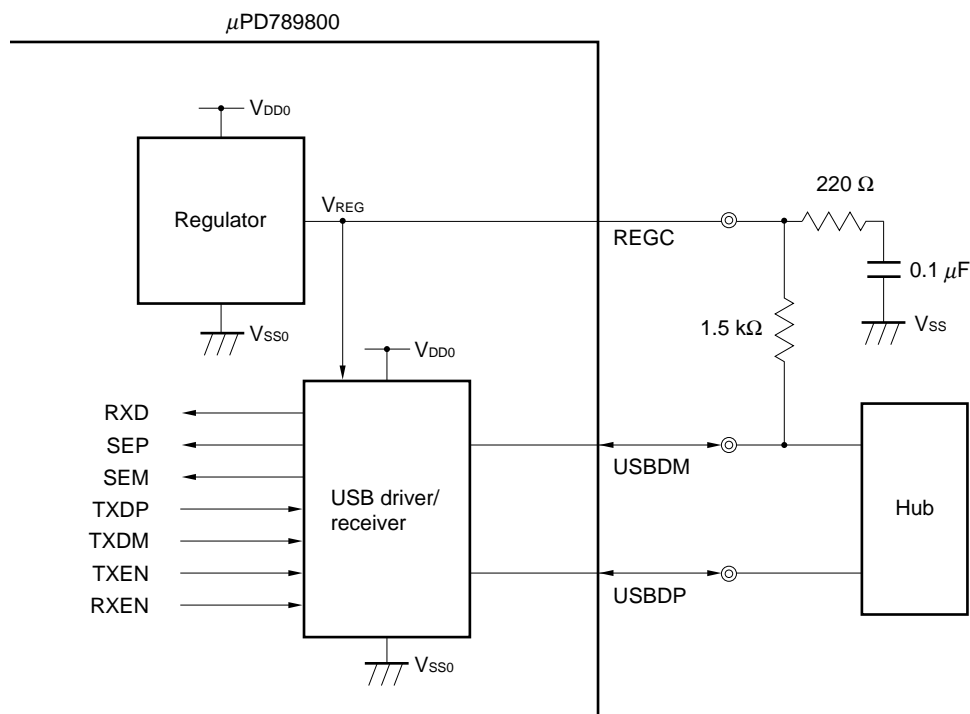
Cautions 1. To settle the V_{REG} voltage, connect the REGC pin to V_{SS} via a 220-Ω resistor and a 0.1-μF capacitor.

2. Connect the pull-up resistor (1.5 kΩ), for the USBDM pin, to the REGC pin.

5.6 Key Return Signal Detection Circuit

The μPD789800 incorporates the key return signal detection circuit that can detect the key return signals input to the P40/$\overline{\text{KR00}}$-P47/$\overline{\text{KR07}}$ pins.

Specify whether to detect the key return signals at the P40/$\overline{\text{KR00}}$-P47/$\overline{\text{KR07}}$ pins by means of key return mode register 00 (KRM00). Inhibit interrupts before setting KRM00 (see **Caution 3**).

KRM00 is set by a 1-bit memory operation instruction or an 8-bit memory operation instruction.

Bit 0 (KRM000) corresponds to the $\overline{\text{KR00}}$/P40-$\overline{\text{KR03}}$/P43 pins. Its setting is common to these four pins. Bits 4 to 7 (KRM004-KRM007) correspond to the $\overline{\text{KR04}}$/P44-$\overline{\text{KR07}}$/P47 pins respectively and are set bit by bit.

Inputting the $\overline{\text{RESET}}$ signal clears KRM00 to 00H.

Figure 5-8 shows the format of key return mode register 00. Figure 5-9 shows the block diagram of the falling edge detection circuit.

Figure 5-8. Format of Key Return Mode Register 00

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
KRM00	KRM007	KRM006	KRM005	KRM004	0	0	0	KRM000	F F F 5 H	0 0 H	R/W

KRM00n	Selection of key return signal detection for the P4n/$\overline{\text{KR0n}}$ pin (n = 4 to 7)
0	No detection
1	Detection (detecting the falling edges of the P4n/$\overline{\text{KR0n}}$ signals)

KRM000	Selection of key return signal detection for the P40/$\overline{\text{KR00}}$-P43/$\overline{\text{KR03}}$ pins
0	No detection
1	Detection (detecting the falling edges of the P40/$\overline{\text{KR00}}$-P43/$\overline{\text{KR03}}$ signals)

Cautions 1. Be sure to set 0 in bits 1 to 3.
2. **When KRM00 is set to 1, the pull-up resistor is forcibly connected to the corresponding pin. However, when the pin is placed in output mode, the pull-up resistor is disconnected.**
3. **Before setting KRM00, inhibit interrupts (set bit 4 of interrupt mask flag register 0 (MK0) (KRMK00 = 1). After setting KRM00, clear bit 4 of interrupt request flag register 0 (IF0) (KRIF00 = 0), then permit interrupts (clear bit 4 of MK0 (KRMK00 = 0)).**

Figure 5-9. Block Diagram of Falling Edge Detection Circuit
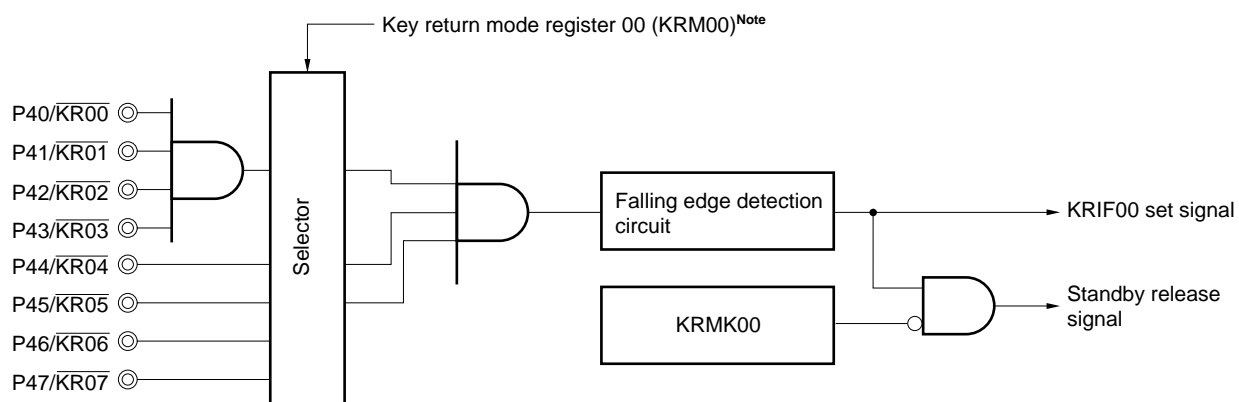
Note Register that selects the pin used for falling edge input

6. INTERRUPT FUNCTION

There are two types and 12 sources of interrupt function as shown below.
- Nonmaskable interrupt: 1 source
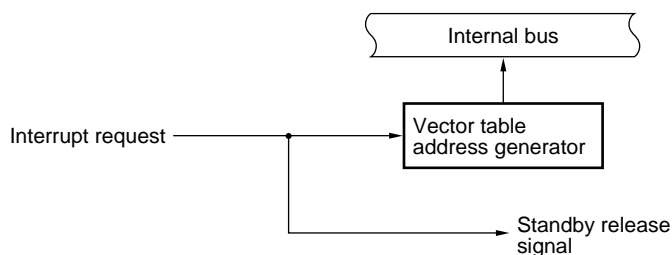- Maskable interrupts : 11 sources

Table 6-1. Interrupt Source List

Type of interrupt	Priority[Note 1]	Interrupt source		Internal/ external	Vector table address	Basic configuration type[Note 2]
		Name	Trigger			
Nonmaskable	-	INTWDT	Watchdog timer overflow (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer mode is selected)			(B)
	1	INTUSBTM	USB timer overflow		0006H	
	2	INTUSBRT	EOP detection when a USB token packet is received		0008H	
	3	INTUSBRD	EOP detection when a USB data/handshake packet is received		000AH	
	4	INTUSBST	EOP detection when a USB data/handshake packet is sent		000CH	
	5	INTUSBRE	Detection of transition from J state to K state or SE0 on the USB bus		000EH	
	6	INTP0	Detection of a pin input edge	External	0010H	(C)
	7	INTCSI10	End of three-wire SIO bus interface transmission and reception	Internal	0012H	(B)
	8	INTTM00	Generation of the 8-bit timer counter 00 match signal		0014H	
	9	INTTM01	Generation of the 8-bit timer/event counter 01 match signal		0016H	
	10	INTKR00	Detection of the key return signal	External	0018H	(C)

Notes 1. The priority is the order of priority when multiple maskable interrupts are generated simultaneously. 0 is the highest priority and 10 is the lowest priority.

2. Types (A) to (C) in the basic configuration correspond to (A) to (C) in Figure 6-1, respectively.
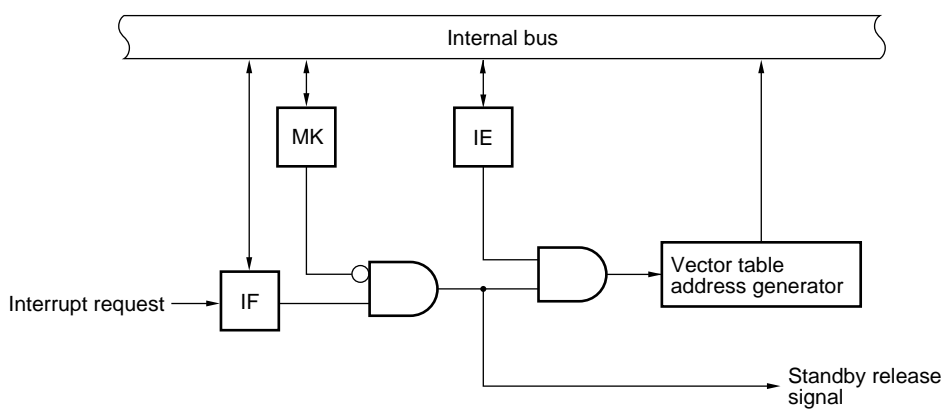
Remark Only one of the two watchdog timer interrupt sources, non-maskable or maskable (internal), can be selected.

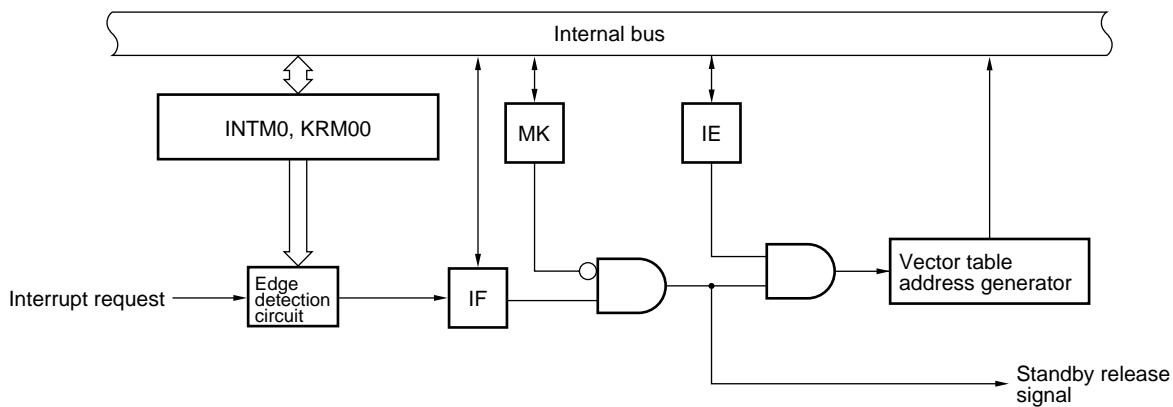**Figure 6-1. Basic Configuration of Interrupt Function**

(A) Internal nonmaskable interrupt

```
                                    ⟨  Internal bus  ⟩
                                            ↑
                                    ┌───────────────┐
Interrupt request ─────────●──────→ │ Vector table  │
                           │        │ address generator │
                           │        └───────────────┘
                           │
                           └──────────→ Standby release
                                        signal
```

(B) Internal maskable interrupt

```
        ⟨                    Internal bus                    ⟩
              ↑     ↕           ↕                    ↑
            ┌───┐ ┌───┐       ┌───┐
            │   │ │MK │       │IE │
            │   │ └───┘       └───┘
            │   │   │           │
                                        ┌───────────────┐
Interrupt request →┌──┐        ┌──┐────→│ Vector table  │
                   │IF│──→     │  │     │ address generator │
                   └──┘        └──┘     └───────────────┘
                                │
                                └──────→ Standby release
                                         signal
```

(C) External maskable interrupt

```
    ⟨                       Internal bus                       ⟩
          ⇕               ↑     ↕           ↕           ↑
    ┌──────────────┐    ┌───┐ ┌───┐       ┌───┐
    │ INTM0, KRM00 │    │   │ │MK │       │IE │
    └──────────────┘    │   │ └───┘       └───┘
           ⇓            │   │   │           │
                                                    ┌───────────────┐
Interrupt request →┌──────┐   ┌──┐   ┌──┐      ┌──┐→│ Vector table  │
                   │Edge  │→  │IF│→  │  │──→   │  │  │ address generator │
                   │detection │   └──┘   └──┘      └──┘  └───────────────┘
                   │circuit │                      │
                   └──────┘                        └────→ Standby release
                                                          signal
```

INTM0 : External interrupt mode register 0
KRM00 : Key return mode register 00
IF   : Interrupt request flag
IE   : Interrupt enable flag
MK   : Interrupt mask flag

7. STANDBY FUNCTION

The standby function is a function to reduce current consumption and there are two kinds of standby function as shown below.

- HALT mode :   Stops the operating clock of the CPU. Intermittent operation together with normal operation can reduce average current consumption.
- STOP mode :   Stops oscillation of the system clock. Stops the entire operation by the system clock and minimizes power consumption.

Figure 7-1. Standby Function
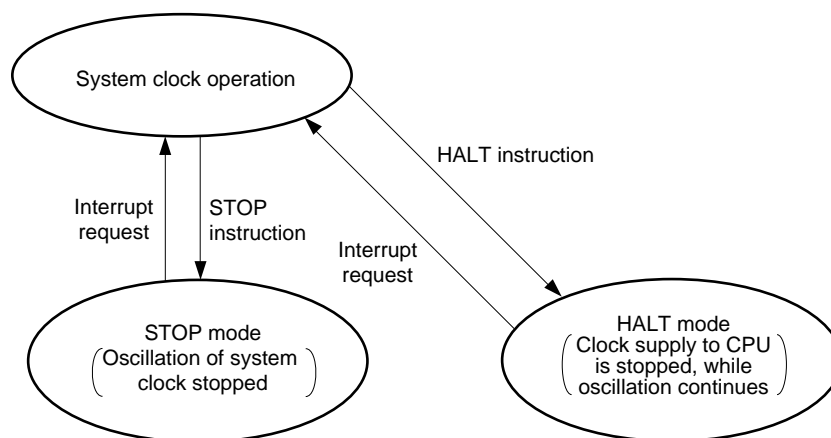
8. RESET FUNCTION

The system is reset in the following two ways.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by detection of inadvertent program loop time of watchdog timer

9. INSTRUCTION SET OVERVIEW

The instruction set for the μPD789800 is listed later.

9.1 Legend

9.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform with the assembly specification). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and a pair of [and] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [and]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or a pair of [and].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed in Table 9-1).

Table 9-1. Operand Formats and Descriptions

Format	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: Immediate data or label FE20H to FF1FH: Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: Immediate data or label (only even address for 16-bit data transfer instructions) 0040H to 007FH: Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

9.1.2 Descriptions of the operation field

A   : A register (8-bit accumulator)
X   : X register
B   : B register
C   : C register
D   : D register
E   : E register
H   : H register
L   : L register
AX   : AX register pair (16-bit accumulator)
BC   : BC register pair
DE   : DE register pair
HL   : HL register pair
PC   : Program counter
SP   : Stack pointer
PSW   : Program status word
CY   : Carry flag
AC   : Auxiliary carry flag
Z   : Zero flag
IE   : Interrupt request enable flag
NMIS   : Flag to indicate that a nonmaskable interrupt is being handled
()   : Contents of a memory location indicated by a parenthesized address or register name
X_H, X_L : Upper and lower 8 bits of a 16-bit register
$\wedge$: Logical product (AND)
$\vee$: Logical sum (OR)
$\veebar$: Exclusive OR
—   : Inverted data
addr16 : 16-bit immediate data or label
jdisp8 : Signed 8-bit data (displacement value)

9.1.3 Description of the flag operation field

(blank) : No change
0   : To be cleared to 0
1   : To be set to 1
×   : To be set or cleared according to the result
R   : To be restored to the previous value

9.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes 1. Except when r = A.

       2. Except when r = A or X.

       3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_CPU), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
XCHW	AX, rp [Note]	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Note Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (fCPU), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	$A \leftarrow A \vee byte$	×		
	saddr, #byte	3	6	$(saddr) \leftarrow (saddr) \vee byte$	×		
	A, r	2	4	$A \leftarrow A \vee r$	×		
	A, saddr	2	4	$A \leftarrow A \vee (saddr)$	×		
	A, !addr16	3	8	$A \leftarrow A \vee (addr16)$	×		
	A, [HL]	1	6	$A \leftarrow A \vee (HL)$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \vee (HL + byte)$	×		
XOR	A, #byte	2	4	$A \leftarrow A \veebar byte$	×		
	saddr, #byte	3	6	$(saddr) \leftarrow (saddr) \veebar byte$	×		
	A, r	2	4	$A \leftarrow A \veebar r$	×		
	A, saddr	2	4	$A \leftarrow A \veebar (saddr)$	×		
	A, !addr16	3	8	$A \leftarrow A \veebar (addr16)$	×		
	A, [HL]	1	6	$A \leftarrow A \veebar (HL)$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \veebar (HL + byte)$	×		
CMP	A, #byte	2	4	$A - byte$	×	×	×
	saddr, #byte	3	6	$(saddr) - byte$	×	×	×
	A, r	2	4	$A - r$	×	×	×
	A, saddr	2	4	$A - (saddr)$	×	×	×
	A, !addr16	3	8	$A - (addr16)$	×	×	×
	A, [HL]	1	6	$A - (HL)$	×	×	×
	A, [HL + byte]	2	6	$A - (HL + byte)$	×	×	×
ADDW	AX, #word	3	6	$AX, CY \leftarrow AX + word$	×	×	×
SUBW	AX, #word	3	6	$AX, CY \leftarrow AX - word$	×	×	×
CMPW	AX, #word	3	6	$AX - word$	×	×	×
INC	r	2	4	$r \leftarrow r + 1$	×	×	
	saddr	2	4	$(saddr) \leftarrow (saddr) + 1$	×	×	
DEC	r	2	4	$r \leftarrow r - 1$	×	×	
	saddr	2	4	$(saddr) \leftarrow (saddr) - 1$	×	×	
INCW	rp	1	4	$rp \leftarrow rp + 1$			
DECW	rp	1	4	$rp \leftarrow rp - 1$			
ROR	A, 1	1	2	$(CY, A_7 \leftarrow A_0, A_{m-1} \leftarrow A_m) \times 1$			×
ROL	A, 1	1	2	$(CY, A_0 \leftarrow A_7, A_{m+1} \leftarrow A_m) \times 1$			×
RORC	A, 1	1	2	$(CY \leftarrow A_0, A_7 \leftarrow CY, A_{m-1} \leftarrow A_m) \times 1$			×
ROLC	A, 1	1	2	$(CY \leftarrow A_7, A_0 \leftarrow CY, A_{m+1} \leftarrow A_m) \times 1$			×

Remark The instruction clock cycle is based on the CPU clock (f$_{CPU}$), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP − 1) ← (PC + 3)$_H$, (SP − 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP − 2			
CALLT	[addr5]	1	8	(SP − 1) ← (PC + 1)$_H$, (SP − 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP − 2			
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2			
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP − 1) ← PSW, SP ← SP − 1			
	rp	1	4	(SP − 1) ← rp$_H$, (SP − 2) ← rp$_L$, SP ← SP − 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp$_H$ ← (SP + 1), rp$_L$ ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X			

Remark The instruction clock cycle is based on the CPU clock (f$_{CPU}$), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1			
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0			
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0			
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1			
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B ← B − 1, then PC ← PC + 2 + jdisp8 if B ≠ 0			
	C, $addr16	2	6	C ← C − 1, then PC ← PC + 2 + jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr) ← (saddr) − 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark The instruction clock cycle is based on the CPU clock (f$_{CPU}$), specified in the processor clock control register (PCC).

10. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)
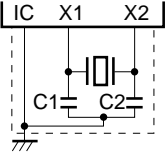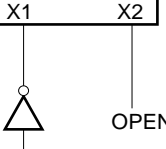
Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V_{DD}			-0.3 to +6.5	V
Input voltage	V_I			-0.3 to V_{DD} + 0.3	V
Output voltage	V_O			-0.3 to V_{DD} + 0.3	V
Output high current	I_{OH}	Each pin		-10	mA
		Total for all pins		-30	mA
Output low current	I_{OL}	Each pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T_A			-40 to +85	°C
Storage temperature	T_{stg}			-65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

Remark The characteristics of a dual-function pin do not differ between the port function and the secondary function, unless otherwise stated.

CHARACTERISTICS OF THE SYSTEM CLOCK OSCILLATION CIRCUIT

(T_A = -40°C to +85°C, V_{DD} = 4.0 to 5.5 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillator frequency (f_X)[Note 1]		6.0	6.0	6.0	MHz
		Oscillation settling time[Note 2]				10	ms
External clock		X1 input frequency (f_X)[Note 1]		6.0	6.0	6.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		71		83	ns

Notes **1.** Only the characteristics of the oscillation circuit are indicated. See the description of the AC characteristics for the instruction execution time.

2. Time required for oscillation to settle once a reset sequence ends or STOP mode is deselected. Use a resonator that can settle oscillation before the oscillation settling time expires.

Caution **When using the system clock oscillation circuit, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.**

- **Keep the wiring as short as possible.**
- **Do not allow signal wires to cross one another.**
- **Keep the wiring away from wires that carry a high, non-stable current.**
- **Keep the grounding point of the capacitors at the same level as V_{SS0}.**
- **Do not connect the grounding point to a grounding wire that carries a high current.**
- **Do not extract a signal from the oscillation circuit.**

★ **Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC CHARACTERISTICS (T$_A$ = -40°C to +85°C, V$_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output high current	I$_{OH}$	Each pin				-1	mA
		Total for all pins				-15	mA
Output low current	I$_{OL}$	Each pin				10	mA
		Total for all pins				80	mA
Input high voltage	V$_{IH1}$	P00-P07, P10-P17		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	$\overline{\text{RESET}}$, P20-P26, P40-P47		0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH3}$	X1		V$_{DD}$ – 0.1		V$_{DD}$	V
	V$_{IH4}$	USBDM, USBDP T$_A$ = 0°C to +70°C		2.0		3.6	V
Input low voltage	V$_{IL1}$	P00-P07, P10-P17		0		0.3V$_{DD}$	V
	V$_{IL2}$	$\overline{\text{RESET}}$, P20, P22, P40-P47		0		0.2V$_{DD}$	V
	V$_{IL3}$	X1		0		0.1	V
	V$_{IL4}$	USBDM, USBDP T$_A$ = 0°C to +70°C		0		0.8	V
Output high voltage	V$_{OH1}$	Pins other than USBDM and USBDP	I$_O$ = -1 mA	V$_{DD}$ – 1.0			V
	V$_{OH2}$	USBDM, USBDP T$_A$ = 0°C to +70°C, RL = 15 kΩ (connected to V$_{SS}$)[Note 1]		2.8			V
Output low voltage	V$_{OL1}$	Pins other than USBDM and USBDP	I$_O$ = 10 mA			1.0	V
	V$_{OL2}$	USBDM, USBDP T$_A$ = 0°C to +70°C, RL = 15 kΩ (connected to V$_{DD}$)[Note 1]				0.3	V
High-level input leakage current	I$_{LIH1}$	Pins other than X1, X2, USBDM, and USBDP	V$_I$ = V$_{DD}$			3	μA
	I$_{LIH2}$	X1, X2	V$_I$ = V$_{DD}$			20	μA
	I$_{LIH3}$	USBDM, USBDP T$_A$ = 0°C to +70°C	0 V ≤ V$_I$ ≤ V$_{REG}$			10	μA
Low-level input leakage current	I$_{LIL1}$	Pins other than X1, X2, USBDM, and USBDP	V$_I$ = 0 V			-3	μA
	I$_{LIL2}$	X1, X2	V$_I$ = 0 V			-20	μA
	I$_{LIL3}$	USBDM, USBDP T$_A$ = 0°C to +70°C	0 V ≤ V$_I$ ≤ V$_{REG}$			-10	μA
High-level output leakage current	I$_{LOH}$	V$_O$ = 0 V				3	μA
Low-level output leakage current	I$_{LOL}$	V$_O$ = 0 V				-3	μA
Software pull-up resistor	R	V$_I$ = 0 V		50	100	200	kΩ
Regulator output voltage	V$_{REG}$	I$_O$ = 0 to -3 mA		3.0	3.3	3.6	V
Supply current[Note 2]	I$_{DD1}$	6.0-MHz crystal oscillation (operating mode)[Note 3]			1.5	3.0	mA
	I$_{DD2}$	6.0-MHz crystal oscillation (HALT mode)[Note 3]			0.5	1.1	mA
	I$_{DD3}$	STOP mode	When the USB function is disabled		10	30	μA
			When the USB function is enabled (T$_A$ = 0°C to +70°C)		50	100	μA

★ (marker next to Output low voltage row)

Notes 1. RL is a resistor connected to a bus line.

2. The power supply current does not include the current flowing through the on-chip pull-up resistor.

3. During high-speed mode operation (when the processor clock control register (PCC) is cleared to 00H)

Remark The characteristics of a dual-function pin do not differ between the port function and the secondary function, unless otherwise stated.

AC CHARACTERISTICS

(1) Basic operations (T_A = -40°C to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	When PCC = 00H (f_X = 6.0 MHz)	0.333	0.333	0.333	μs
		When PCC = 02H (f_X = 6.0 MHz)	1.333	1.333	1.333	μs
TI01 input frequency	f_{TI}		0		4.0	MHz
TI01 input high/low level width	t_{TIH}, t_{TIL}		0.1			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INTP0	10			μs
$\overline{RESET}$ input low level width	t_{RSL}		10			μs

(2) Serial interface

(a) USB function (T_A = 0°C to +70°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USBDM and USBDP rise time	t_R	CL = 50 pF[Note]	75			ns
		CL = 350 pF[Note]			300	ns
USBDM and USBDP fall time	t_F	CL = 50 pF[Note]	75			ns
		CL = 350 pF[Note]			300	ns
t_R and t_F matching	t_{RFM}	t_R/t_F	80		120	%
Differential output signal cross-over point	V_{CRS}		1.3		2.0	V
Data transfer rate	t_{DRATE}	When the microcontroller operates at the system clock (f_X) of 6.0 MHz	1.5	1.5	1.5	Mbps
Transmission differential signal jitter	t_{UDJ1}	Upon transferring the next bit	-95	0	95	ns
	t_{UDJ2}	Upon transferring the bit following the next bit	-150	0	150	ns
Transmission EOP width	t_{EOPT1}		1.25	1.33	1.50	μs
Reception EOP width	t_{EOPR1}	EOP width to be eliminated			300	μs
	t_{EOPR2}	EOP width to be detected	675			μs
Reception USB reset width	t_{URES1}	USB reset width to be eliminated			2.5	μs
	t_{URES2}	USB reset width to be detected	5.5			μs

Note CL is the capacitance of the USBDM and USBDP output lines.

(b) Three-wire serial I/O mode (T$_A$ = -40°C to +85°C, V$_{DD}$ = 4.0 to 5.5 V)

(i) $\overline{SCK10}$ ...Internal clock output (when f$_X$ = 6.0 MHz)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t$_{KCY1}$	When TPS100[Note 1] = 0		667	667	667	ns
		When TPS100[Note 1] = 1		1,333	1,333	1,333	ns
$\overline{SCK10}$ high/low level width	t$_{KH1}$, t$_{KL1}$	When TPS100[Note 1] = 0		283	333		ns
		When TPS100[Note 1] = 1		617	667		ns
SI10 setup time	t$_{SIK1}$	Relative to $\overline{SCK10}$ ↑		150			ns
SI10 hold time	t$_{KSI1}$	Relative to $\overline{SCK10}$ ↑	When TPS100[Note 1] = 0	333			ns
			When TPS100[Note 1] = 1	667			ns
SO10 output dalay	t$_{KSO1}$	Relative to $\overline{SCK10}$ ↓, CL = 100 pF[Note 2]		0		200	ns

Notes 1. Bit 4 of serial operation mode register 10 (CSIM10)
   2. CL is the capacitance of the SO output line.

(ii) $\overline{SCK10}$ ...External clock output

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t$_{KCY2}$		667			ns
$\overline{SCK10}$ high/low level width	t$_{KH2}$, t$_{KL2}$		283			ns
SI10 setup time	t$_{SIK2}$		100			ns
SI10 hold time	t$_{KSI2}$		333			ns
SO10 output delay	t$_{KSO2}$	Relative to $\overline{SCK10}$ ↓, CL = 100 pF[Note]	0		250	ns

Note CL is the capacitance of the SO output line.

AC TIMING MEASUREMENT POINTS (except the X1 input and USB function)

$0.8V_{DD}$ ⟶ Measurement points ⟵ $0.8V_{DD}$
$0.2V_{DD}$ ⟶ ⟵ $0.2V_{DD}$

CLOCK TIMING

$1/f_X$

t_{XL} t_{XH}

X1 input

V_{IH3} (MIN.)
V_{IL3} (MAX.)

TI TIMING

$1/f_{TI}$

t_{TIL} t_{TIH}

TI01
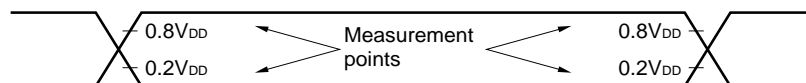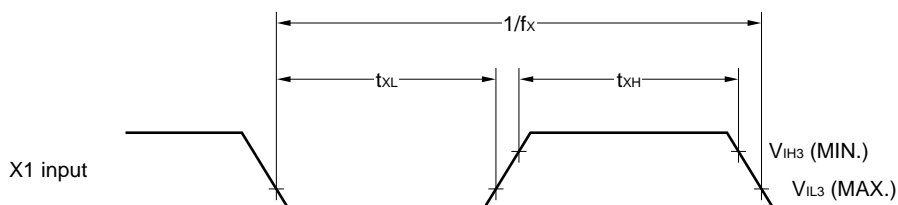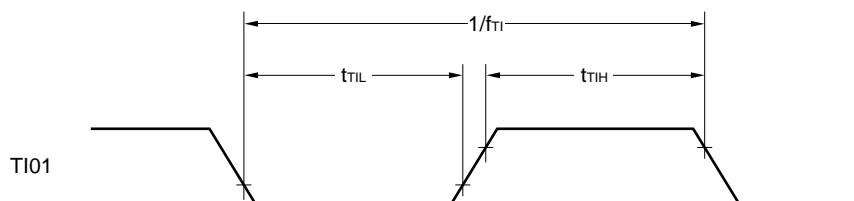
INTERRUPT INPUT TIMING

t_{INTL} t_{INTH}

INTP0
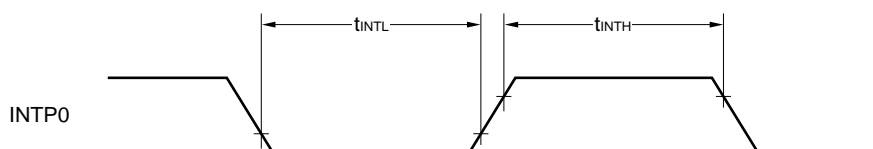
RESET INPUT TIMING

t_{RSL}
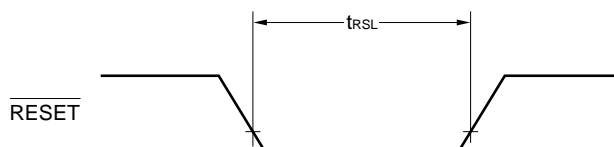
$\overline{RESET}$

SERIAL TRANSFER TIMING

USB Function:

USBDM and USBDP rise/fall time

USBDM, USBDP

0.9V_DD

0.1V_DD

t_R t_F
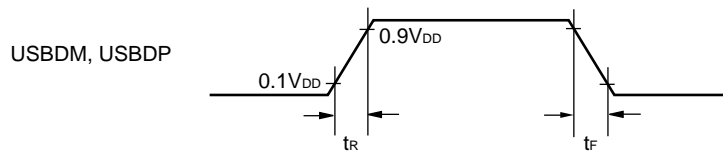
Transmission different signal jitter

1,333 ns

667 ns

USBDM, USBDP   Next bit   Bit following the next bit

t_{UDJ1} t_{UDJ2}
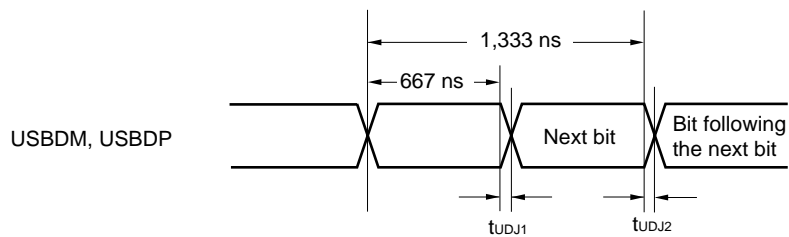
Differential output signal cross-over point, transmission EOP width, reception EOP width, and reception USB reset width

USBDM, USBDP   V_CRS

t_{EOPT1}, t_{EOPRm}, t_{URESm}

m = 1, 2

Three-Wire Serial I/O Mode:

t_{KCYm}

t_{KLm} t_{KHm}

$\overline{SCK10}$ 0.8V_DD   0.2V_DD

t_{SIKm} t_{KSIm}

SI10   Input data

t_{KSOm}

SO10   Output data
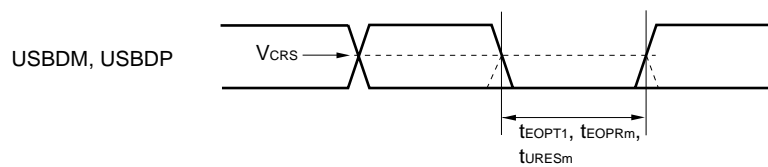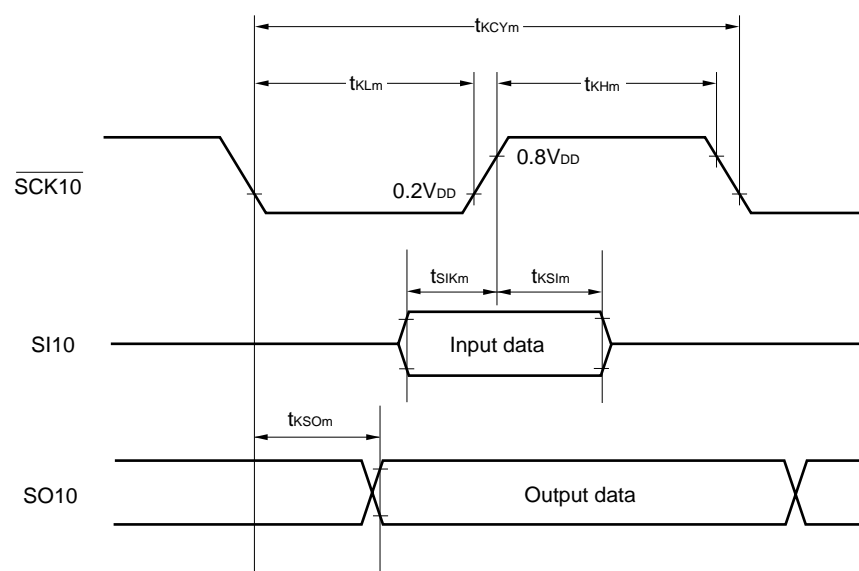
m = 1, 2

DATA HOLD CHARACTERISTICS OF DATA MEMORY AT LOW VOLTAGE IN STOP MODE
(T_A = -40°C to +85°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold supply voltage	V_{DDDR}		4.0		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation settling time[Note 1]	t_{WAIT}	Reset by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Reset by interrupt request		**Note 2**		ms

> **Notes 1.** During the oscillation settling time, CPU operations are disabled to prevent them from becoming unstable upon the start of oscillation.
>
> **2.** $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected according to the setting of bits 0 to 2 (OSTS0 to OSTS2) of the oscillation settling time selection register.

> **Remark** f_X: System clock oscillation frequency

DATA HOLD TIMING (STOP mode release by $\overline{\text{RESET}}$)
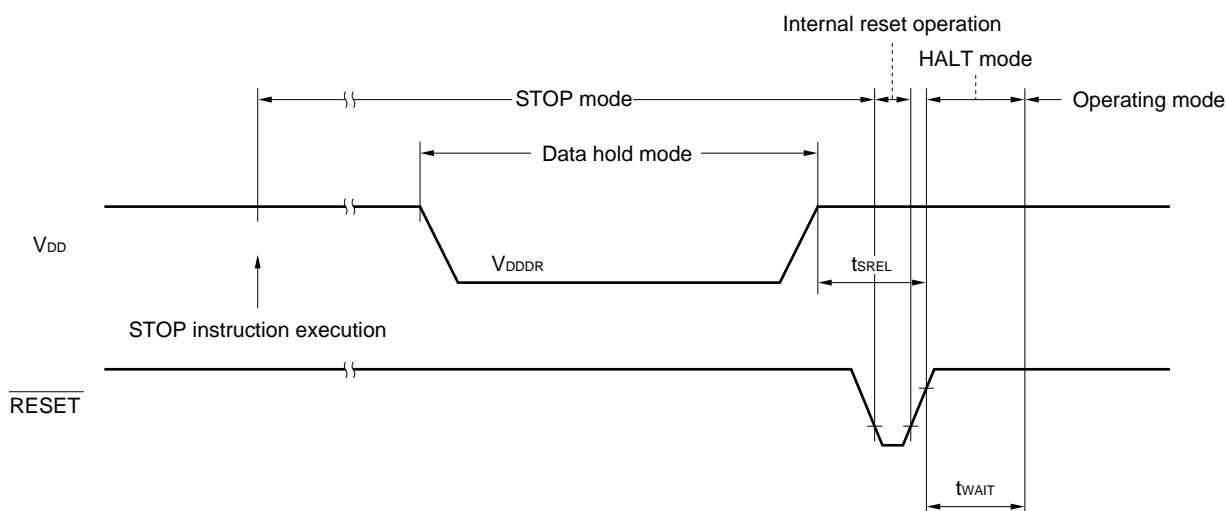
DATA HOLD TIMING (standby release signal: STOP mode release by interrupt signal)
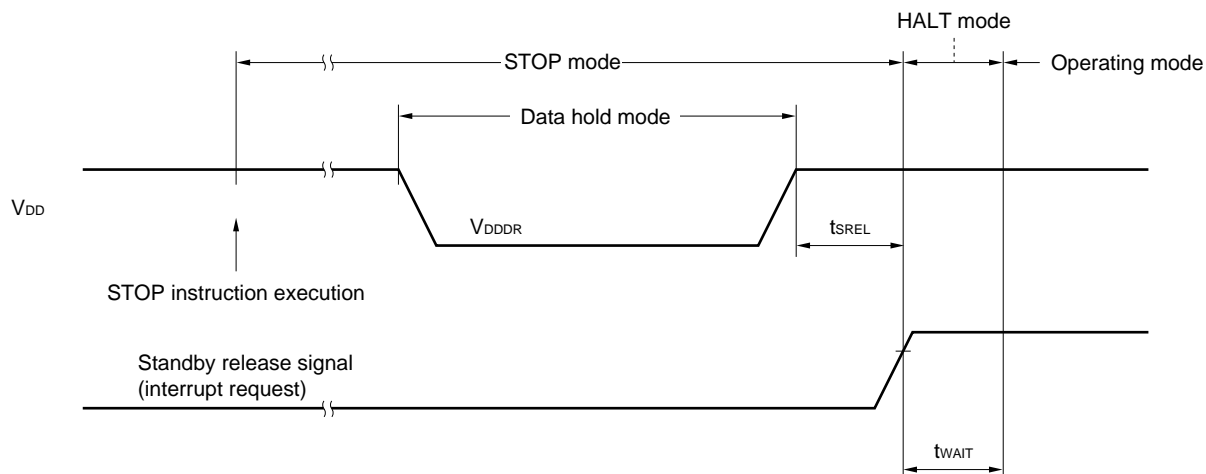
11. PACKAGE DRAWINGS

44-PIN PLASTIC QFP (10x10)
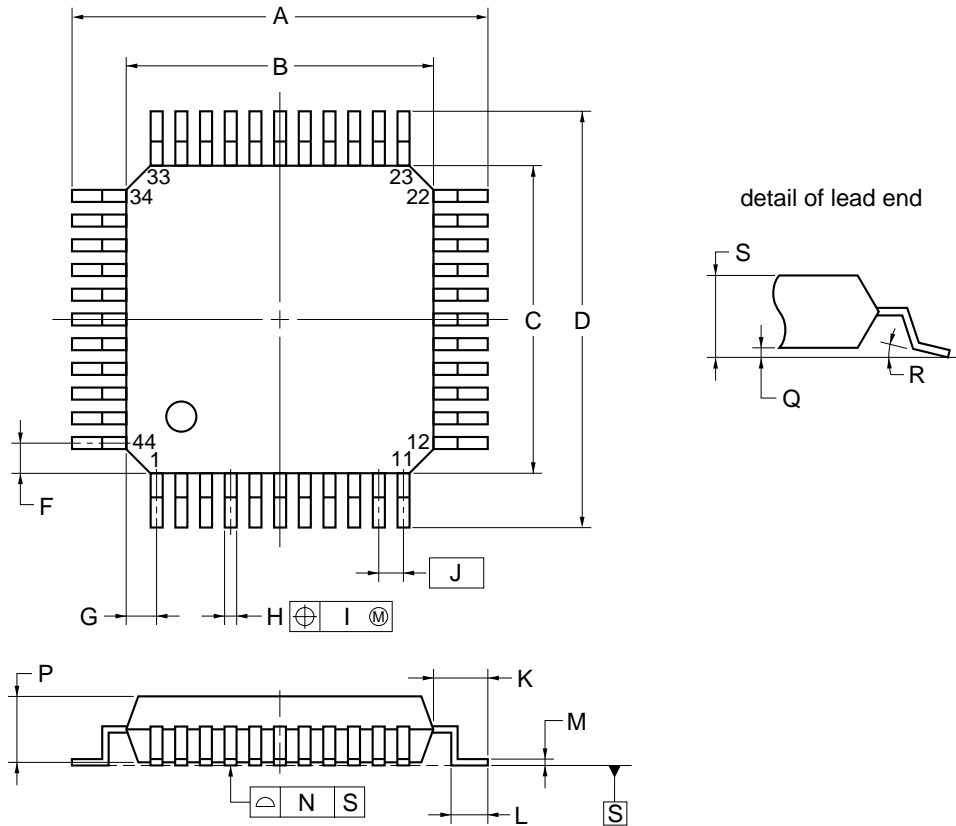
detail of lead end

NOTE

Each lead centerline is located within 0.16 mm of
its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	13.2±0.2
B	10.0±0.2
C	10.0±0.2
D	13.2±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.16
J	0.8 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.17^{+0.06}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.125±0.075
R	$3°^{+7°}_{-3°}$
S	3.0 MAX.

S44GB-80-3BS-2

44 PIN PLASTIC LQFP (10 x 10)
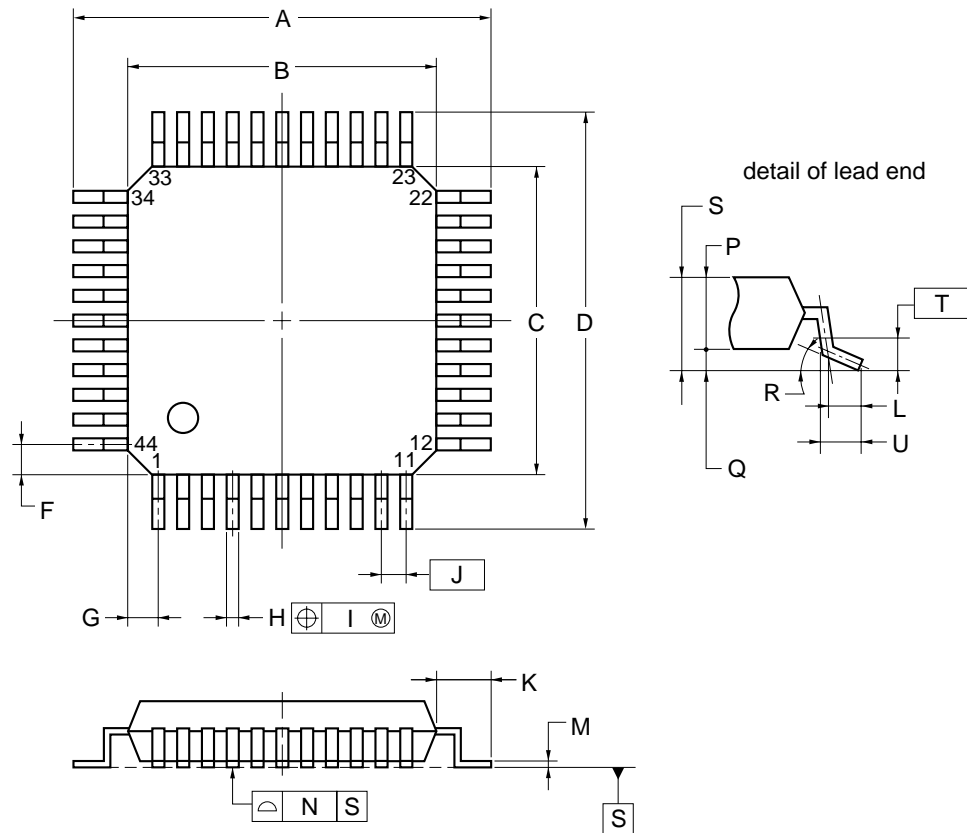
detail of lead end

NOTE

Each lead centerline is located within 0.16 mm of
its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3°^{+4°}_{-3°}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

12. RECOMMENDED SOLDERING CONDITIONS

The µPD789800 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual** (C10535E).

For soldering methods and conditions other than those recommended below, contact our sales representatives.

Table 12-1. Surface Mounting Type Soldering Conditions

µPD789800GB-×××-3BS-MTX: 44-pin plastic QFP (10 × 10)

Soldering method	Soldering conditions	Symbol
Infrared reflow	Package peak temperature: 235°C Duration: 30 sec. max. (at 210°C or above) Maximum allowable number of reflow processes: 3	IR35-00-3
VPS	Package peak temperature: 215°C Duration: 40 sec. max. (at 200°C or above) Maximum allowable number of reflow processes: 3	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120°C max. (Package surface temperature)	WS60-00-1
Partial heating method	Terminal temperature: 300°C max. Duration: 3 sec. max. (per device side)	-

Caution   Use of more than one soldering method should be avoided (except for partial heating method).

µPD789800GB-×××-8ES: 44-pin plastic LQFP (10 × 10)

Soldering method	Soldering conditions	Symbol
Infrared reflow	Package peak temperature: 235°C Duration: 30 sec. max. (at 210°C or above) Maximum allowable number of reflow processes: 2	IR35-00-2
VPS	Package peak temperature: 215°C Duration: 40 sec. max. (at 200°C or above) Maximum allowable number of reflow processes: 2	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120°C max. (Package surface temperature)	WS60-00-1
Partial heating method	Terminal temperature: 300°C max. Duration: 3 sec. max. (per device side)	-

Caution   Use of more than one soldering method should be avoided (except for partial heating method).

APPENDIX A   DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD789800.

LANGUAGE PROCESSING SOFTWARE

RA78K0S[Notes 1, 2, 3]	Assembler package common to the 78K/0S series
CC78K0S[Notes 1, 2, 3]	C compiler package common to the 78K/0S series
DF789801[Notes 1, 2, 3]	Device file for the μPD789800 sub-series
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to the 78K/0S series

FLASH MEMORY WRITE TOOLS

Flashpro III	Dedicated flash writer
FA-44GB[Note 4]	Flash memory write adapter (GB-3BS type)
FA-44GB-8ES[Note 4]	Flash memory write adapter (GB-8ES type)

DEBUGGING TOOLS (1/2)

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging hardware and software of application system using 78K/0S Series. Supports integrated debugger (ID78K0S-NS). Used in combination with AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-70000-MC-PS-B AC adapter	This is the adapter for supplying power from outlet of 100 to 240 VAC.
IE-70000-98-IF-C Interface adapter	This adapter is needed when PC-9800 series (excluding notebook models) is used as a host machine of IE-78K0S-NS. (Compatible with C bus)
IE-70000-CD-IF-A PC card interface	This PC card and interface cable are needed when a notebook-type personal computer is used as a host machine of IE-78K0S-NS. (Compatible with a PCMCIA socket)
IE-70000-PC-IF-C Interface adapter	This adapter is needed when IBM PC/AT™ and compatibles are used as a host machine of IE-78K0S-NS. (Compatible with ISA bus)
IE-70000-PCI-IF Interface adapter	This adapter is needed when a personal computer with a built-in PCI bus is used as a host machine of IE-78K0S-NS.
IE-789801-NS-EM1 Emulation board	Emulation board for emulating the peripheral hardware inherent to the device. Used in combination with in-circuit emulator.

Notes 1. Based on the PC-9800 series (Japanese Windows™)

   2. Based on the IBM PC/AT and compatibles (Japanese/English Windows)

   3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), and NEWS™ (NEWS-OS™)

   4. Product manufactured by Naito Densei Machida Mfg. Co., Ltd. (044-822-3813)

Remark   The RA78K0S and CC78K0S can be used in combination with the DF789801.

DEBUGGING TOOLS (2/2)

NP-44GB[Notes 1, 2] Emulation prove		This probe is used to connect the in-circuit emulator to the target system and is designed for 44-pin plastic QFP. It should be used in combination with EV-9200G-44.
	EV-9200G-44 Conversion socket	This conversion socket connects the NP-44GB to the target system board designed to mount a 44-pin plastic QFP (GB-3BS, GB-8ES type).
NP-44GB-TQ[Notes 1, 2] Emulation prove		This probe is used to connect the in-circuit emulator to the target system and is designed for 44-pin plastic QFP. It should be used in combination with TGB-044SAP.
	TGB-044SAP[Note 3] Conversion socket	This conversion socket connects the NP-44GB-TQ to the target system board designed to mount a 44-pin plastic QFP (GB-3BS, GB-8ES type).
SM78K0S[Notes 4, 5]		System simulator common to the 78K/0S series
ID78K0S-NS[Notes 4, 5]		Integrated debugger common to the 78K/0S series
DF789801[Notes 4, 5]		Device file for the μPD789800 sub-series

REAL-TIME OS

MX78K0S[Notes 4, 5]	OS for the 78K/0S series

Notes 1. Product manufactured by Naito Densei Machida Mfg. Co., Ltd. (044-822-3813)

    2. Either probe and socket combination can be selected for use.

    3. Product manufactured by TOKYO ELETEC Corporation

       For further information, consult:

       Tokyo Electronic Div. (TEL (03) 3820-7112), or

       Osaka Electronic Div. (TEL (06) 6244-6672)

       Daimaru Kogyo Corporation.

    4. Based on the PC-9800 series (Japanese Windows)

    5. Based on the IBM PC/AT and compatibles (Japanese/English Windows)

Remark The SM78K0S can be used in combination with the DF789801.

APPENDIX B   RELATED DOCUMENTS

DOCUMENTS RELATED TO DEVICES

Document name	Document No.	
	Japanese	English
μPD789800 Data Sheet	U12627J	This manual
★ μPD78F9801 Data Sheet	U12626J	U12626E
μPD789800 Sub-Series User's Manual	U12978J	U12978E
78K/0S Series User's Manual, Instruction	U11047J	U11047E

DOCUMENTS RELATED TO DEVELOPMENT TOOLS (USER'S MANUAL)

Document name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator for IBM PC/AT (Windows)	Reference	U11489J	U11489E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K0S-NS Integrated Debugger Windows-Based	Reference	U12901J	U12901E
IE-78K0S-NS In-circuit Emulator		U13549J	U13549E
IE-789801-NS-EM1 Emulation Board		U13390J	U13390E

DOCUMENTS RELATED TO SOFTWARE TO BE INCORPORATED INTO THE PRODUCT (USER'S MANUAL)

Document name		Document No.	
		Japanese	English
OS for 78K/0S Series MX78K0S	Basic	U12938J	U12938E

OTHER DOCUMENTS

Document name	Document No.	
	Japanese	English
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality Control/Reliability Handbook	C12769J	-
Guide for Products Related to Micro-Computer: Other Companies	U11416J	-

Caution   The above documents may be revised without notice. Use the latest versions when you design application systems.

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┌─────────────────────── NOTES FOR CMOS DEVICES ───────────────────────┐
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① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability

- Ordering information

- Product release schedule

- Availability of related technical literature

- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
      800-366-9782
Fax: 408-588-6130
      800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Madrid Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP Brasil
Tel: 55-11-6462-6810
Fax: 55-11-6462-6829

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[MEMO]

Some related documents may be preliminary versions. Note, however, that whether a related document is preliminary is not indicated in this document.

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