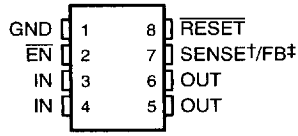
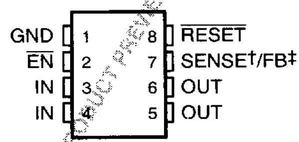
- **Available in 3.3-V, 4.85-V, and 5-V Fixed-Output and Adjustable Versions**
- **Integrated Precision Supply-Voltage Supervisor Monitoring Regulator Output Voltage**
- **Active-Low Reset Signal with 200-ms Pulse Width**
- **Very Low Dropout Voltage . . . Maximum of 35 mV at I_O = 100 mA (TPS7350)**
- **Low Quiescent Current – Independent of Load . . . 340 μA Typ**
- **Extremely Low Sleep-State Current, 0.5 μA Max**
- **2% Tolerance Over Full Range of Load, Line, and Temperature for Fixed-Output Versions**
- **Output Current Range of 0 mA to 250 mA**
- **TSSOP Package Option Offers Reduced Component Height For Critical Applications**

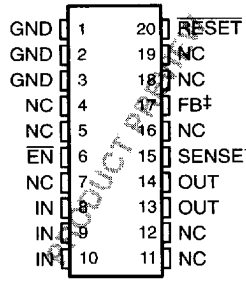
D PACKAGE (TOP VIEW)



P PACKAGE (TOP VIEW)



PW PACKAGE (TOP VIEW)



NC – No internal connection
† SENSE – Fixed voltage options only (TPS7333, TPS7348, and TPS7350)
‡ FB – Adjustable version only (TPS7301)

description

The TPS73xx devices are members of a family of micropower low-dropout (LDO) voltage regulators. They are differentiated from the TPS71xx and TPS72xx LDOs by their integrated delayed microprocessor-reset function. If the precision delayed reset is not required, the designer should consider the TPS71xx and TPS72xx.†

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)			NEGATIVE-GOING RESET THRESHOLD VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	MIN	TYP	MAX	SMALL OUT-LINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
−40°C to 125°C	4.9	5	5.1	4.55	4.65	4.75	TPS7350QD	TPS7350QP	TPS7350QPWLE	TPS7350Y
	4.75	4.85	4.95	4.5	4.6	4.7	TPS7348QD	TPS7348QP	TPS7348QPWLE	TPS7348Y
	3.23	3.3	3.37	2.868	2.934	3	TPS7333QD	TPS7333QP	TPS7333QPWLE	TPS7333Y
	Adjustable 1.2 V to 9.75 V			1.101	1.123	1.145	TPS7301QD	TPS7301QP	TPS7301QPWLE	TPS7301Y

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7350QDR). The PW package is only available left-end taped and reeled. The TPS7301Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.

† The TPS71xx and the TPS72xx are 500-mA and 250-mA output regulators respectively, offering performance similar to that of the TPS73xx but without the delayed-reset function. The TPS72xx devices are further differentiated by availability in 8-pin thin shrink small-outline packages (TSSOP) for applications requiring minimum package size.

description (continued)

The RESET output of the TPS73xx is designed to initiate a reset in microcomputer and micro-processor systems in the event of an undervoltage condition. An internal comparator in the TPS73xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

If that occurs, the RESET output (open-drain NMOS) turns on, taking the RESET signal low. RESET stays low for the duration of the undervoltage condition. Once the undervoltage condition ceases, a 200-ms (typ) time-out begins. At the completion of the 200-ms delay, RESET goes high.

An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 35 mV at an output current of 100 mA for the TPS7350) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is low and remains constant, independent of output loading (typically 340 μA over the full range of output current, 0 mA to 250 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The LDO family also features a sleep mode; applying a logic high signal to EN (enable) shuts down the regulator, reducing the quiescent current to 0.5 μA maximum at T_J = 25°C.

The TPS73xx is offered in 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version). The TPS73xx family is available in PDIP (8 pin), SO (8 pin) and TSSOP (20 pin) packages. The TSSOP has a maximum height of 1.2 mm.

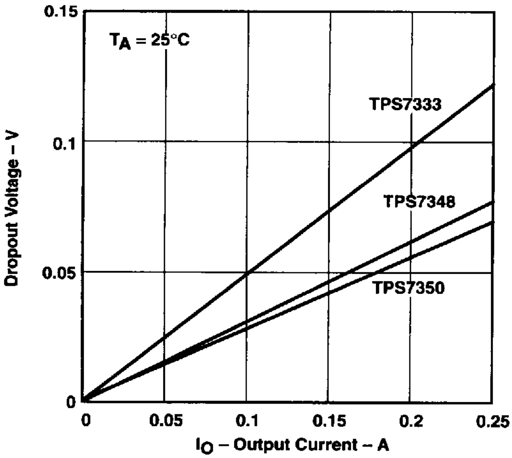
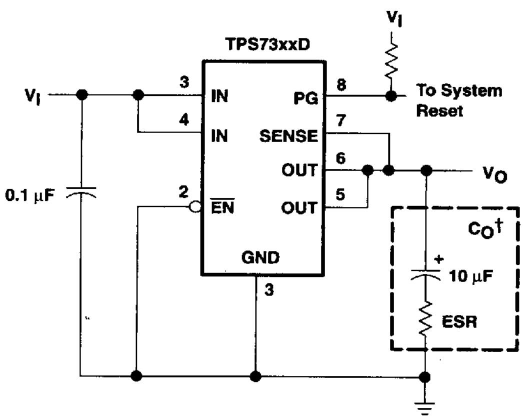


Figure 1. Dropout Voltage Versus Output Current



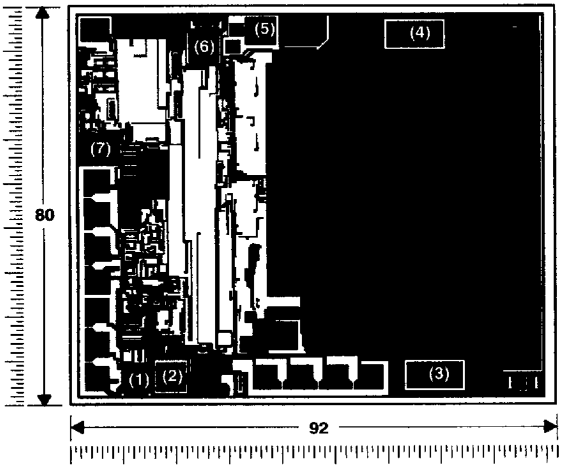
† Capacitor selection is nontrivial. See application information section for details.

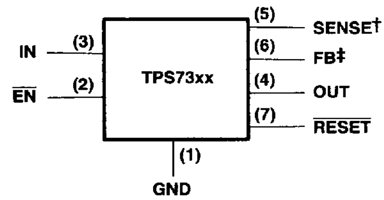
Figure 2. Typical Application Configuration

TPS73xxY chip information

These chips, when properly assembled, display characteristics similar to the TPS73xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

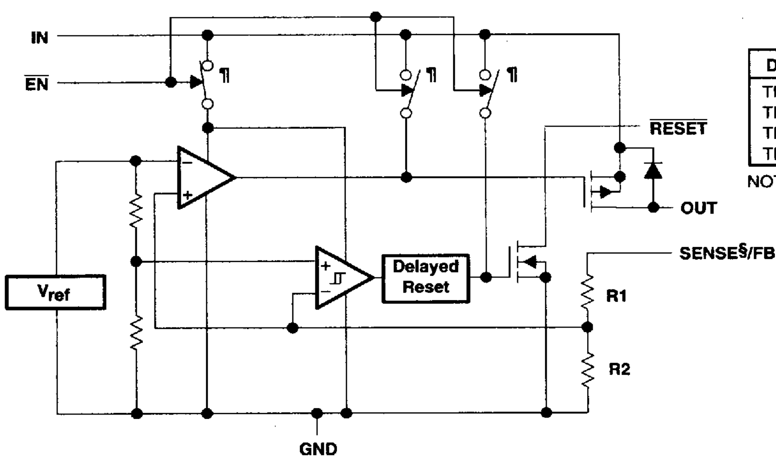
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

† SENSE – Fixed voltage options only (TPS7333, TPS7348, and TPS7350)
‡ FB – Adjustable version only (TPS7301)

NOTE A. For most applications, OUT and SENSE should be tied together as close as possible to the device; for other implementations, refer to SENSE-pin connection discussion in the applications information section of this data sheet.

functional block diagram



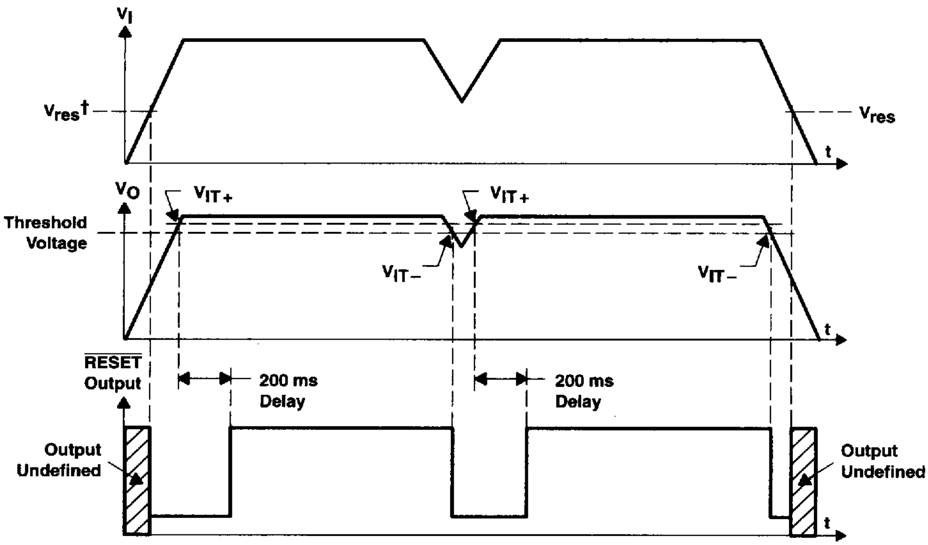
RESISTOR DIVIDER OPTIONS

DEVICE	R1	R2	UNIT
TPS7301	0	∞	Ω
TPS7333	420	233	kΩ
TPS7348	726	233	kΩ
TPS7350	756	233	kΩ

NOTE A. Resistors are nominal values only.

§ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in applications information section.
¶ Switch positions are shown with EN low (active).

timing diagram



† V_{res} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Input voltage range§, V_I, $\overline{\text{RESET}}$, SENSE, $\overline{\text{EN}}$ .... −0.3 to 10 V
Output current, I_O .... 2 A
Continuous total power dissipation .... See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, T_J .... −55°C to 150°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
§ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P†	1175 mW	9.4 mW/°C	752 mW	235 mW
PW†‡	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Figure 4)

PACKAGE	$T_C \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 70°C$ POWER RATING	$T_C = 125°C$ POWER RATING
D	2188 mW	9.4 mW/°C	1765 mW	1248 mW
P†	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW†‡	4025 mW	32.2 mW/°C	2576 mW	805 mW

† The P and PW packages are product preview only and are not yet available.
‡ Refer to thermal information section for detailed power dissipation considerations when using the TSSOP package.

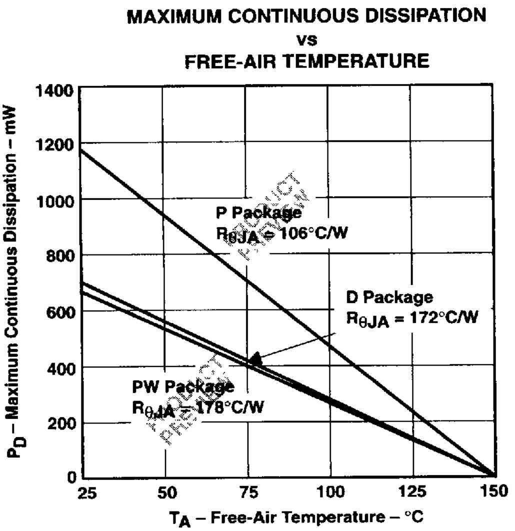


Figure 3

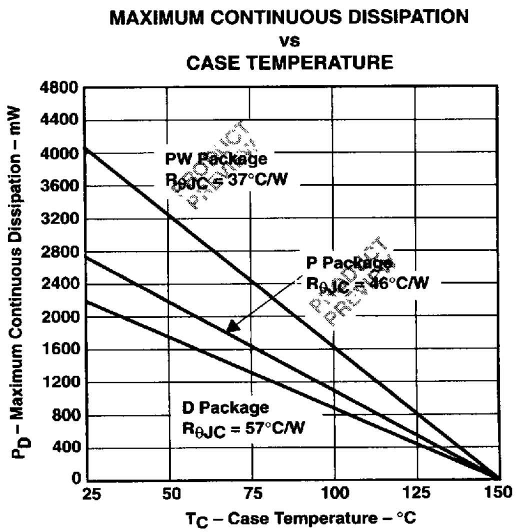


Figure 4

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	TPS7301Q	2.5	10	V
	TPS7333Q	3.77	10	
	TPS7348Q	5.2	10	
	TPS7350Q	5.33	10	
High-level input voltage at $\overline{EN}$, V_{IH}		2		V
Low-level input voltage at $\overline{EN}$, V_{IL}			0.5	V
Output current range, I_O		0	250	mA
Operating virtual junction temperature range, T_J		−40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage, V_{DO}, at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because the TPS7301 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the electrical characteristics table. The minimum value of 2.5 V is the absolute lower limit for the recommended input voltage range for the TPS7301.

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 µF(CSR‡ = 1 Ω), SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS§	T_J	TPS7301Q, TPS7333Q TPS7348Q, TPS7350Q MIN	TYP	MAX	UNIT
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 250 mA	25°C		340	400	µA
		−40°C to 125°C			550	
Input current (standby mode)	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C		0.01	0.5	µA
		−40°C to 125°C			2	
Output current limit	V_O = 0 V, V_I = 10 V	25°C		1.2	2	A
		−40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V	25°C		0.01	0.5	µA
		−40°C to 125°C			1	
$\overline{RESET}$ leakage current	Normal operation, V at $\overline{RESET}$ = 10 V	25°C		0.02	0.5	µA
		−40°C to 125°C			0.5	
Output voltage temperature coefficient		−40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ logic high (standby mode)	2.5 V ≤ V_I ≤ 6 V	−40°C to 125°C	2			V
	6 V ≤ V_I ≤ 10 V		2.7			
$\overline{EN}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V	25°C			0.5	V
		−40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage		25°C		50		mV
$\overline{EN}$ input current	0 V ≤ V_I ≤ 10 V	25°C	−0.5	0.001	0.5	µA
		−40°C to 125°C	−0.5		0.5	
Minimum V_I for active pass element		25°C		2.05	2.5	V
		−40°C to 125°C			2.5	
Minimum V_I for valid $\overline{RESET}$	$I_{O(RESET)}$ = −300 µA	25°C		1	1.5	V
		−40°C to 125°C			1.9	

‡ CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
§ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7301Q electrical characteristics at I_O = 10 mA, V_I = 3.5 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF(CSR† = 1 Ω), FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7301Q MIN	TPS7301Q TYP	TPS7301Q MAX	UNIT
Reference voltage (measured at FB)	V_I = 3.5 V,	I_O = 10 mA	25°C		1.182		V
	2.5 V ≤ V_I ≤ 10 V, See Note 1	5 mA ≤ I_O ≤ 250 mA,	–40°C to 125°C	1.147		1.217	V
Reference voltage temperature coefficient			–40°C to 125°C		61	75	ppm/°C
Pass-element series resistance (see Note 2)	V_I = 2.4 V,	50 μA ≤ I_O ≤ 150 mA	25°C		0.7	1	Ω
			–40°C to 125°C			1	
	V_I = 2.4 V,	150 mA ≤ I_O ≤ 250 mA	25°C		0.83	1.3	
			–40°C to 125°C			1.3	
	V_I = 2.9 V,	50 μA ≤ I_O ≤ 250 mA	25°C		0.52	0.85	
			–40°C to 125°C			0.85	
	V_I = 3.9 V,	50 μA ≤ I_O ≤ 250 mA	25°C		0.32		
	V_I = 5.9 V,	50 μA ≤ I_O ≤ 250 mA	25°C		0.23		
Input regulation	V_I = 2.5 V to 10 V, See Note 1	50 μA ≤ I_O ≤ 250 mA,	25°C		3	18	mV
			–40°C to 125°C			25	
Output regulation	2.5 V ≤ V_I ≤ 10 V, See Note 1	I_O = 5 mA to 250 mA,	25°C		5	14	mV
			–40°C to 125°C			25	
	2.5 V ≤ V_I ≤ 10 V, See Note 1	I_O = 50 μA to 250 mA,	25°C		7	22	mV
			–40°C to 125°C			54	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	48	59		dB
			–40°C to 125°C	44			
		I_O = 250 mA, See Note 1	25°C	45	54		
			–40°C to 125°C	44			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		95		μVrms
		C_O = 10 μF	25°C		89		
		C_O = 100 μF	25°C		74		
$\overline{RESET}$ trip-threshold voltage§	$V_{O(FB)}$ decreasing		–40°C to 125°C	1.101		1.145	V
$\overline{RESET}$ hysteresis voltage§	Measured at $V_{O(FB)}$		25°C		12		mV
$\overline{RESET}$ output low voltage§	V_I = 2.13 V,	$I_{O(RESET)}$ = 400 μA	25°C		0.1	0.4	V
			–40°C to 125°C			0.4	
FB input current			25°C	–10	0.1	10	nA
			–40°C to 125°C	–20		20	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.
§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When V_I < 2.9 V and I_O > 150 mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 32) to a point where the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.
2. To calculate dropout voltage, use equation: $V_{DO} = I_O \cdot r_{DS(on)}$
$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for V_I = 2.4 V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V respectively. For other programmed values, refer to Figure 32.

TPS7333Q electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF(CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7333Q MIN	TPS7333Q TYP	TPS7333Q MAX	UNIT
Output voltage	V_I = 4.3 V,	I_O = 10 mA	25°C		3.3		V
	4.3 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	−40°C to 125°C	3.23		3.37	
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		4.5	7	mV
			−40°C to 125°C			8	
	I_O = 100 mA,	V_I = 3.23 V	25°C		44	60	
			−40°C to 125°C			80	
	I_O = 250 mA,	V_I = 3.23 V	25°C		108	150	
			−40°C to 125°C			200	
Pass-element series resistance	(3.23 V − V_O)/I_O, I_O = 250 mA	V_I = 3.23 V,	25°C		0.44	0.6	Ω
			−40°C to 125°C			0.8	
Input regulation	V_I = 4.3 V to 10 V,	50 μA ≤ I_O ≤ 250 mA	25°C		6	23	mV
			−40°C to 125°C			29	
Output regulation	I_O = 5 mA to 250 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		21	32	mV
			−40°C to 125°C			60	
	I_O = 50 μA to 250 mA,	4.3 V ≤ V_I ≤ 10 V	25°C		31	60	mV
			−40°C to 125°C			120	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	46	51		dB
			−40°C to 125°C	44			
		I_O = 250 mA	25°C	39	49		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		274		μVrms
		C_O = 10 μF	25°C		228		
		C_O = 100 μF	25°C		159		
$\overline{RESET}$ trip-threshold voltage	V_O decreasing		−40°C to 125°C	2.868			V
$\overline{RESET}$ trip-threshold voltage	V_O increasing		−40°C to 125°C				V
$\overline{RESET}$ hysteresis voltage			25°C		18		mV
$\overline{RESET}$ output low voltage	V_I = 2.8 V,	$I_{O(RESET)}$ = −1 mA	25°C		0.17	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7348Q electrical characteristics at I_O = 10 mA, V_I = 5.85 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF(CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7348Q MIN	TYP	MAX	UNIT
Output voltage	V_I = 5.85 V,	I_O = 10 mA	25°C		4.85		V
	5.85 V ≤ V_I ≤ 10 V,	5 mA ≤ I_O ≤ 250 mA	–40°C to 125°C	4.75		4.95	
Dropout voltage	I_O = 10 mA,	V_I = 4.75 V	25°C		2.9	6	mV
			–40°C to 125°C			8	
	I_O = 100 mA,	V_I = 4.75 V	25°C		28	37	
			–40°C to 125°C			52	
	I_O = 250 mA,	V_I = 4.75 V	25°C		70	91	
			–40°C to 125°C			130	
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 250 mA	V_I = 4.75 V,	25°C		0.28	0.37	Ω
			–40°C to 125°C			0.52	
Input regulation	V_I = 5.85 V to 10 V,	50 μA ≤ I_O ≤ 250 mA	25°C		9	35	mV
			–40°C to 125°C			37	
Output regulation	I_O = 5 mA to 250 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		28	40	mV
			–40°C to 125°C			75	
	I_O = 50 μA to 250 mA,	5.85 V ≤ V_I ≤ 10 V	25°C		42	65	mV
			–40°C to 125°C			130	
Ripple rejection	f = 120 Hz	I_O = 50 μA	25°C	45	53		dB
			–40°C to 125°C	39			
		I_O = 250 mA	25°C	39	50		
			–40°C to 125°C	35			
Output noise-spectral density	f = 120 Hz		25°C		2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF	25°C		410		μVrms
		C_O = 10 μF	25°C		328		
		C_O = 100 μF	25°C		212		
$\overline{RESET}$ trip-threshold voltage	V_O decreasing		–40°C to 125°C	4.5		4.7	V
$\overline{RESET}$ trip-threshold voltage	V_O increasing		–40°C to 125°C				V
$\overline{RESET}$ hysteresis voltage			25°C		26		mV
$\overline{RESET}$ output low voltage	$I_{O(RESET)}$ = –1.2 mA, V_I = 4.12 V		25°C		0.2	0.4	V
			–40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7350Q electrical characteristics at $I_O = 10$ mA, $V_I = 6$ V, $\overline{EN} = 0$ V, $C_O = 4.7$ µF(CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		T_J	TPS7350Q MIN	TPS7350Q TYP	TPS7350Q MAX	UNIT
Output voltage	$V_I = 6$ V,	$I_O = 10$ mA	25°C		5		V
	$6\text{ V} \le V_I \le 10$ V,	$5\text{ mA} \le I_O \le 250$ mA	−40°C to 125°C	4.9		5.1	
Dropout voltage	$I_O = 10$ mA,	$V_I = 4.88$ V	25°C		2.9	6	mV
			−40°C to 125°C			8	
	$I_O = 100$ mA,	$V_I = 4.88$ V	25°C		27	35	
			−40°C to 125°C			50	
	$I_O = 250$ mA,	$V_I = 4.88$ V	25°C		68	88	
			−40°C to 125°C			125	
Pass-element series resistance	$(4.88\text{ V} - V_O)/I_O$, $I_O = 250$ mA	$V_I = 4.88$ V,	25°C		0.27	0.35	Ω
			−40°C to 125°C			0.5	
Input regulation	$V_I = 6$ V to 10 V,	$50\text{ µA} \le I_O \le 250$ mA	25°C		4	20	mV
			−40°C to 125°C			45	
Output regulation	$I_O = 5$ mA to 250 mA,	$6\text{ V} \le V_I \le 10$ V	25°C		28	40	mV
			−40°C to 125°C			75	
	$I_O = 50$ µA to 250 mA,	$6\text{ V} \le V_I \le 10$ V	25°C		41	65	mV
			−40°C to 125°C			130	
Ripple rejection	f = 120 Hz	$I_O = 50$ µA	25°C	43	53		dB
			−40°C to 125°C	38			
		$I_O = 250$ mA	25°C	41	51		
			−40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C		2		µV/√Hz
Output noise voltage	$10\text{ Hz} \le f \le 100$ kHz, CSR† = 1 Ω	$C_O = 4.7$ µF	25°C		430		µVrms
		$C_O = 10$ µF	25°C		345		
		$C_O = 100$ µF	25°C		220		
$\overline{\text{RESET}}$ trip-threshold voltage	V_O decreasing		−40°C to 125°C	4.55		4.75	V
$\overline{\text{RESET}}$ trip-threshold voltage	V_O increasing		−40°C to 125°C				V
$\overline{\text{RESET}}$ hysteresis voltage			25°C		28		mV
$\overline{\text{RESET}}$ output low voltage	$I_{O(RESET)} = -1.2$ mA, $V_I = 4.25$ V		25°C		0.15	0.4	V
			−40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

switching characteristics

PARAMETER	TEST CONDITIONS	T_J	TPS7301Q, TPS7333Q TPS7348Q, TPS7350Q			UNIT
			MIN	TYP	MAX	
$\overline{RESET}$ time-out delay	See Figure 5	25°C	140	200	260	ms
		−40°C to 125°C	100		300	

electrical characteristics at I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF(CSR† = 1 Ω), T_J = 25°C, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	TPS7301Y, TPS7333Y TPS7348Y, TPS7350Y			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	$\overline{EN}$ ≤ 0.5 V, $V_I = V_O + 1$ V, 0 mA ≤ I_O ≤ 250 mA		340		μA
Input current (standby mode)	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V		0.01		μA
Output current limit	V_O = 0 V, V_I = 10 V		1.2		A
Pass-element leakage current in standby mode	$\overline{EN} = V_I$, 2.7 V ≤ V_I ≤ 10 V		0.01		μA
$\overline{RESET}$ leakage current	Normal operation, V at $\overline{RESET}$ = 10 V		0.02		μA
Thermal shutdown junction temperature			165		°C
$\overline{EN}$ logic low (active mode)	2.7 V ≤ V_I ≤ 10 V				V
$\overline{EN}$ hysteresis voltage			50		mV
$\overline{EN}$ input current	0 V ≤ V_I ≤ 10 V		0.001		μA
Minimum V_I for active pass element			2.05		V
Minimum V_I for valid $\overline{RESET}$	$I_{O(\overline{RESET})}$ = −300 μA		1		V

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7301Y electrical characteristics at $I_O = 10$ mA, $V_I = 3.5$ V, $\overline{EN} = 0$ V, $C_O = 4.7\ \mu F$(CSR† = 1 Ω), $T_J = 25°C$, FB shorted to OUT at device leads (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7301Y MIN	TPS7301Y TYP	TPS7301Y MAX	UNIT
Reference voltage (measured at FB)	$V_I = 3.5$ V,	$I_O = 10$ mA		1.182		V
Pass-element series resistance (see Note 2)	$V_I = 2.4$ V,	$50\ \mu A \le I_O \le 150$ mA		0.7		Ω
	$V_I = 2.4$ V,	$150\ mA \le I_O \le 250$ mA		0.83		
	$V_I = 2.9$ V,	$50\ \mu A \le I_O \le 250$ mA		0.52		
	$V_I = 3.9$ V,	$50\ \mu A \le I_O \le 250$ mA		0.32		
	$V_I = 5.9$ V,	$50\ \mu A \le I_O \le 250$ mA		0.23		
Input regulation	$V_I = 2.5$ V to 10 V, See Note 1	$50\ \mu A \le I_O \le 250$ mA,		3		mV
Output regulation	$2.5\ V \le V_I \le 10$ V, See Note 1	$I_O = 5$ mA to 250 mA,		5		mV
	$2.5\ V \le V_I \le 10$ V, See Note 1	$I_O = 50\ \mu A$ to 250 mA,		7		mV
Ripple rejection	f = 120 Hz	$I_O = 50\ \mu A$		59		dB
	f = 120 Hz	$I_O = 250$ mA, See Note 1		54		
Output noise-spectral density	f = 120 Hz			2		$\mu V/\sqrt{Hz}$
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	$C_O = 4.7\ \mu F$		95		µVrms
		$C_O = 10\ \mu F$		89		
		$C_O = 100\ \mu F$		74		
$\overline{RESET}$ hysteresis voltage§	Measured at $V_{O(FB)}$			12		mV
$\overline{RESET}$ output low voltage§	$V_I = 2.13$ V,	$I_{O(RESET)} = 400\ \mu A$		0.1		V
FB input current				0.1		nA

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.
§ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 1. When $V_I < 2.9$ V and $I_O > 150$ mA simultaneously, pass element $r_{DS(on)}$ increases (see Figure 32) to a point where the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.
2. To calculate dropout voltage, use equation: $V_{DO} = I_O \cdot r_{DS(on)}$
$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for $V_I = 2.4$ V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V respectively. For other programmed values, refer to Figure 32.

TPS7333Y electrical characteristics at I_O = 10 mA, V_I = 4.3 V, $\overline{EN}$ = 0 V, C_O = 4.7 µF(CSR† = 1 Ω), T_J = 25°C, SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7333Y MIN	TPS7333Y TYP	TPS7333Y MAX	UNIT
Output voltage	V_I = 4.3 V,	I_O = 10 mA		3.3		V
Dropout voltage	I_O = 10 mA,	V_I = 3.23 V		4.5		mV
	I_O = 100 mA,	V_I = 3.23 V		44		
	I_O = 250 mA,	V_I = 3.23 V		108		
Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 250 mA	V_I = 3.23 V,		0.44		Ω
Input regulation	V_I = 4.3 V to 10 V,	50 µA ≤ I_O ≤ 250 mA		6		mV
Output regulation	I_O = 5 mA to 250 mA,	4.3 V ≤ V_I ≤ 10 V		21		mV
	I_O = 50 µA to 250 mA,	4.3 V ≤ V_I ≤ 10 V		31		mV
Ripple rejection	f = 120 Hz	I_O = 50 µA		51		dB
		I_O = 250 mA		49		
Output noise-spectral density	f = 120 Hz			2		µV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 µF		274		µVrms
		C_O = 10 µF		228		
		C_O = 100 µF		159		
$\overline{RESET}$ hysteresis voltage				18		mV
$\overline{RESET}$ output low voltage	V_I = 2.8 V,	$I_{O(RESET)}$ = –1 mA		0.17		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7348Y electrical characteristics at I_O = 10 mA, V_I = 5.85 V, $\overline{EN}$ = 0 V, C_O = 4.7 μF(CSR† = 1 Ω), SENSE shorted to OUT (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		TPS7348Y MIN	TPS7348Y TYP	TPS7348Y MAX	UNIT
Output voltage	V_I = 5.85 V,	I_O = 10 mA		4.85		V
Dropout voltage	I_O = 10 mA,	V_I = 4.75 V		2.9		mV
	I_O = 100 mA,	V_I = 4.75 V		28		
	I_O = 250 mA,	V_I = 4.75 V		70		
Pass-element series resistance	(4.75 V – V_O)/I_O, I_O = 250 mA	V_I = 4.75 V,		0.28		Ω
Input regulation	V_I = 5.85 V to 10 V,	50 μA ≤ I_O ≤ 250 mA		9		mV
Output regulation	I_O = 5 mA to 250 mA,	5.85 V ≤ V_I ≤ 10 V		28		mV
	I_O = 50 μA to 250 mA,	5.85 V ≤ V_I ≤ 10 V		42		mV
Ripple rejection	f = 120 Hz	I_O = 50 μA		53		dB
		I_O = 250 mA		50		
Output noise-spectral density	f = 120 Hz			2		μV/√Hz
Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω	C_O = 4.7 μF		410		μVrms
		C_O = 10 μF		328		
		C_O = 100 μF		212		
$\overline{RESET}$ hysteresis voltage				26		mV
$\overline{RESET}$ output low voltage	$I_{O(RESET)}$ = –1.2 mA, V_I = 4.12 V			0.2		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.
‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER MEASUREMENT INFORMATION

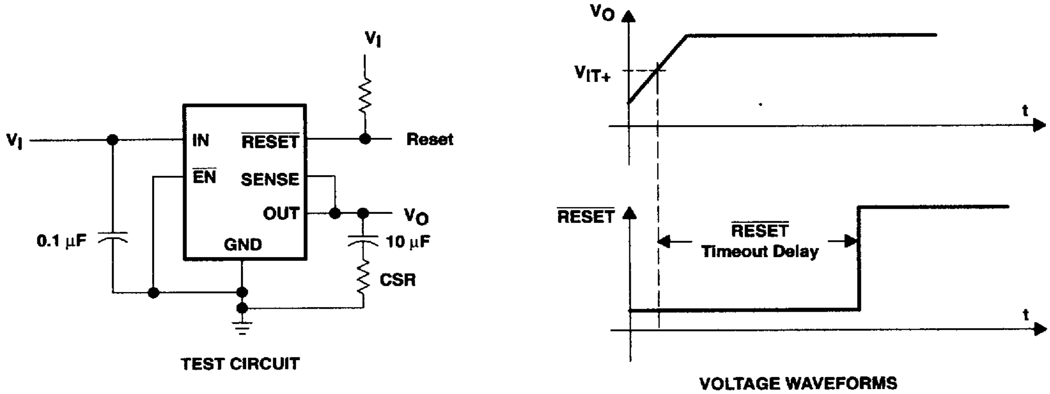


Figure 5. Test Circuit and Voltage Waveforms

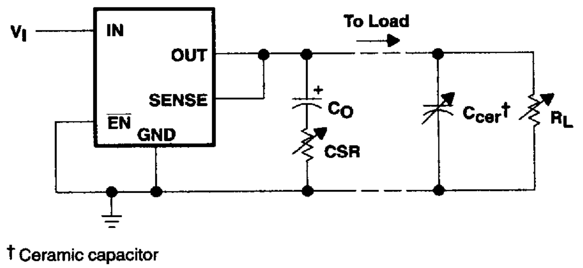


Figure 6. Test Circuit for Typical Regions of Stability (Refer to Figures 28 through 31)

TYPICAL CHARACTERISTICS

Table of Graphs

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TYPICAL CHARACTERISTICS

QUIESCENT CURRENT vs OUTPUT CURRENT

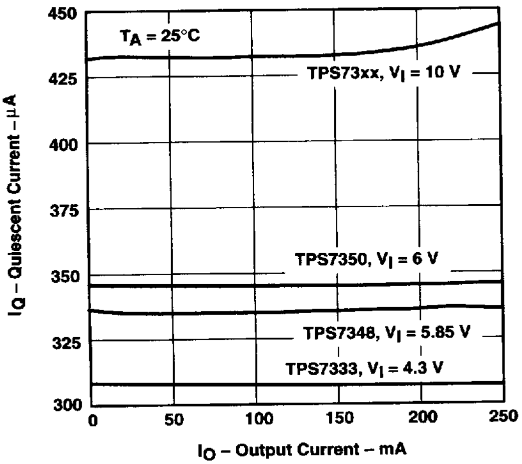


Figure 7

QUIESCENT CURRENT vs INPUT VOLTAGE

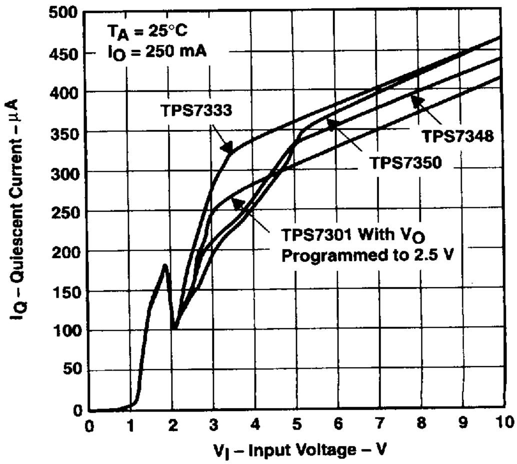


Figure 8

TPS7348Q QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

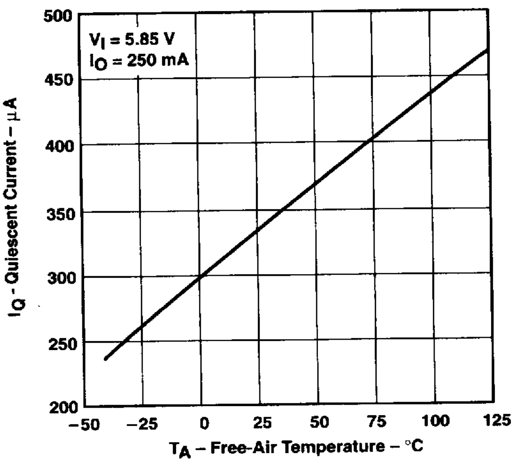


Figure 9

DROPOUT VOLTAGE vs OUTPUT CURRENT

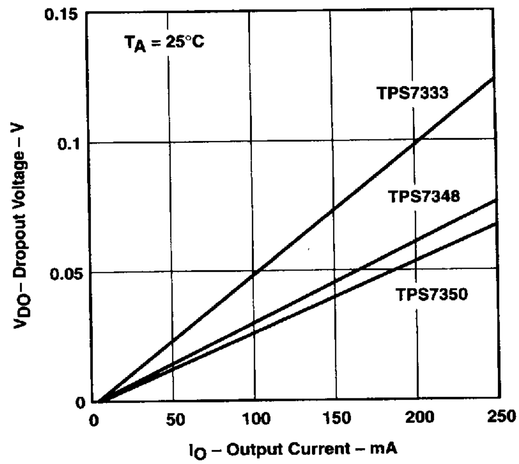


Figure 10

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

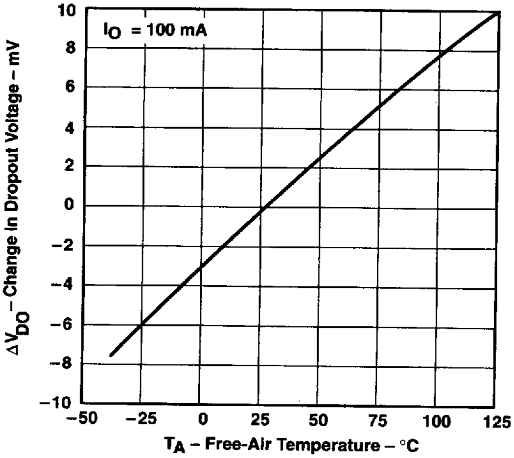


Figure 11

TPS7301 DROPOUT VOLTAGE vs OUTPUT CURRENT

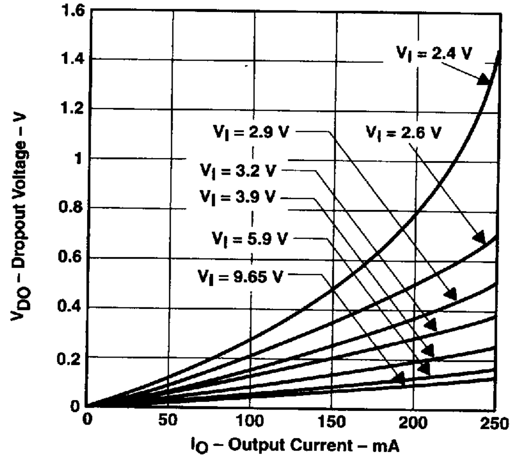


Figure 12

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

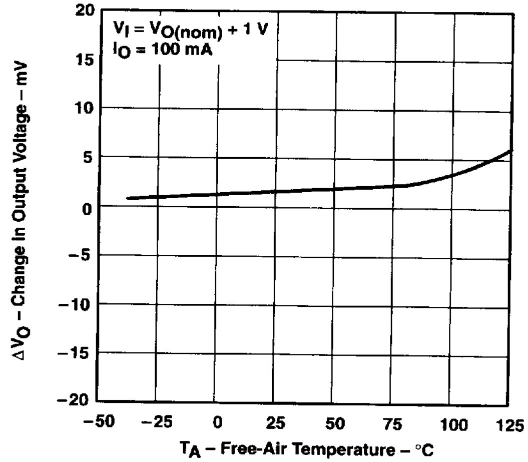


Figure 13

OUTPUT VOLTAGE vs INPUT VOLTAGE

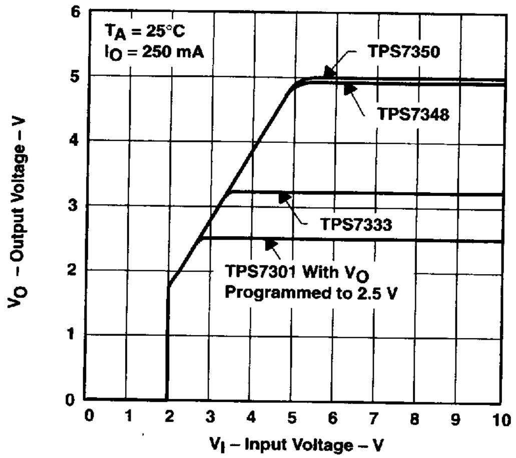


Figure 14

TYPICAL CHARACTERISTICS

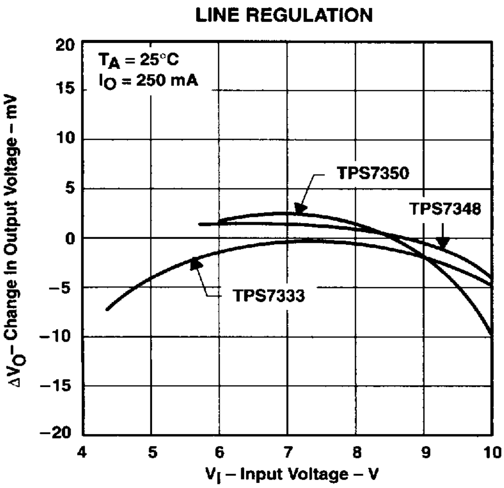


Figure 15

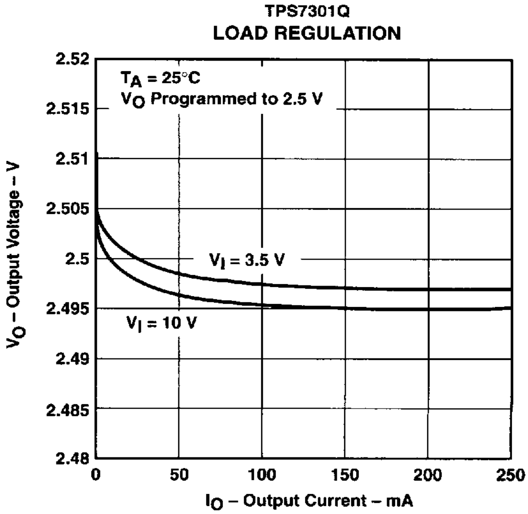


Figure 16

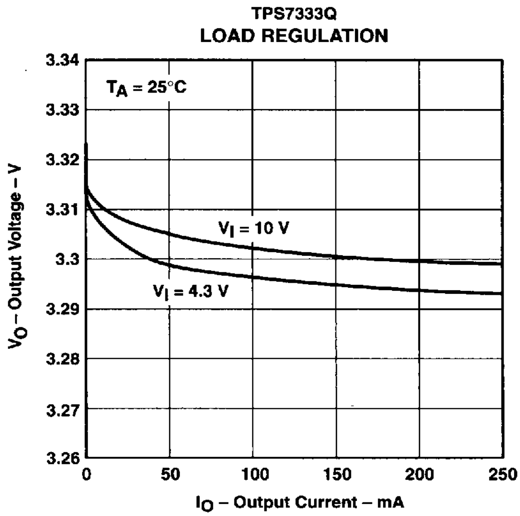


Figure 17

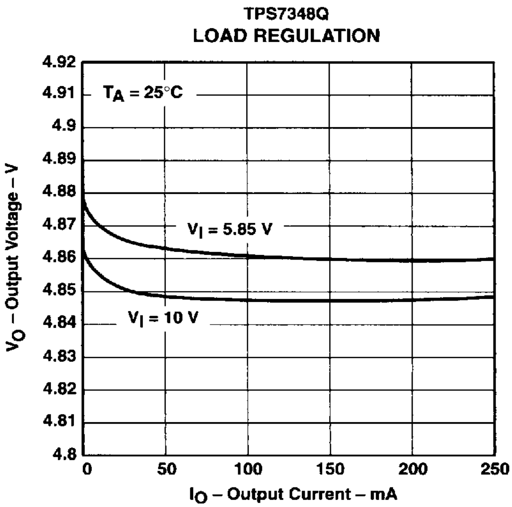


Figure 18

TYPICAL CHARACTERISTICS

TPS7350Q
LOAD REGULATION

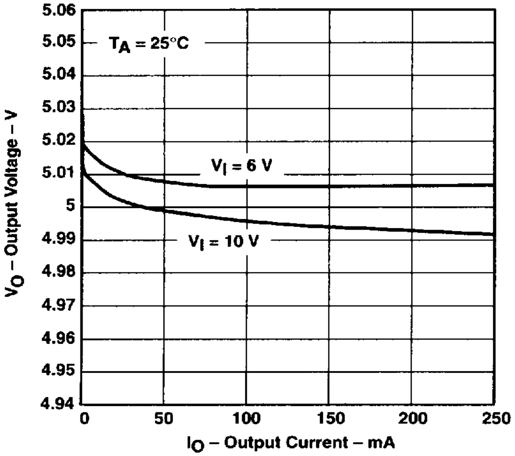


Figure 19

OUTPUT VOLTAGE RESPONSE FROM ENABLE ($\overline{EN}$)

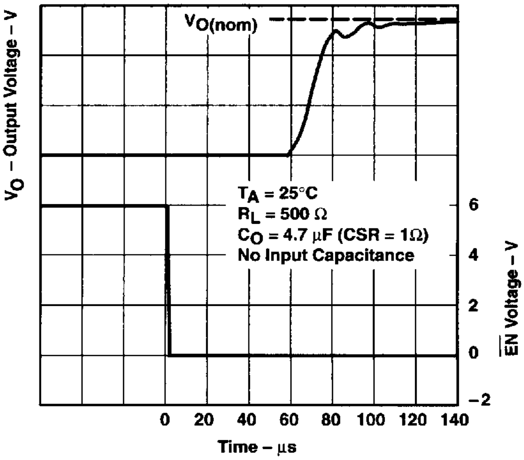


Figure 20

TPS7301 (WITH V_O PROGRAMMED TO 2.5 V) OR TPS7333
LOAD TRANSIENT RESPONSE

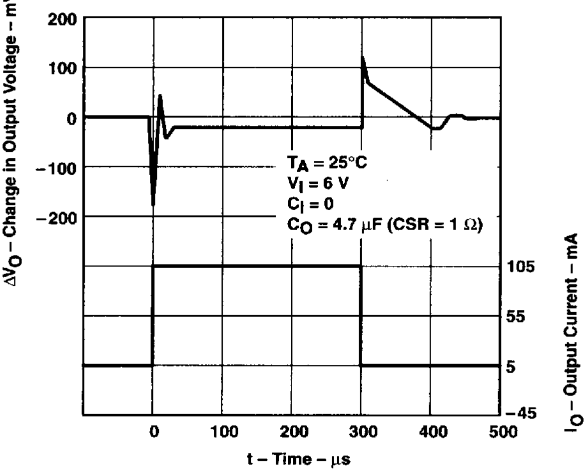


Figure 21

TYPICAL CHARACTERISTICS

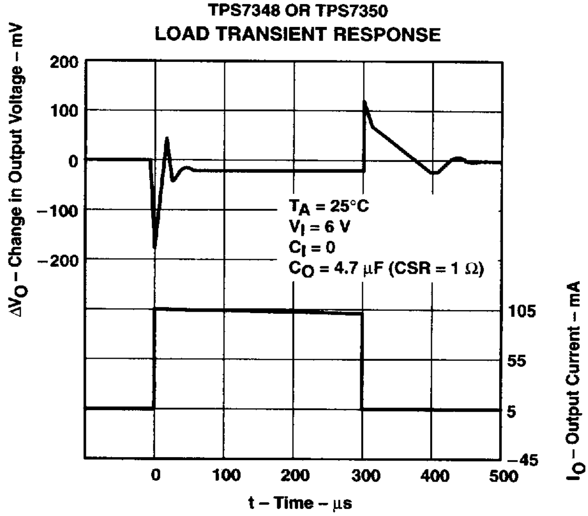


Figure 22

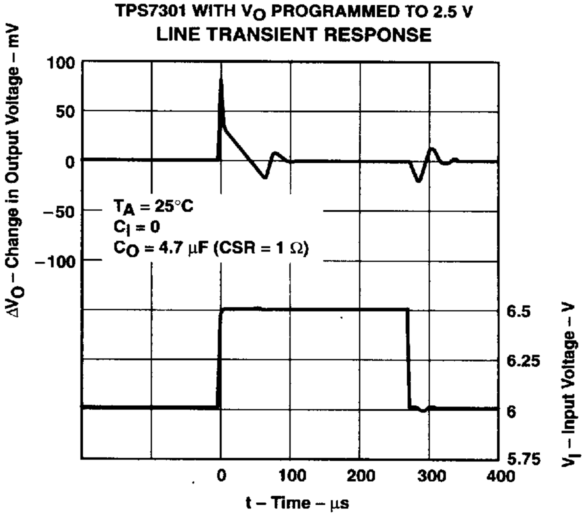


Figure 23

TYPICAL CHARACTERISTICS

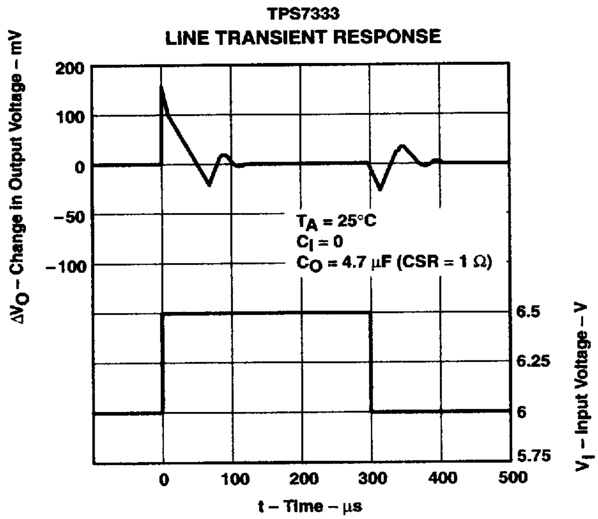


Figure 24

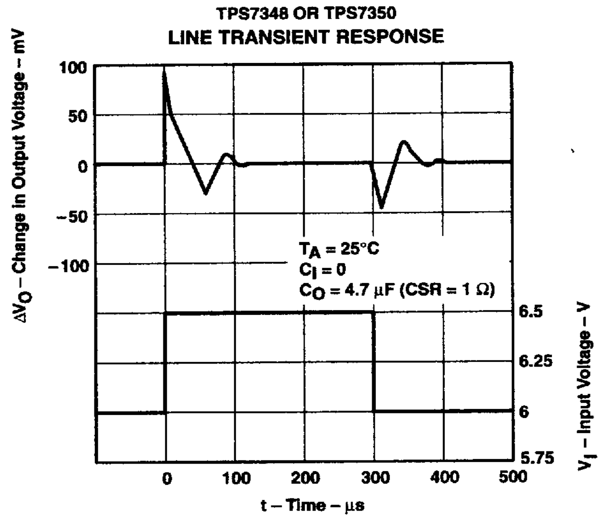


Figure 25

TYPICAL CHARACTERISTICS

**RIPPLE REJECTION
vs
FREQUENCY**

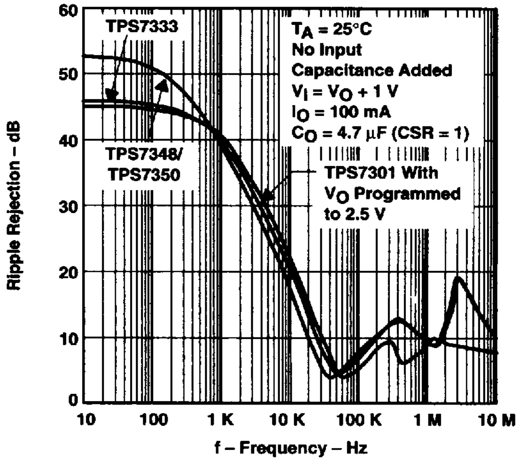


Figure 26

**OUTPUT SPECTRAL-NOISE DENSITY
vs
FREQUENCY**

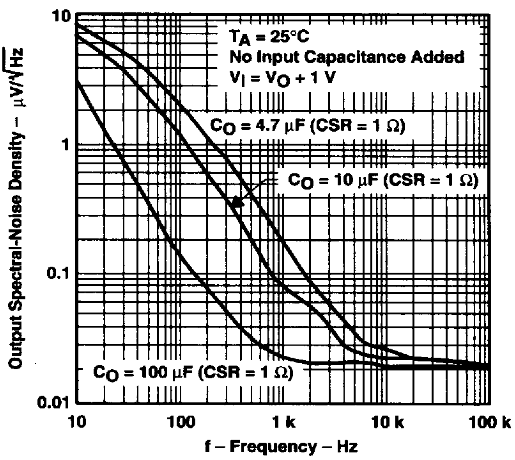


Figure 27

TYPICAL CHARACTERISTICS

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT

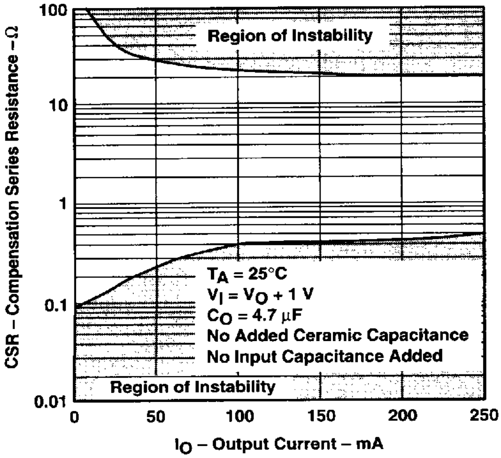


Figure 28

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE

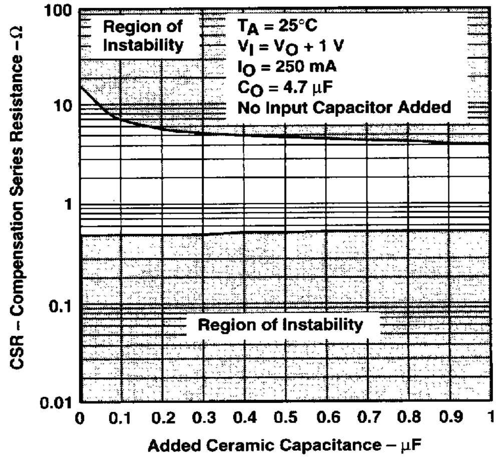


Figure 29

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT

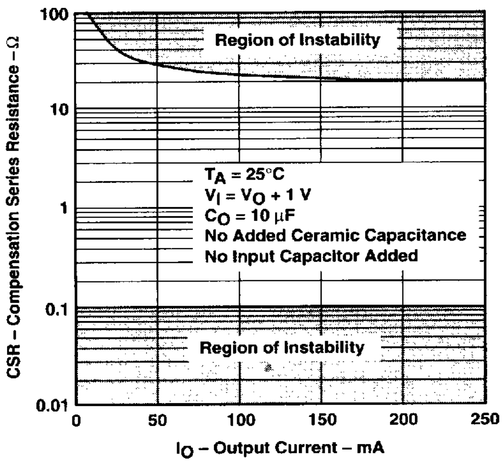


Figure 30

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE

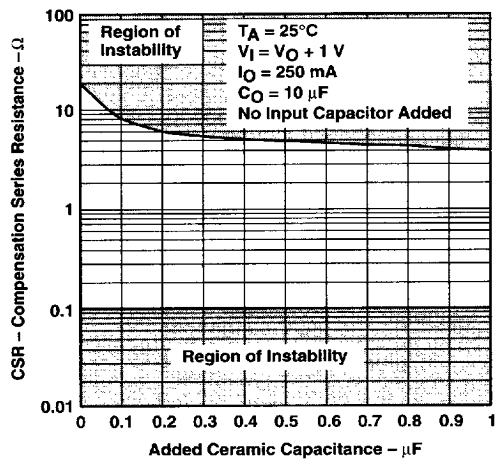


Figure 31

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TYPICAL CHARACTERISTICS

PASS-ELEMENT RESISTANCE vs INPUT VOLTAGE

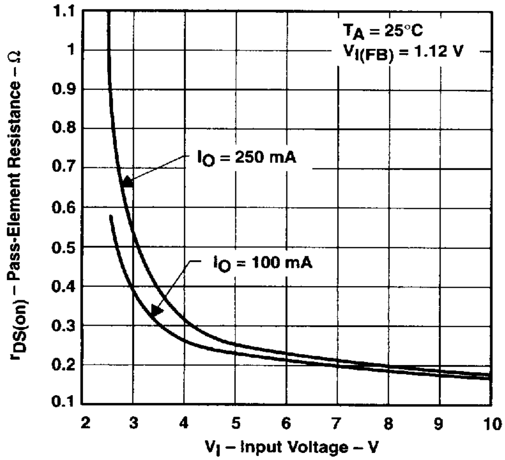


Figure 32

MINIMUM INPUT VOLTAGE FOR VALID $\overline{\text{RESET}}$ vs FREE-AIR TEMPERATURE

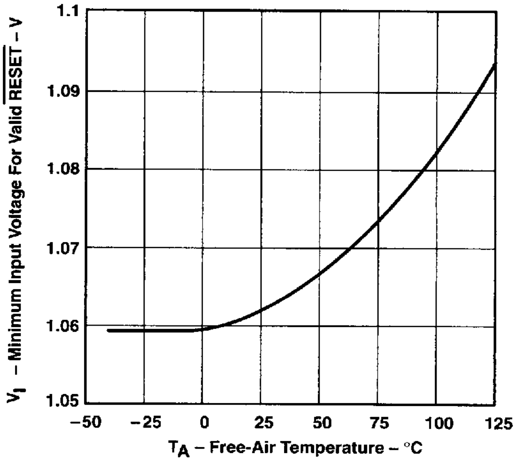


Figure 33

NEGATIVE-GOING RESET THRESHOLD vs FREE-AIR TEMPERATURE

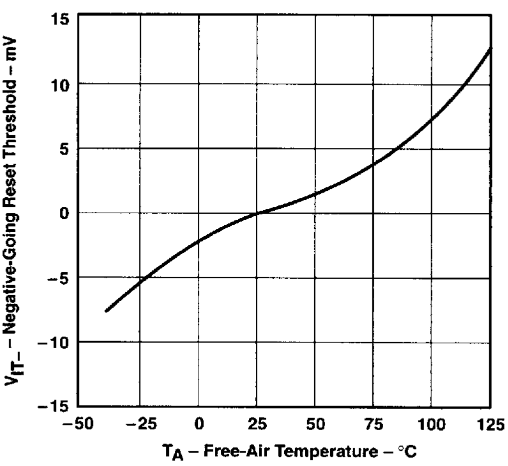


Figure 34

$\overline{\text{RESET}}$ OUTPUT CURRENT vs INPUT VOLTAGE

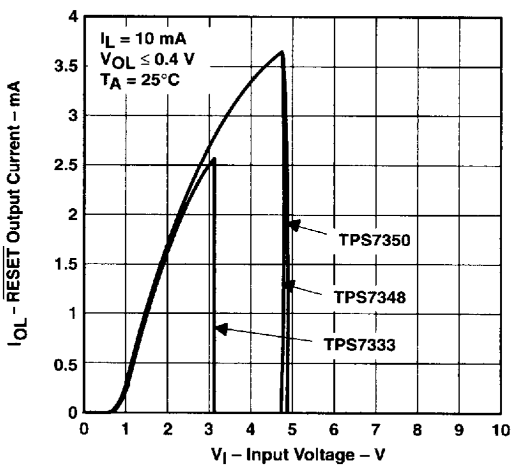


Figure 35

8961724 0099630 2T8

TYPICAL CHARACTERISTICS

RESET DELAY TIME vs FREE-AIR TEMPERATURE

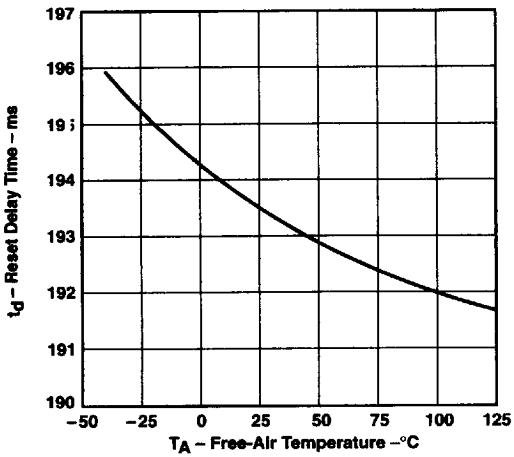


Figure 36

DISTRIBUTION FOR RESET DELAY

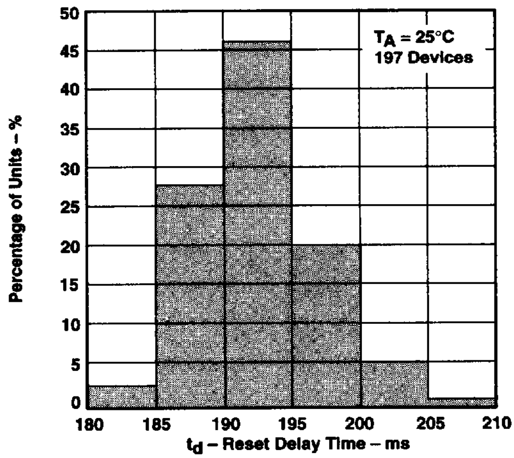


Figure 37

THERMAL INFORMATION

In response to system-miniaturization trends, integrated circuits are being offered in low-profile and fine-pitch surface-mount packages. Implementation of many of today's high-performance devices in these packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are illustrated in this discussion:

- Improving the power-dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

Figure 38 is an example of a thermally enhanced PWB layout for the 20-lead TSSOP package. This layout involves adding copper on the PWB to conduct heat away from the device. The $R_{\theta JA}$ for this component/board system is illustrated in Figure 39. The family of curves illustrates the effect of increasing the size of the copper-heat-sink surface area. The PWB is a standard FR4 board (L × W × H = 3.2 inch × 3.2 inch × 0.062 inch); the board traces and heat sink area are 1-oz (per square foot) copper.

Figure 40 shows the thermal resistance for the same system with the addition of a thermally conductive compound between the body of the TSSOP package and the PWB copper routed directly beneath the device. The thermal conductivity for the compound used in this analysis is 0.815 W/m · °C.

Using these figures to determine the system $R_{\theta JA}$ allows the maximum power-dissipation limit to be calculated with the equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}}$$

Where

$T_{J(max)}$ is the maximum allowable junction temperature or 125°C i.e., 150°C absolute maximum and 125°C maximum recommended operating temperature for specified operation.

This limit should then be applied to the internal power dissipated by the TPS73xx regulator. The equation for calculating total internal power dissipation of the TPS71xx is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O + V_I \cdot I_Q$$

Because the quiescent current of the TPS73xx family is very low, the second term is negligible, further simplifying the equation to:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O$$

For a 20-lead TSSOP/FR4 board system with thermally conductive compound between the board and the device body, where $T_A = 55°C$, airflow = 100 ft/min, and copper heat sink area = 1 cm^2, the maximum power-dissipation limit can be calculated. As indicated in Figure 40, the system $R_{\theta JA}$ is 94°C/W; therefore, the maximum power-dissipation limit is:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(system)}} = \frac{125°C - 55°C}{94°C/W} = 745 \text{ mW}$$

If the system implements a TPS7348 regulator where $V_I = 6$ V and $I_O = 385$ mA, the internal power dissipation is:

$$P_{D(total)} = \left(V_I - V_O\right) \cdot I_O = (6 - 4.85) \cdot 0.385 = 443 \text{ mW}$$

THERMAL INFORMATION

Comparing $P_{D(total)}$ with $P_{D(max)}$ reveals that the power dissipation in this example does not exceed the maximum limit. When it does, one of two corrective actions can be taken. The power-dissipation limit can be raised by increasing either the airflow or the heat-sink area. Alternatively, the internal power dissipation of the regulator can be lowered by reducing either the input voltage or the load current. In either case, the above calculations should be repeated with the new system parameters.

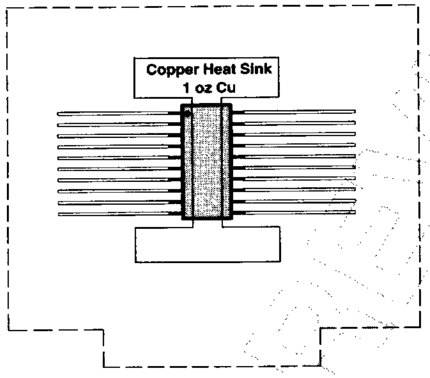


Figure 38. Thermally Enhanced PWB Layout (not to scale) for the 20-Pin TSSOP

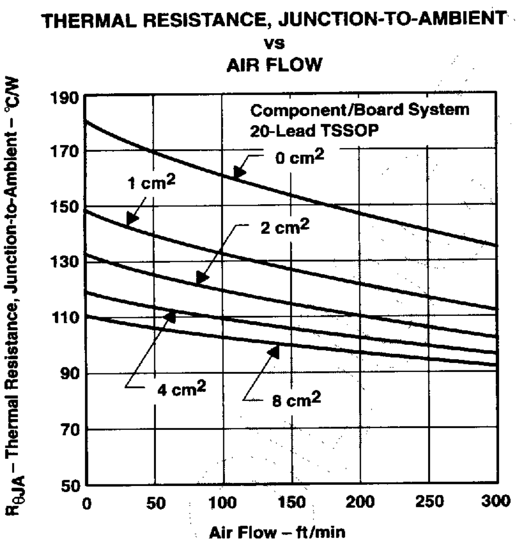


Figure 39

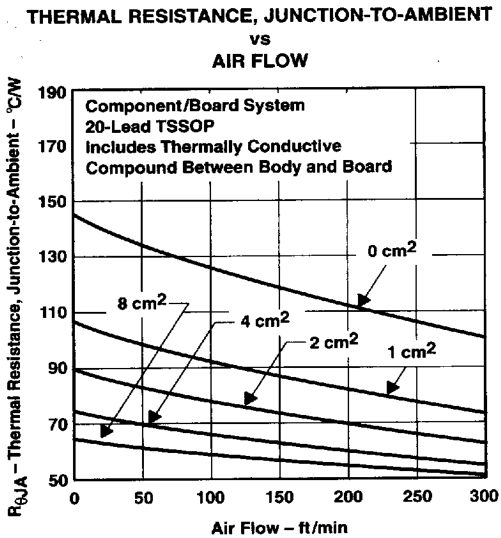


Figure 40

APPLICATION INFORMATION

The TPS73xx series of low-dropout (LDO) regulators is designed to overcome many of the shortcomings of earlier generation LDOs, while adding features such as a power-saving shutdown mode and a supply-voltage supervisor. The TPS73xx family includes three fixed-output voltage regulators: the TPS7333 (3.3 V), the TPS7348 (4.85 V), and the TPS7350 (5 V). The family also offers an adjustable device, the TPS7301 (adjustable from 1.2 V to 9.75 V).

device operation

The TPS73xx, unlike many other LDOs, features very low quiescent currents that remain virtually constant even with varying loads. Conventional LDO regulators use a pnp-pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that such devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS73xx uses a PMOS transistor to pass current; because the gate of the PMOS element is voltage driven, operating currents are low and invariable over the full load range. The TPS73xx specifications reflect actual performance under load.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power-up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS73xx quiescent current remains low even when the regulator drops out, thus eliminating both problems.

Included in the TPS73xx family is a 4.85-V regulator, the TPS7348. Designed specifically for 5-V cellular systems, its 4.85-V output, regulated to within ± 2%, allows for operation within the low-end limit of 5-V systems specified to ± 5% tolerance; therefore, maximum regulated operating lifetime is obtained from a battery pack before the device drops out, adding crucial talk minutes between charges.

The TPS73xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 0.5 μA. When the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 120 μs.

minimum load requirements

The TPS73xx family is stable even at zero load; no minimum load is required for operation.

SENSE-pin connection

The SENSE terminal of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way as to minimize/avoid noise pickup. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection when the TPS73xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

APPLICATION INFORMATION

external capacitor requirements (continued)

As with most LDO regulators, the TPS73xx family requires an output capacitor for stability. A low-ESR 10-µF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 41). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106K035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to −40°C). Where component height and/or mounting area is a problem, physically smaller, 10-µF devices can be screened for ESR. Figures 28 through 31 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2 µF), the output capacitance can be reduced to 4.7 µF, provided ESR is maintained between 0.7 and 2.5 Ω. Because capacitor minimum ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the CSR graphs (Figures 28 through 31), minimum ESR is not a problem when using 10-µF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS73xx family. This information, along with the CSR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1 µF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 µF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 µF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 µF, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 µF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 µF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 µF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 µF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 µF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 µF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 µF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 µF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 µF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 µF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 µF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.

APPLICATION INFORMATION

external capacitor requirements (continued)

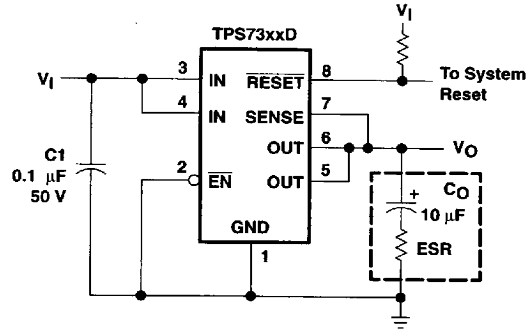


Figure 41. Typical Application Circuit

programming the TPS7301 adjustable LDO regulator

Programming the adjustable regulators is accomplished using an external resistor divider as shown in Figure 42. The equation governing the output voltage is:

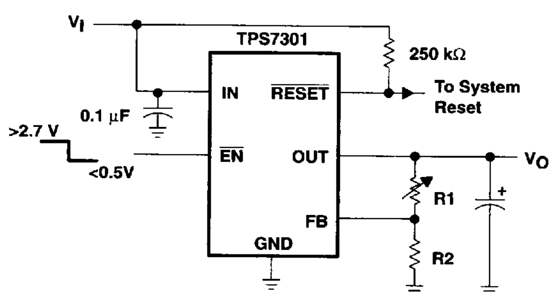
$$V_O = V_{ref} \cdot \left(1 + \frac{R1}{R2}\right) \tag{1}$$

where

V_{ref} = reference voltage, 1.182 V typ

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. A recommended value for R2 is 169 kΩ with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving equation 1 for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	191	169	kΩ
3.3 V	309	169	kΩ
3.6 V	348	169	kΩ
4 V	402	169	kΩ
5 V	549	169	kΩ
6.4 V	750	169	kΩ

Figure 42. TPS7301 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

undervoltage supervisor function

The $\overline{\text{RESET}}$ output of the TPS73xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS73xx monitors the output voltage of the regulator to detect the undervoltage condition. When that occurs, the $\overline{\text{RESET}}$ output transistor turns on taking the $\overline{\text{RESET}}$ signal low.

On power-up, the output voltage tracks the input voltage. The $\overline{\text{RESET}}$ output becomes active (low) as V_I approaches the minimum required for a valid $\overline{\text{RESET}}$ signal (specified at 1.5 V for 25°C and 1.9 V over full recommended operating temperature range). When the output voltage reaches the appropriate positive-going input threshold (V_{IT+}), a 200-ms (typ) timeout period begins during which the $\overline{\text{RESET}}$ output remains low. Once the timeout has expired, the $\overline{\text{RESET}}$ output become inactive. Since the $\overline{\text{RESET}}$ output is an open-drain NMOS, a pull-up resistor should be used to ensure that a logic-high signal is indicated.

The supply-voltage-supervisor function is also activated during power-down. As the input voltage decays and after the dropout voltage is reached, the output voltage tracks linearly with the decaying input voltage. When the output voltage drops below the specified negative-going input threshold (V_{IT-} — see electrical characteristics tables), the $\overline{\text{RESET}}$ output becomes active (low). It is important to note that if the input voltage decays below the minimum required for a valid $\overline{\text{RESET}}$, the $\overline{\text{RESET}}$ is undefined.

Since the circuit is monitoring the regulator output voltage, the $\overline{\text{RESET}}$ output can also be triggered by disabling the regulator or by any fault condition that causes the output to drop below V_{IT-}. Examples of fault conditions include a short circuit on the output and a low input voltage. Once the output voltage is reestablished, either by reenabling the regulator or removing the fault condition, then the internal timer is initiated, which holds the $\overline{\text{RESET}}$ signal active during the 200-ms (typ) timeout period.

NOTE:
$V_{IT+} = V_{IT-}$ +Hysteresis

output noise

The TPS73xx has very low output noise, with a spectral noise density < 2 $\mu V/\sqrt{Hz}$. This is important when noise-susceptible systems, such as audio amplifiers, are powered by the regulator.

regulator protection

The TPS73xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS73xx also features internal current limiting and thermal protection. During normal operation, the TPS73xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

APPLICATION INFORMATION

power dissipation and junction temperature

The junction temperature must be held to 150°C or less to ensure proper regulator operation, which limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

$T_J max$ is the maximum allowable junction temperature, i.e.,150°C absolute maximum and 125°C recommended operating temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 238°C/W for the 8-terminal TSSOP.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \cdot I_O$$

Power dissipation resulting from quiescent current is negligible.