



# SSI 32P541

## Read Data Processor

T-52-38

February, 1990

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### DESCRIPTION

The SSI 32P541 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals. The circuit will handle data rates up to 15 Mbit/s.

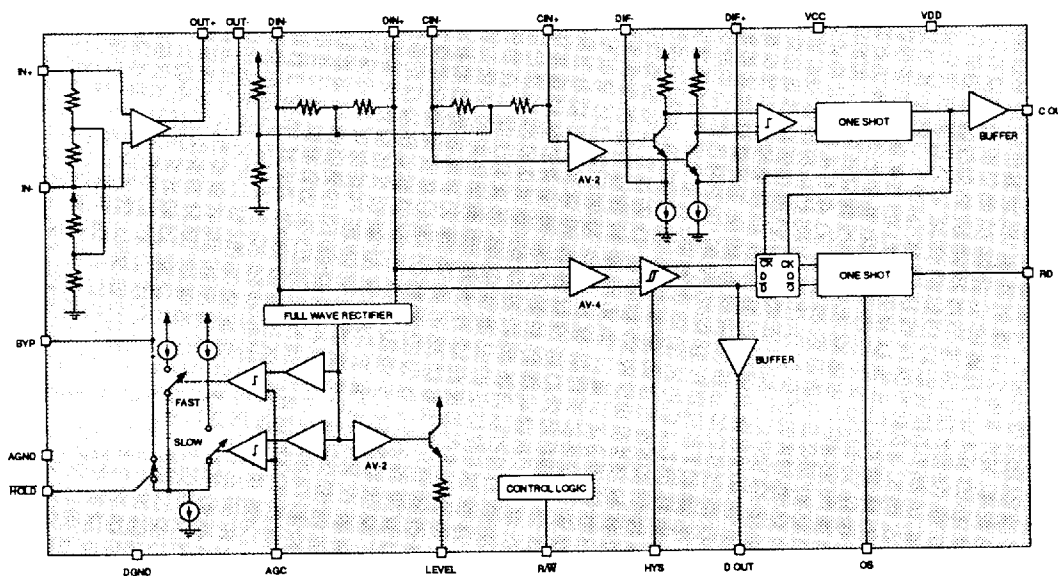
In read mode the SSI 32P541 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast setting of the input coupling capacitors during a write to read transition. The SSI 32P541 requires +5V and +12V power supplies and is available in a 24-pin DIP and 28-pin PLCC.

### FEATURES

- Level qualification supports high resolution MFM and RLL encoded data retrieval
- Wide bandwidth AGC input amplifier
- Supports data rates up to 15 Mbit/s
- Standard  $12V \pm 10\%$  and  $5V \pm 10\%$  supplies
- Supports embedded servo pattern decoding
- Write to read transient suppression
- Fast and slow AGC attack regions for fast transient recovery

### BLOCK DIAGRAM



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## CIRCUIT OPERATION

## READ MODE

In the read mode (R/W input high or open) the input read signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

The amplified head signals are AC coupled to the IN+ and IN- pins of the AGC amplifier that is gain controlled by full wave rectifying and amplifying the (DIN+ - DIN-) voltage level and comparing it to a reference level at the AGC pin. A fast attack mode, which supplies a 1.7 mA charging current for the capacitor at the BYP pin, is entered whenever the instantaneous DIN± level is more than 125% of set level. Between 100% and 125% the slow attack mode is invoked, providing 0.18 mA of charging current. The two attack modes allow rapid AGC recovery from a write to read transition while reducing zero crossing distortion once the amplifier is in range.

The level at the AGC pin should be set such that the differential voltage level at the DIN+, DIN- pins is 1.00 Vpp at the OUT+, OUT- pins which allows for up to 6 dB loss in any external filter connected between the OUT+, OUT- outputs and the DIN+, DIN- inputs.

Gain of the AGC section is nominally

$$\frac{Av2}{Av1} = \exp - \left( \frac{V2 - V1}{5.8 + V1} \right)$$

Where: Av1 and Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

$V1 = (K \times T)/q = 26 \text{ mV}$  at room temperature.

One filter for both data (DIN+, DIN- input) and clock (CIN+, CIN- input) paths, or a separate filter for each path may be used. If two filters are used, care must be exercised to control time delays so that each path is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

The filtered data path signal is fed into a hysteresis comparator that is set at a fraction of the input signal level by using an external filter/network between the LEVEL and HYS pins. Using this approach allows

setting the AGC slow attack and decay times slow enough to minimize distortion of the clock path signal. This "feed-forward" technique, utilizing a fraction of the rectified data path input available at the LEVEL pin as the hysteresis threshold, is especially useful in the slow decay mode of the AGC loop. By using a short time constant for the hysteresis level, the qualification method can continue as the AGC amplifier gain is slowly ramped up. This level will also shorten the write to read transient recovery time without affecting data timing as the circuit will be properly decoding before the AGC gain has settled to its final value. The comparator output is the "D" input of a D type flip-flop. The DOUT pin provides a buffered test point for monitoring this function.

The filtered clock path signal is differentiated to transform signal peaks to zero-crossings which clock an edge-trigger circuit to provide output pulses at each zero-crossing. The pulses are used to clock the D type flip-flop. The COUT pin is a buffered test point for monitoring this function.

The differentiator function is set by an external network between the DIF+, DIF- pins. The transfer function is:

$$AV = \frac{-2000Cs}{LCs^2 + (R + 92)Cs + 1}$$

Where: C = external capacitor (20 pF to 150 pF)

L = external inductor

R = external resistor

$s = j\omega = j2\pi f$

During normal operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to CIN+, CIN-. The D input to the flip-flop only changes state when the signal applied to the DIN+, DIN- inputs exceeds the hysteresis comparator threshold opposite in polarity to the previous peak that exceeded the threshold.

The clocking path, then, determines signal timing and the data path determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold.

The delays from CIN+, CIN- inputs to the flip-flop clock input and from the DIN+, DIN- inputs to the flip-flop D input are well matched.

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**WRITE (DISABLED) MODE**

In the write or disabled mode ( $R/\overline{W}$  input low) the digital circuitry is disabled and the AGC amplifier input impedance is reduced. In addition the AGC amplifier gain is set to maximum so that the loop is in its fast attack mode when changing back to Read Mode. The lowered input impedance facilitates more rapid settling of the write to read transient by reducing the time constant of the network between the SSI 32P541 and read/write preamplifier, such as the SSI 32R510.

Internal SSI 32P541 timing is such that this settling is accomplished before the AGC loop is activated when going to read mode. Coupling capacitors should be chosen with as low a value as possible, consistent with bandwidth requirements, to allow more rapid settling.

**LAYOUT CONSIDERATIONS**

The SSI 32P541 is a high gain wide bandwidth device

that requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 32P541 and associated circuitry grounds from other circuits on the disk drive PCB.

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R/W	HOLD	MODE
1	1	READ - Read amp on, AGC active, Digital section active
1	0	HOLD - Read amp on, AGC gain held constant Digital section active
0	X	WRITE - AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced

**PIN DESCRIPTION**

NAME	TYPE	DESCRIPTION
VCC	-	5 volt power supply
VDD	-	12 volt power supply
AGND, DGND	-	Analog and Digital ground pins
R/W	I	TTL compatible read/write control pin
IN+, IN-	I	Analog signal input pins
OUT+, OUT-	O	AGC Amplifier output pins
BYP	-	The AGC timing capacitor is tied between this pin and AGND
HOLD	I	TTL compatible pin that holds the AGC gain when pulled low
AGC	I	Reference input voltage level for the AGC circuit
DIN+, DIN-	I	Analog input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
LEVEL	O	Provides rectified signal level for input to the hysteresis comparator
DOUT	O	Buffered test point for monitoring the flip-flop D input
CIN+, CIN-	I	Analog input to the differentiator
DIF+, DIF-	-	Pins for external differentiating network
COUT	O	Buffered test point for monitoring the clock input to the flip-flop
OS	-	Connection for read output pulse width setting capacitor
RD	O	TTL compatible read output

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# ELECTRICAL SPECIFICATIONS

Unless otherwise specified  $4.5 \leq VCC \leq 5.5V$ ,  $10.8V \leq VDD \leq 13.2V$ ,  $25^\circ C \leq T_J \leq 135^\circ C$ .

## ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6	V
12V Supply Voltage, VDD	14	V
Storage Temperature	-65 to 150	°C
Lead Temperature	260	°C
R/W, IN+, IN-, HOLD	-0.3 to VCC + 0.3	V
RD	-0.3V to VCC + 0.3V or +12	mA
All others	-0.3 to VDD + 0.3	V

## POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC - VCC Supply Current	Outputs unloaded			14	mA
IDD - VDD Supply Current	Outputs unloaded			70	mA
Pd - Power Dissipation	Outputs unloaded, $T_J = 135^\circ C$			730	mW

## LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIL - Input Low Voltage		-0.3		0.8	V
VIH - Input High Voltage		2.0			V
IIL - Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH - Input High Current	VIH = 2.4V			100	μA
VOL - Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH - Output High Voltage	IOH = -400 μA	2.4			V

## MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read to Write Transition Time				1.0	μs
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2		3.0	μs
Read to Hold Transition Time				1.0	μs

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## WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Common Mode Input Impedance (both sides)	R/W pin = low		250		$\Omega$

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## READ MODE

Unless otherwise specified IN+ and IN- are AC coupled, OUT+, and OUT- are loaded differentially with  $> 600\Omega$  and each side is loaded with  $< 10\text{ pF}$  to GND, a 2000 pF capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.

## AGC AMPLIFIER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Input Resistance	$V(\text{IN+} - \text{IN-}) = 100\text{ mVpp}$ @ 2.5 MHz		5K		$\Omega$
Differential Input Capacitance	$V(\text{IN+} - \text{IN-}) = 100\text{ mVpp}$ @ 2.5 MHz			10	pF
Common Mode Input Impedance (both sides)	R/W pin high		1.8		k $\Omega$
	R/W pin low		0.25		k $\Omega$
Minimum Gain Range	$1.0\text{ Vpp} \leq V(\text{OUT+} - \text{OUT-}) \leq 2.5\text{ Vpp}$	4.0		83	V/V
Input Noise Voltage	Gain set to maximum			30	nV/ $\sqrt{\text{Hz}}$
Bandwidth	Gain set to maximum -3 dB point	30			MHz
Maximum Output Voltage Swing	Set by AGC pin voltage	3.0			Vpp
Maximum AGC Amplifier Output Offset	Vout offset (max. gain) - Vout offset (min. gain) $V_{\text{BYP}} = 2.5\text{V to } 4.5\text{V}$			600	mV
OUT+ to OUT- Pin Current	No DC path to GND	$\pm 3.2$			mA
Output Resistance		12		32	$\Omega$
Output Capacitance				15	pF
(DIN+ - DIN-) Input Voltage Swing VS AGC Input Level	$30\text{ mVpp } V(\text{IN+} - \text{IN-}) \leq 550\text{ mVpp}$ $0.5\text{ Vpp} \leq V(\text{DIN+} - \text{DIN-}) \leq 1.5\text{ Vpp}$	0.37		0.56	Vpp/V
(DIN+ - DIN-) Input Voltage Swing Variation	$30\text{ mVpp } V(\text{IN+} - \text{IN-}) \leq 550\text{ mVpp}$ AGC Fixed, over supply & temperature			8	%
Gain Decay Time (Td)	$V_{\text{in}} = 300\text{ mVpp} \rightarrow 150\text{ mVpp}$ @ 2.5 MHz, Vout to 90% of final value Figure 1a		50		$\mu\text{s}$
Gain Attack time (Ta)	From Write to Read transition to Vout at 110% of final value $V_{\text{in}} = 400\text{ mVpp}$ @ 2.5 MHz. Figure 1b		4		$\mu\text{s}$

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## AGC AMPLIFIER (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Fast AGC Capacitor Charge Current	$V(DIN+ - DIN-) = 1.6V$ $V(AGC) = 2.2V$	1.3		2.0	mA
Slow AGC Capacitor Charge Current	$V(DIN+ - DIN-) = 1.6V$ Vary $V(AGC)$ until slow discharge	0.14		0.22	mA
Fast to Slow Attack Switchover Point	$V(DIN+ - DIN-)$ $V(DIN+ - DIN-) \text{ Final}$		1.25		
AGC Capacitor Discharge Current	$V(DIN+ - DIN-) = 0.0V$ Read Mode		4.5		$\mu A$
	Hold Mode $V_{BYP} = 5.0V$	-0.2		+0.2	$\mu A$
	$6.1V < V_{BYP} < 8.1V$	-0.45		+30	$\mu A$
CMRR (Input Referred)	$V(IN+) = V(IN-) = 100 \text{ mVpp}$ @ 5 MHz, gain at max.	40			dB
PSRR (Input Referred)	$\Delta VCC$ or $\Delta VDD = 100 \text{ mVpp}$ @ 5 MHz, gain at max.	30			dB

## HYSTERESIS COMPARATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	$V(DIN+ - DIN-) = 100 \text{ mVpp}$ @ 2.5 MHz	5		11	k $\Omega$
Differential Input Capacitance	$V(DIN+ - DIN-) = 100 \text{ mVpp}$ @ 2.5 MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		k $\Omega$
Comparator Offset Voltage	HYS pin at GND, $\leq 1.5 \text{ k}\Omega$ across DIN+, DIN-			10	mV
Peak Hysteresis Voltage vs. HYS pin voltage (input referred)	At DIN+, DIN- pins $1V < V(HYS) < 3V$	0.16		0.25	V/V
HYS Pin Input Current	$1V < V(HYS) < 3V$	0.0		-20	$\mu A$
Level Pin Output Voltage vs $V(DIN+ - DIN-)$	$0.6 <  V(DIN+ - DIN-) $ $< 1.3 \text{ Vpp}$ , 10 k $\Omega$ from LEVEL pin to GND	1.5		2.5	V/Vpp
LEVEL Pin Max Output Current		3.0			mA
LEVEL Pin Output Resistance	$I(LEVEL) = 0.5 \text{ mA}$		180		$\Omega$
DOUT Pin Output Low Voltage	$0.0 \leq IOL \leq 0.5 \text{ mA}$	VDD -4.0		VDD -2.8	V
DOUT Pin Output High Voltage	$0.0 \leq IOH \leq 0.5 \text{ mA}$	VDD -2.5		VDD -1.8	V

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## ACTIVE DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	V <sub>pp</sub>
Differential Input Resistance	V(CIN+ - CIN-) = 100 mV <sub>pp</sub> @ 2.5 MHz	5.8		11.0	kΩ
Differential Input Capacitance	V(CIN+ - CIN-) = 100 mV <sub>pp</sub> @ 2.5 MHz			6.0	pF
Common mode Input Impedance	(both sides)		2.0		kΩ
Voltage Gain From CIN± to DIF±	R(DIF+ to DIF-) = 2 kΩ	1.7		2.2	V/V
DIF+ to DIF- Pin Current	Differentiator Impedance must be set so as not to clip signal at this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- are AC Coupled			10.0	mV
CO <sub>UT</sub> Pin Output Low Voltage	0.0 ≤ IOH ≤ 0.5 mA		VDD - 3.0		V
CO <sub>UT</sub> Pin Output Pulse voltage V(high) - V(low)	0.0 ≤ IOH ≤ 0.5 mA		+0.4		V
CO <sub>UT</sub> Pin Output Pulse Width	0.0 ≤ IOH ≤ 0.5 mA		30		ns

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## OUTPUT DATA CHARACTERISTICS (See Figure 2)

Unless otherwise specified V(CIN+ - CIN-) = V(DIN+ - DIN-) = 1.0 V<sub>pp</sub> AC coupled since wave at 2.5 MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65 pF, V(Hys) = 1.8 DC, a 60 pF capacitor is connected between OS and VCC, RD- is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to GND.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
D-Flip-Flop Set Up Time (Td1)	Min delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ - DIF-) reaching a peak	0			ns
Propagation Delay (Td3)				110	ns
Output Data Pulse Width Variation	Td5 = 670 Cos, 50 pF ≤ Cos ≤ 200 pF			±15	%
Pulse Pairing	Td3 - Td4			3	ns
Output Rise Time	VOH = 2.4V			14	ns
Output Fall Time	VOL = 0.4V			18	ns

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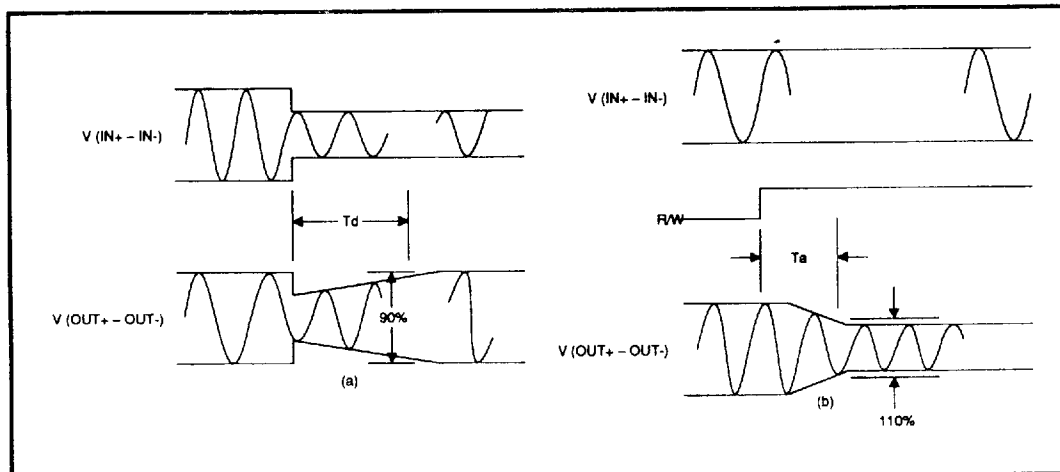


FIGURE 1(a), (b): AGC Timing Diagrams

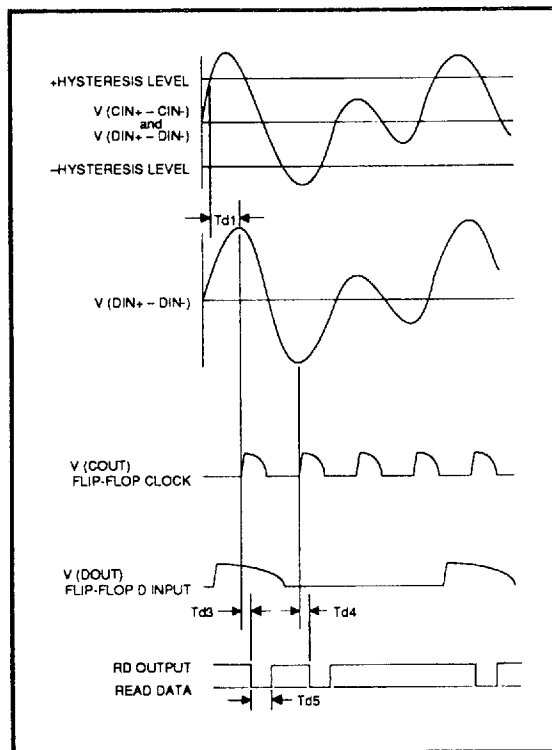


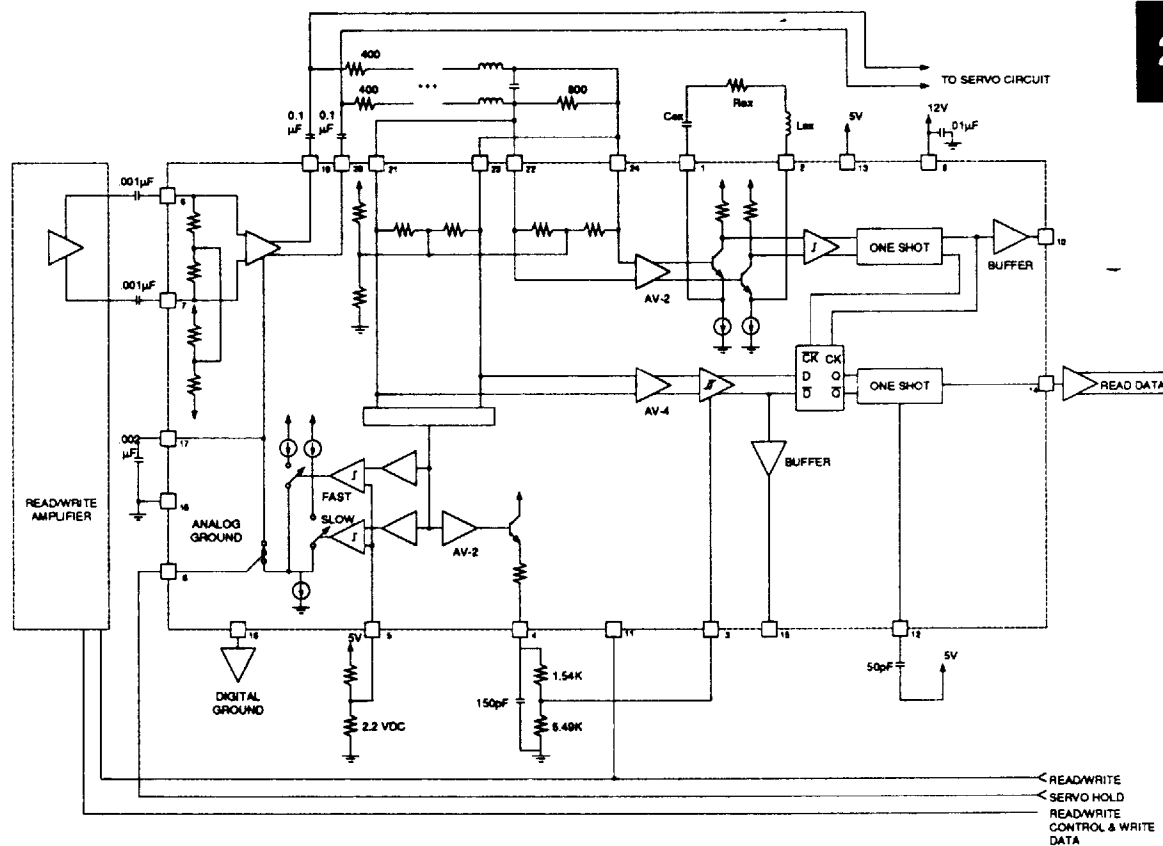
FIGURE 2: Timing Diagram

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NOTES: Circuit traces for the 12V bypass capacitor and the AGC Hold Capacitor should be as short as possible with both capacitors returned to the Analog Ground Pin.

Component values, where given, are for a 5 Mbit/s system.

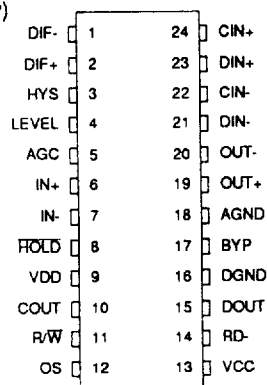
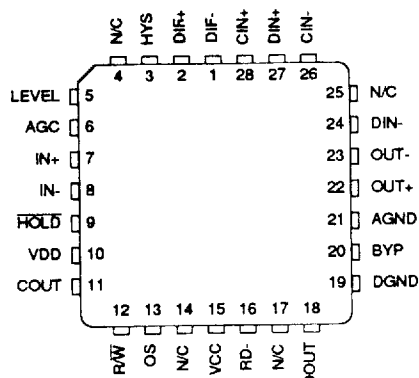
FIGURE 3: Typical Read/Write Electronics Set Up

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**PACKAGE PIN DESIGNATIONS**

(Top View)

**24-Lead PDIP, SOL****28-Lead PLCC****THERMAL CHARACTERISTICS:  $\theta_{ja}$** 

24-Lead PDIP	115°C/W
24-Lead SOL	80°C/W
28-Lead PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

**ORDERING INFORMATION**

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P541 Read Data Processor		
24-Lead PDIP	32P541-P	32P541-P
28-Lead PLCC	32P541-CH	32P541-CH
24-Lead SOL	32P541-CL	32P541-CL

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