SSI 32B451
SCSI Controller

July, 1990

DESCRIPTION

The SSI 32B451 SCSI bus interface device is designed to adapt a peripheral controller (target) system to a small computer system interface (SCSI) bus.

As a target adapter, the SSI 32B451 contains circuitry to complement the logic of the SSI 32C453 Dual Port Buffer Controller for SCSI arbitration; SCSI REQ/ACK handshake; and parity generation and checking. In its role as a target SCSI adapter, the circuitry on the device maximizes SCSI bus performance in all phases and ensures conformance with the SCSI specification.

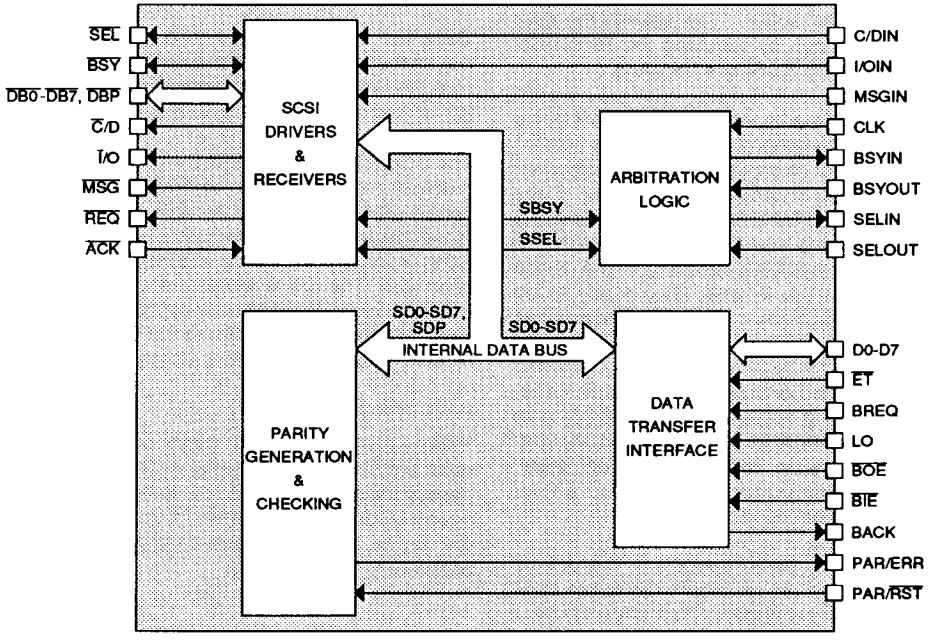
The SSI 32B451 includes high current drivers and Schmitt trigger receivers which allow for direct connection to the SCSI bus for the single ended interfacing option. The SSI 32B451 is intended for use in designs based around the SSI 32C452 storage controller and the SSI 32C453 Dual Port Buffer Controller.

FEATURES

- **Supports asynchronous data transfer up to 1.5 Mbytes/sec**
- **Supports target role in SCSI applications**
- **Includes high current drivers and Schmitt trigger receivers for direct connection to the SCSI bus**
- **Full hardware compliance to ANSI X3T9.2 Rev. 17B specification as a target peripheral adapter**
- **Contains circuitry to support SCSI arbitration, (re)selection and parity features**
- **Complements the SSI 32C453 Buffer controller**
- **Plug compatible with AIC 500L**
- **Available in 44 pin PLCC**
- **Single +5V supply**

7

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The purpose of the SSI 32B451 is to fulfill a support role within a hardware design. The device contains four circuit functions which interact within the overall design. The partial schematic in Figure 10 illustrates this interaction. This section describes each of the functional circuits.

DATA TRANSFER INTERFACE

The data transfer interface logic coordinates the transfer of data between the data transfer logic and the SCSI bus. Standard two-wire DMA handshaking is supported by the BREQ and BACK signals. This section is organized to connect directly with the SSI 32C453, Dual Port Buffer Controller, but is easily connected to any other data transfer control device. Before DMA controlled information transfer can begin, a valid connection must exist to the SCSI bus with BSY active and no phase error. The direction of information flow is controlled by the I/O In signal from the storage controller or a latch.

The device complements the buffer controller handshake timing by latching the SCSI data before transferring into the controller buffer. This speeds the data transfer across the bus by reducing the $\overline{REQ}/\overline{ACK}$ timing restraints for the SCSI bus transfers.

In the target-in state (read operation), the data is being transferred from the peripheral controller to the initiator or the host. The buffer controller device controls when the buffer is accessed to pass on to the device. Once valid data is present on D0-D7 of the buffer data, LO is asserted, latching data into the device. The buffer controller then asserts BREQ, indicating to the device that valid data is in the internal latch ready to be transferred over the SCSI bus. The device then places data on the SCSI bus and then asserts $\overline{REQ}$. The data setup time required by SCSI specification is dictated primarily by the buffer controller. The host (initiator) asserts $\overline{ACK}$ indicating acceptance of the SCSI data transfer cycle. The device asserts BACK to the buffer controller logic indicating completion of that cycle. Refer to Read Operation timing diagram (Figure 4) for an illustration of this handshake.

In the target-out state (write operation), the data is being transferred from the initiator to the buffer upon the control of the buffer controller. The buffer controller asserts BREQ requesting transfer of a byte of data from the initiator. The device, in turn, asserts $\overline{REQ}$ and the initiator responds by driving the SCSI data bus and asserting $\overline{ACK}$ which latches data into the device. BACK is asserted by the device indicating that the byte is latched inside the device and is available to be transferred to the buffer RAM. The buffer controller then asserts $\overline{BIE}$ to enable output of the data to the RAM. When the buffer controller has completed transferring the data it negates $\overline{BIE}$ and BREQ indicating to the device that the cycle is complete. Refer to Write Operation timing diagram (Figure 3) for an illustration of this handshake.

ARBITRATION

The purpose of this block is to complement the logic in the SSI 32C453, buffer controller device, for SCSI bus arbitration during selection of the target controller or reselection of the initiator phases. The device simply passes along the $\overline{SEL}$ and $\overline{BSY}$ signals as SEL IN and BSY IN, respectively. It also monitors the control line BSYOUT received from the buffer controller chip for a minimum of three clock periods and a maximum of four clock periods (Bus-Free Delay) after which time it outputs $\overline{BSY}$.

Once the device has performed these functions it leaves the actual arbitration activity to the local microcontroller and the buffer controller. Refer to the SSI 32C453 specification for details of this activity.

The SCSI signals $\overline{SEL}$, SELOUT, $\overline{BSY}$ and BSYOUT received from the buffer controller are internally inverted and become SELIN, $\overline{SEL}$, BSYIN and $\overline{BSY}$, respectively. The actual monitoring of these lines for SCSI timing specification is accomplished by the buffer controller. The actual arbitration activity for the SCSI bus is performed by the buffer controller device and the local microcontroller. Refer to the SSI 32C453 specification for the timing of this activity.

PARITY GENERATION

Parity functions as 'Odd' parity only. For incoming data, the SSI 32B451 checks parity or computes and passes the computed bit to the buffer RAM depending upon the condition of PAR/$\overline{RST}$ line. For outgoing data, the device always computes parity on the data and presents to the SCSI bus.

For the incoming SCSI data, the device generates parity internally and compares it against the parity bit received if the PAR/$\overline{RST}$ line is high. The result of this comparison is latched at the PAR/ERR output signal. An error is indicated by a high signal at this output. To clear the error condition, the PAR/$\overline{RST}$ line must be driven to a low level.

Alternatively, if PAR/$\overline{RST}$ is held low, the device computes parity on incoming SCSI data and presents this parity bit at the PAR/ERR output. This value can be stored in the buffer RAM for parity checking at a later time.

For outgoing data, parity is always generated and presented for the SCSI bus on the $\overline{DBP}$ line by the device.

NOTE: Parity, as a function of SCSI, is optional. However, the SSI 32B451 ignores this and works parity continuously. The surrounding design has responsibility of either monitoring parity or ignoring it.

SCSI INTERFACE

Drivers and receivers are provided internally to the SSI 32B451 for direct connection to the SCSI bus. The only components necessary outside of the chip are the pull-up and pull-down resistors for the interface and receivers for SCSI Attention and Reset signals. The data and parity signals received from the SCSI bus are passed along to the Data Transfer Interface and parity circuits described above. The data and parity bits to be sent over to the SCSI bus are buffered by this circuit.

PIN DESCRIPTION

This section describes the names of pins, their symbols, their functions and their active states. The signals are grouped in four categories according to their interface to other components on the board. The four categories area:

* SCSI Bus Interface
* Buffer Controller/Buffer RAM Interface
* Storage Controller Interface
* Others

SCSI BUS INTERFACE

The following group of signals interface directly to the SCSI bus. All output and bi-directional lines have 48 mA sinking current capability. All input buffers are Schmitt trigger inputs and all outputs have high current open drain buffers to allow direct connection to the SCSI bus.

NAME	PIN #	TYPE	I/O	DESCRIPTION
$\overline{DB0}$-$\overline{DB7}$	13-17 19-21	SCSI	I/O	Data Bus. Buffered data bus signals interface directly to SCSI bus.
$\overline{DBP}$	10	SCSI	I/O	Data Bus Parity. Parity bit for the SCSI data bus signals. It is always generated when data is transferred on the SCSI bus. It can be ignored on reception. Active low.
$\overline{ACK}$	7	SCSI	I	Acknowledge. This signal is an input from the initiator in response to the SSI 32B451's $\overline{REQ}$, and indicates valid data on the SCSI bus. Active low.
$\overline{SEL}$	23	SCSI	I/O	Select. Active low signal used by an initiator (the host) to select a target or by a target to reselect an initiator.

SCSI BUS INTERFACE (Continued)

NAME	PIN #	TYPE	I/O	DESCRIPTION
$\overline{BSY}$	25	SCSI	I/O	Busy. Active low. An "OR-tied" signal that indicates the bus is being used.
$\overline{MSG}$	11	SCSI	O	Message. Open drain SCSI signal. Signal driven by the device to indicate that the SCSI communication is in the message phase. Active low.
$\overline{C}$/D	27	SCSI	O	Command/Data. Open drain SCSI signal driven by the device that indicates control or data information is on the data bus.
$\overline{REQ}$	22	SCSI	O	Request. Active low true signal driven to request data byte transfers. Also, used to "Acknowledge" at completion of transfer.
$\overline{I}$/O	26	SCSI	O	Input/Output. SCSI signal that controls the direction of data movement on the SCSI bus with respect to the initiator.

BUFFER CONTROLLER/BUFFER RAM INTERFACE
The following group of signals are associated with buffer data and control. All signals except the buffer data signals interface to the SSI 32C453, Dual Port Buffer Controller.

NAME	PIN #	TYPE	I/O	DESCRIPTION
BREQ	35	TTL	I	Buffer Request. When asserted, this signal indicates that the peripheral buffer controller is requesting to transfer a byte of data. Active high input.
BACK	6	TTL	O	Buffer Acknowledge. When asserted this signal indicates acceptance of data transfer. Active high output.
LO	38	TTL	I	Latch Out. Latches data into the device to be presented to the SCSI bus. Active high.
$\overline{BIE}$	39	TTL	I	Bus In Enable. Active low. A strobe from the data transfer control logic which indicates it is transferring data from the SCSI bus to the local buffer.
$\overline{BOE}$	5	TTL	I	Bus Out Enable. Active low. A strobe from the data transfer control logic which indicates it is transferring data from the local buffer to the SCSI bus.
$\overline{ET}$	8	TTL	I	Target Enable. Active low. A signal connected to the SSI 32C453. When this signal is active it provides microcode and hardware control to enable all drivers except Busy on the SCSI bus.

BUFFER CONTROLLER/BUFFER RAM INTERFACE (Continued)

NAME	PIN #	TYPE	I/O	DESCRIPTION
SEL IN	29	TTL	O	Select In. Active high. Used to pass the select line from the SCSI bus to the buffer controller.
SEL OUT	28	TTL	I	Select Out. Active high. Used as an input from the buffer controller to indicate when to drive the select line on the SCSI bus.
BSY IN	31	TTL	O	Busy In. Active high. Used to pass busy from the SCSI bus to the buffer controller. Indicates other devices are actively accessing the bus.
BSY OUT	32	TTL	I	Busy Out. Active high. Used as an input from the buffer controller to indicate when to drive the busy line on the SCSI bus.
D0-D7	2-4 40-44	TTL	I/O	Buffer Data. These lines connect to buffer RAM data pins.

STORAGE CONTROLLER INTERFACE

The following group of pins interface with the SSI 32C452, Storage Controller. These lines may also be connected to an output port of a microcontroller or a latch.

NAME	PIN #	TYPE	I/O	DESCRIPTION
MSG IN	9	TTL	I	Message In. Active high signal from the storage controller drives the SCSI $\overline{MSG}$ signal low.
I/O IN	33	TTL	I	I/O In. A high signal from the storage controller drives the SCSI $\overline{I}$/O signal low.
C/D IN	30	TTL	I	C/D In. A high signal from the storage controller drives the SCSI $\overline{C}$/D signal low.

OTHERS

The following group of lines are the miscellaneous signals.

NAME	PIN #	TYPE	I/O	DESCRIPTION
CLK	34	TTL	I	Clock. Used for clock input between 2.5 MHz and 5 MHz. This signal is used internally during the arbitration phase only.
PAR/ERR	37	TTL	O	Parity/Error. Logic 1 indicates a parity error detected on the SCSI bus when PAR/$\overline{RST}$ is held high. When the PAR/$\overline{RST}$ line is held low, parity will be passed to the controller buffer by using the PAR/ERR line as the parity bit for each byte.

OTHERS (Continued)

NAME	PIN #	TYPE	I/O	DESCRIPTION
PAR/$\overline{RST}$	36	TTL	I	Parity/Reset. When held high, the device checks SCSI bus parity error by setting logic 1 (high) on the PAR/ERR pin. When held low, parity is passed through the device to the controller buffer with the PAR/ERR line being the parity bit.
GND	12, 18, 24			Ground. Device system ground.
VCC	1			Power Supply. +5V input for power to the device.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.)

PARAMETER	RATING	UNIT
VCC with respect to VSS (GND)	+7	V
Max. voltage on any pin with respect to VSS	-0.5 to +7	V
Operating temperature	0 to 70	°C
Storage temperature	-55 to +125	°C

DC OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, VCC = +5V ± 5%, VSS = 0V)

PARAMETER		CONDITION	MIN	MAX	UNITS
IIL	Input Leakage ($\overline{BREQ}$, LO, $\overline{BOE}$, $\overline{BIE}$, $\overline{ET}$ $\overline{SELOUT}$, BSYOUT, CDIN, I/OIN, $\overline{MSGIN}$, PAR/$\overline{RST}$, CLK, $\overline{ACK}$)	0 < Vin < VCC	-10	+10	µA
IOL	SCSI Output Leakage ($\overline{SEL}$, $\overline{BSY}$, $\overline{DB0}$-$\overline{DB7}$, $\overline{DBP}$, $\overline{MSG}$, $\overline{C/D}$, $\overline{I/O}$)	0.5 < Vout < VCC	-50	+50	µA
IOL	D0-D7	0.45 < Vout < VCC	-10	+10	µA
VIL	Input Low Voltage		0	0.8	V

DC OPERATING CHARACTERISTICS (Continued)

PARAMETER		CONDITION	MIN	MAX	UNITS
VIH	Input High Voltage		2.0		V
VOH	Output High Voltage	IOH = -400 µA	2.4		V
VOL	SCSI Output Low Voltage	IOL = 48 mA		0.5	V
VOL	All others	IOL = 2 mA		0.4	V
	Power Dissipation			500	mW
Vhsy	Hysteresis Voltage (all SCSI signals)		200		mV
Iccs	Standby Current	Ta = 70°C		600	µA
Icc	Supply Current	Ta = 70°C		30	mA
Cin	Input Capacitance			15	pF

AC CHARACTERISTICS

The following sections list the timing characteristics necessary for the proper operation of the device. Unless otherwise specified, all timing parameters pertain to input clock frequency (2.5 MHz min. to 5.0 MHz max.).

7

Note: AC timing is measured at Voh = 2.0V, Vol = 0.8V, Cin = 50 pF. Timing characteristics are valid over the entire operating temperature, 0 to 70°C, and voltage range, 4.75 to 5.25 volts.

CLOCK AND PARITY TIMING (See Figures 1 & 2)

SYMBOL	PARAMETER	MIN	MAX	UNITS
TICLK/2	Input Clock Half-Cycle	100	200	ns
TICLK	Input Clock Width	200	400	ns
DPV	Data Valid to Parity Detect		100	ns

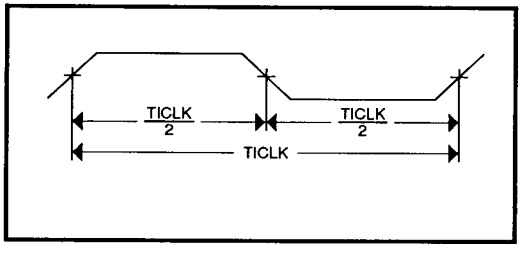


FIGURE 1: Input Clock Timing

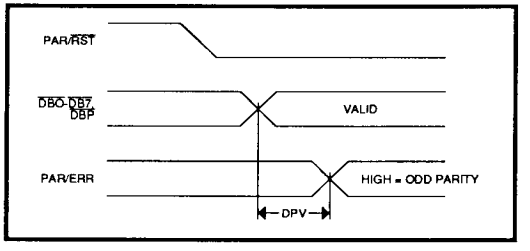
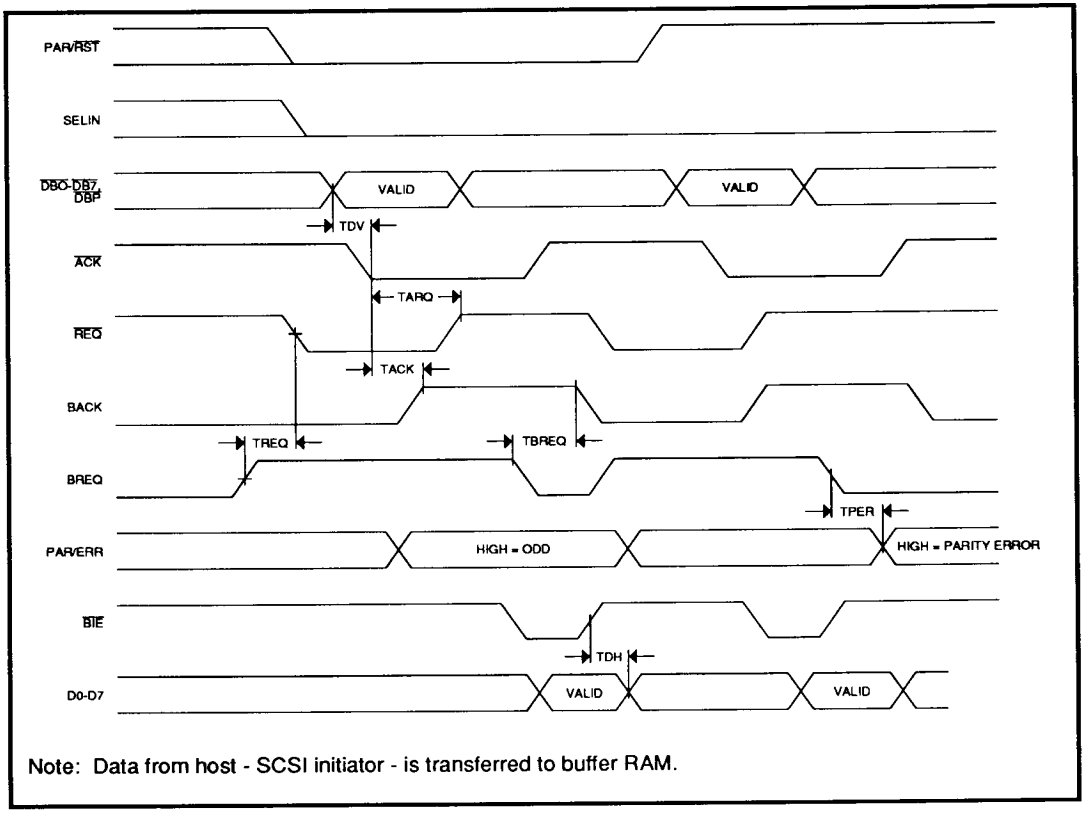


FIGURE 2: SCSI Bus Parity Timing

WRITE OPERATION TIMING (See Figure 3)

SYMBOL	PARAMETER	MIN	MAX	UNITS
TREQ	BREQ ↑ to $\overline{REQ}$ ↓		21	ns
TARQ	$\overline{ACK}$ ↓ to $\overline{REQ}$ ↑		55	ns
TACK	$\overline{ACK}$ ↓ to BACK ↑		50	ns
TBREQ	BREQ ↓ to BACK ↓		25	ns
TDH	$\overline{BIE}$ ↑ to Data Invalid		40	ns
TDV	SCSI Data Valid to $\overline{ACK}$ ↓	55		ns
TPER	BREQ ↓ to Parity Error Valid		45	ns

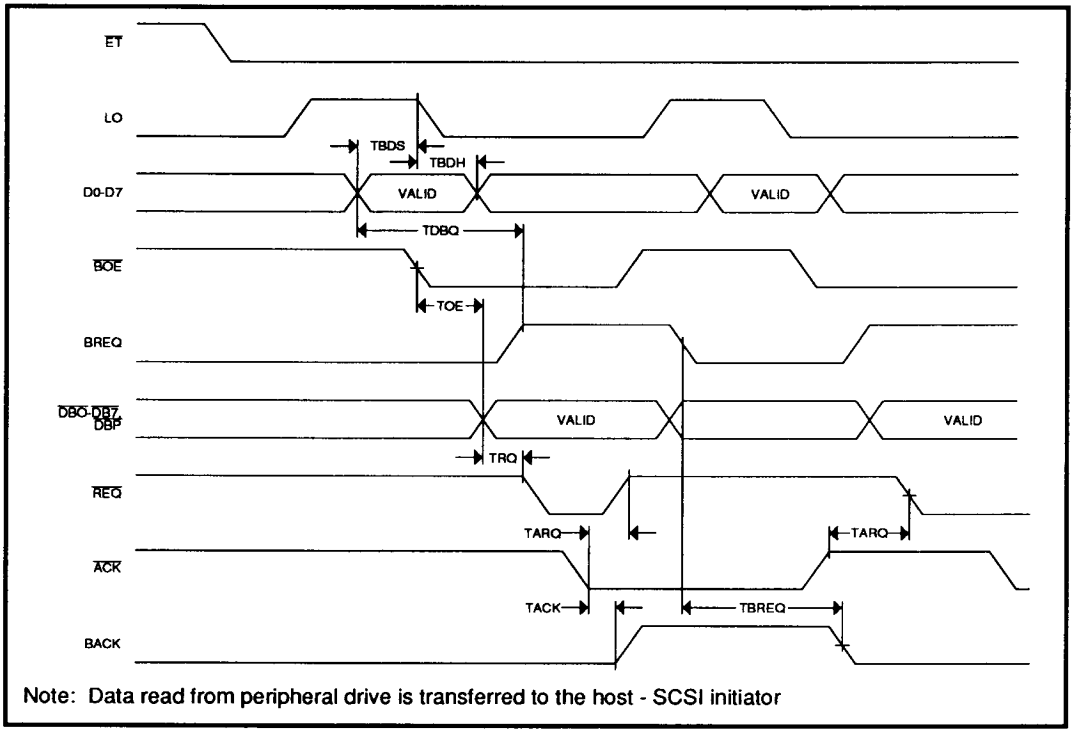


Note: Data from host - SCSI initiator - is transferred to buffer RAM.

FIGURE 3: Write Operation Timing

READ OPERATION TIMING (See Figure 4)

SYMBOL	PARAMETER	MIN	MAX	UNITS
TBDS	Buffer Data Valid to LO ↓	0		ns
TBDH	LO ↓ to Buffer Data Invalid	25		ns
TDBQ	Buffer Data Valid to BREQ ↑	90		ns
TRQ	SCSI Bus Data Valid to $\overline{REQ}$ ↓	55		ns
TARQ	$\overline{ACK}$ ↓ to $\overline{REQ}$ ↑		55	ns
TACK	$\overline{ACK}$ ↓ to BACK ↑		55	ns
TARQ	$\overline{ACK}$ ↑ to $\overline{REQ}$ ↓		55	ns
TBREQ	BREQ ↓ to BACK ↓		25	ns
TOE	$\overline{BOE}$ to SCSI Data Valid		35	ns



Note: Data read from peripheral drive is transferred to the host - SCSI initiator

FIGURE 4: Read Operation Timing

ARBITRATION AND CONTROL SIGNAL TIMING (See Figures 5 & 6)

SYMBOL	PARAMETER	MIN	MAX	UNITS
TSELO	SELOUT ↑ or ↓ to $\overline{SEL}$ ↓ or ↑		35	ns
TBOT	BSYOUT ↑ or ↓ to $\overline{BSY}$ ↓ or ↑	3 x TICLK	4 x TICLK + 40	ns
TCNT	MSGIN, I/OIN, CDIN to $\overline{MSG}$, $\overline{I}$/O, $\overline{C}$/D		35	ns

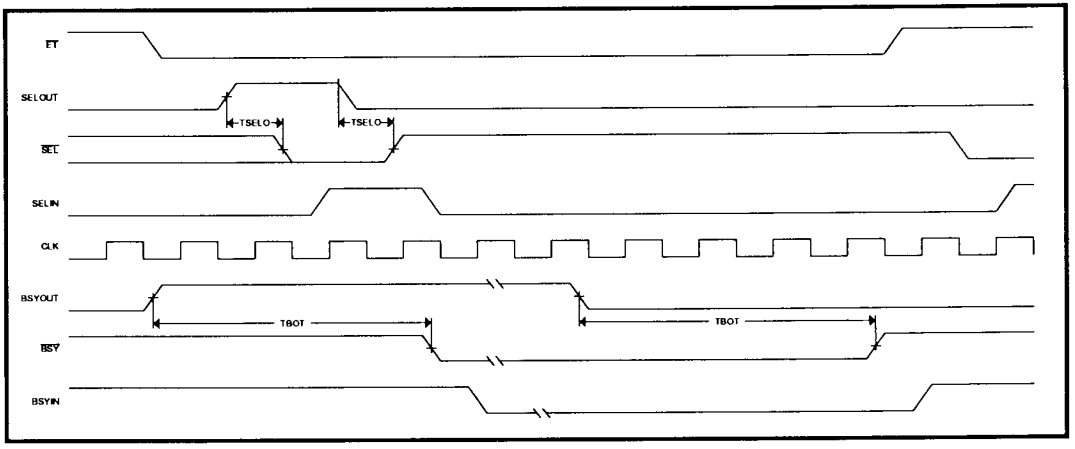


FIGURE 5: Arbitration Signals Timing

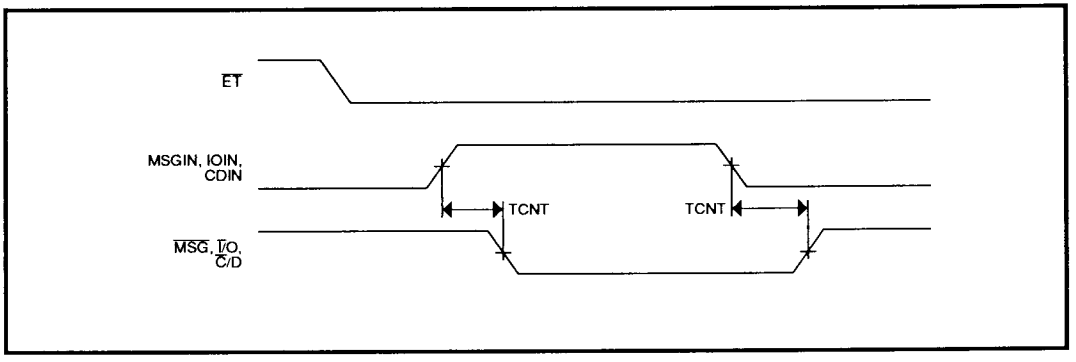


FIGURE 6: SCSI Control Signal Timing

APPLICATION NOTES

The SSI 32B451 supports the SSI 32C453 and the local microprocessor in performing all the SCSI target controller functions. For successful SCSI bus operation, the target controller must follow all the requirements of the SCSI protocol defined by ANSI specification X3T9.2 Rev. 17B. An overview of a typical SCSI signal sequence is shown in Figure 7.

Before any SCSI operations can begin, the local microprocessor polls the $\overline{BSY}$ line through the SSI 32C453 (BSYIN signal). When this signal is asserted, the microprocessor checks the arbitration I.D. asserted by the initiator.

Following the Arbitration phase, the SCSI bus enters the Selection phase. SSI 32B451 assists the Arbitration and Selection phases by passing the two control signals, BSY and SEL, and the SCSI I.D. to the SSI 32C453 and the local buffer, respectively. Other phases following Arbitration and Selection are command, data in, data out, status, message in and message out. Table 1 shows the various phases and their sources.

Table 2 shows the various control signal status during different SCSI phases. Being a target device, the SSI 32B451 drives these control lines out on the SCSI bus.

The SSI 32B451 requires local microprocessor supervision for successful operation over the SCSI bus. Firmware support for the local microprocessor consists of various routines. Flow charts for these routines are shown in Figures 8 and 9.

SCSI SPECIFIC INFORMATION

This information from the ANSI Standard for the Small Systems Computer Interface is provided to assist in implementing a SCSI based controller with the SSI 32B451.

TABLE 1: Bus Phase Signal Sources

BUS PHASE	SIGNALS				
	$\overline{BSY}$	$\overline{SEL}$	$\overline{C/D}$, $\overline{I/O}$, $\overline{MSG}$, REQ	ACK/ATN	DB7-DB0
Bus Free	None	None	None	None	None
Arbitration	All	Winner	None	None	SCSI ID
Selection	I & T	Initiator	None	Initiator	Initiator
Reselection	I & T	Target	Target	Initiator	Target
Command	Target	None	Target	Initiator	Initiator
Data In Target	Target	None	Target	Initiator	Target
Data Out	Target	None	Target	Initiator	Initiator
Status Target	Target	None	Target	Initiator	Target
Message In	Target	None	Target	Initiator	Target
Message	Target	None	Target	Initiator	Initiator

DEFINITIONS FOR TABLE 1

All: The signal is driven by all SCSI devices which are actively arbitrating.

SCSI ID: The SCSI ID is a unique data bit (DB) for each of the SCSI devices in the system and is driven onto the SCSI bus by each device that is actively arbitrating. The other seven data bits shall not be driven by the SCSI device. The parity bit may be asserted or undriven during arbitration but can't be driven false.

I & T: This signal is driven by the initiator, target or both as specified in the selection or reselection phase.

Initiator: If this signal is driven it can be driven only by the active initiator.

None: The signal is released meaning it is not driven by any SCSI device.

Winner: The signal shall be driven by the one SCSI device that wins arbitration.

Target: If the signal is driven it can be driven only by the active target.

TABLE 2: Signal Status, Information Transfer Phases

SIGNALS			PHASE NAME	DIRECTION OF TRANSFER
$\overline{MSG}$	$\overline{C}$/D,	$\overline{I}$/O		
1	1	1	Data Out	Initiator to Target
1	1	0	Data In	Initiator from Target
1	0	1	Command	Initiator to Target
1	0	0	Status	Initiator from Target
0	1	1	#	
0	1	0	#	
0	0	1	Message Out	Initiator to Target
0	0	0	Message In	Initiator from Target
# = Reserved for future standardization				

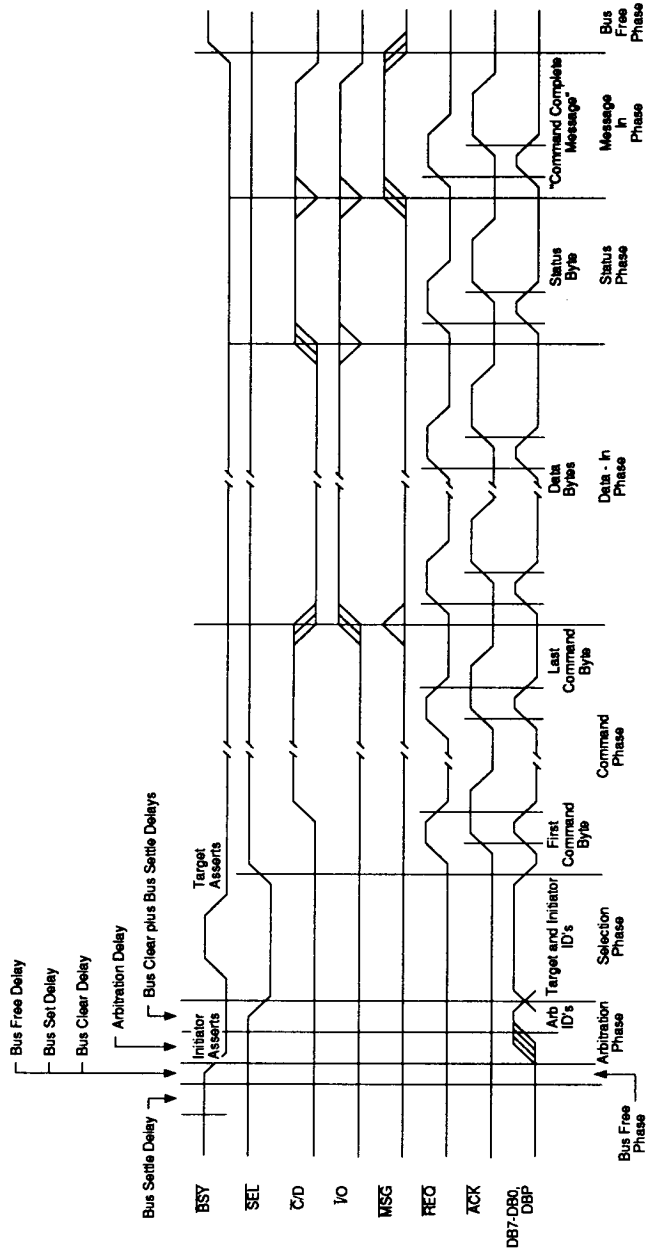


FIGURE 7: SCSI Signal Sequence Example

7

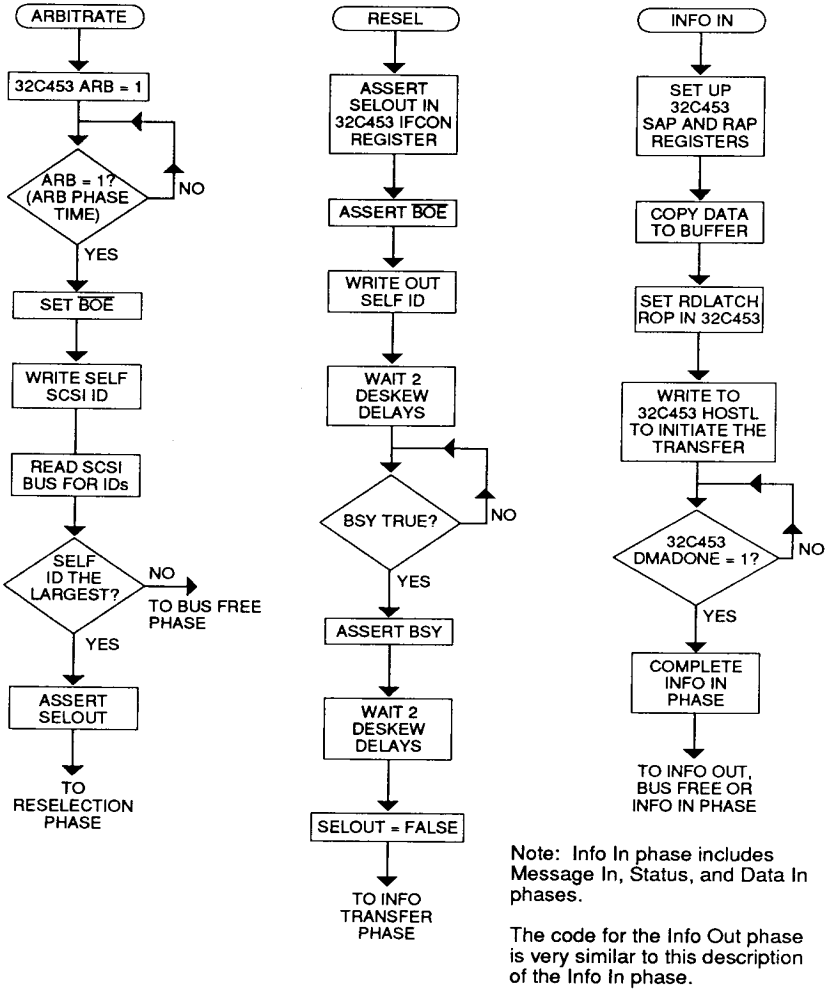


FIGURE 8: Flow Charts for Various SSI 32B451 Routines

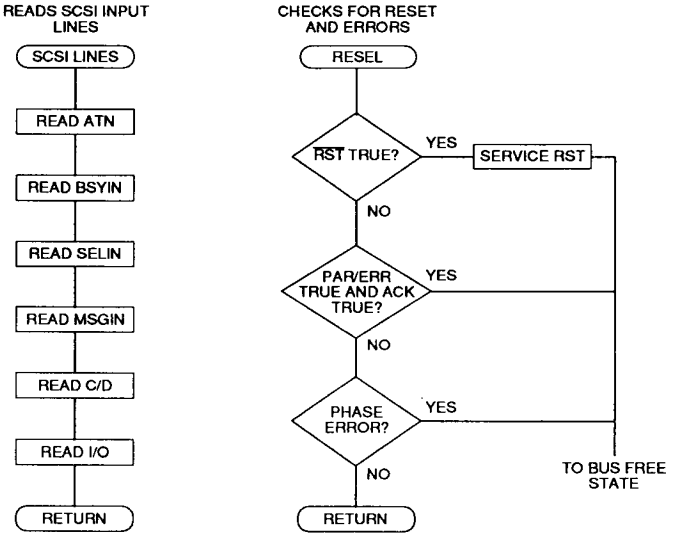


FIGURE 9: SCSI Background Routines Using SSI 32B451

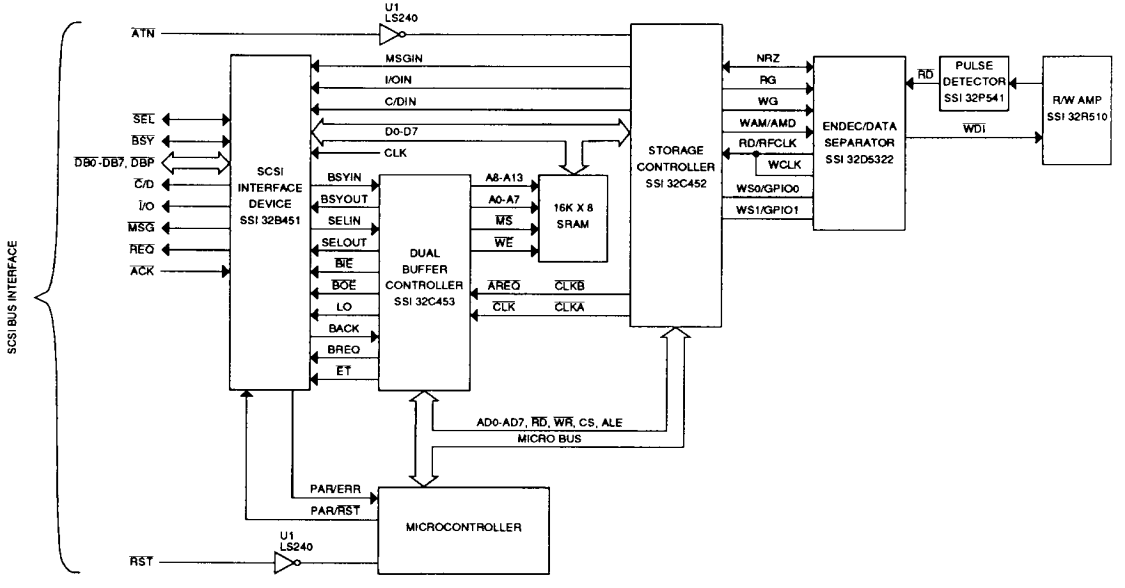
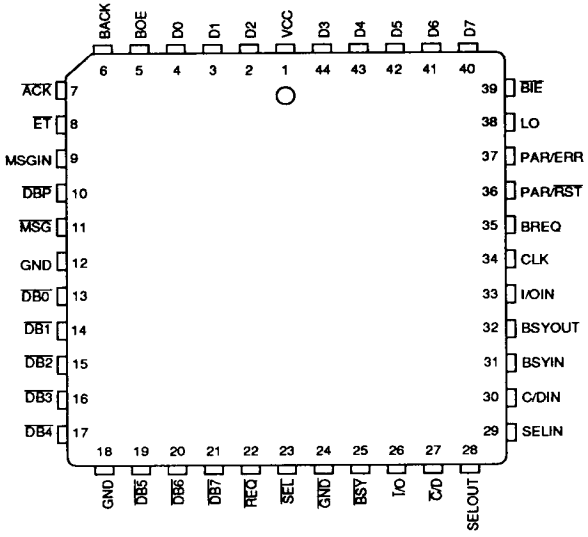


FIGURE 10: Partial Schematic for SCSI Implementation with Arbitration Support Using SSI Devices

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32B451 44-pin PLCC	SSI 32B451-CH	32B451-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457