PLESSEY
SEMICONDUCTORS

T-73-31

PDSP16318/PDSP16318A
COMPLEX ACCUMULATOR

The PDSP16318 contains two independent 20-bit Adder/Subtractors combined with accumulator registers and shift structures. The four port architecture permits full 20MHz throughput in FFT and filter applications.

Two PDSP16318As combined with a single PDSP16112A Complex Multiplier provide a complete arithmetic solution for a Radix 2 DIT FFT Butterfly. A new complex Butterfly result can be generated every 50ns allowing 1K complex FFT's to be executed in 256μs.

The PDSP16318/A is recommended for new designs instead of PDSP16316/A.

FEATURES

- Full 20MHz Throughput in FFT Applications
- Four Independent 16-bit I/O Ports
- 20-bit Addition or Accumulation
- Fully Compatible with PDSP16112 Complex Multiplier
- On Chip Shift Structures for Result Scaling
- Overflow Detection
- Independent Three-State Outputs and Clock Enables for 2 Port 20MHz Operation
- 1.4 micron CMOS
- 500mW Maximum Power Dissipation
- 84 Pin PGA Package

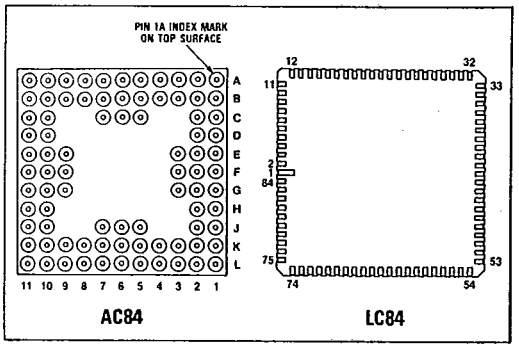

Fig.1 Pin connections - bottom view

APPLICATIONS

- High Speed Complex FFT or DFTs
- Complex Finite Impulse Response (FIR) Filtering
- Complex Conjugation
- Complex Correlation/Convolution

ASSOCIATED PRODUCTS

PDSP16112	16×12 Complex Multiplier
PDSP16116	16×16 Complex Multiplier
PDSP1601	ALU and Barrel Shifter
PDSP1640	20MHz Address Generator
PDSP16330	Pythagoras Processor

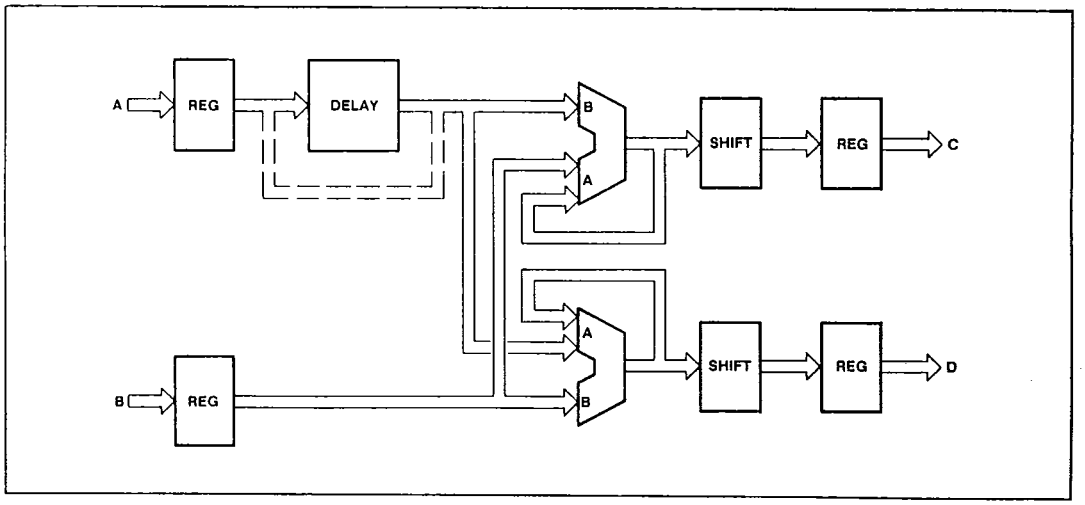

Fig.2 PDSP16318 simplified block diagram

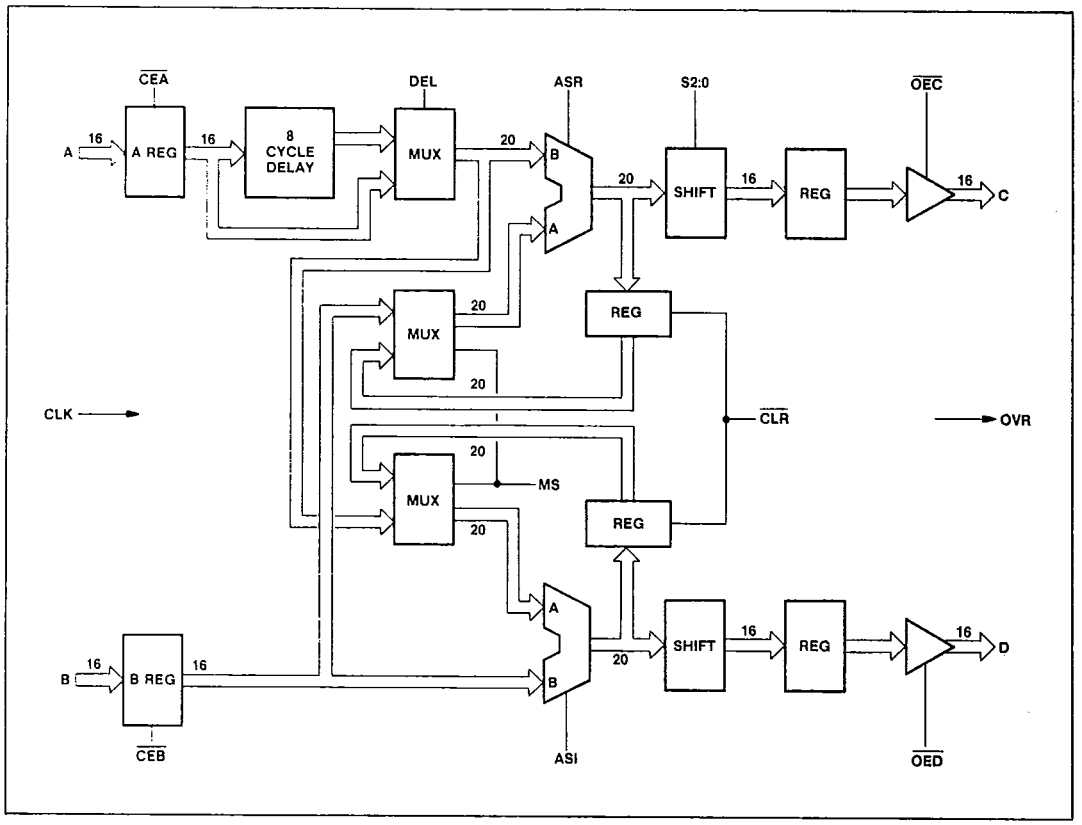

Fig.3 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16318 is a Dual 20-bit Adder/Subtractor configured to support Complex Arithmetic. The device may be used with each of the adders allocated to real or imaginary data (e.g. Complex Conjugation), the entire device allocated to Real or Imaginary Data (e.g. Radix 2 Butterflys) or each of the adders configured as accumulators and allocated to real or imaginary data (Complex Filters). Each of these modes ensures that a full 20MHz throughput is maintained through both adders, the first and last mode illustrating true Complex operation, where both real and imaginary data is handled by the single device.

Both Adder/Subtractors may be controlled independently via the ASR and ASI inputs. These controls permit A + B, A - B, B - A or pass A operations, where the A input to the Adder is derived from the input multiplexer. The $\overline{CLR}$ control line allows the clearing of both accumulator registers.The two multiplexers may be controlled via the MS inputs, to select either new input data, or fed-back data from the accumulator registers. The PDSP16318 contains an 8-cycle deskew register selected via the DEL control. This deskew register is used in FFT applications to ensure correct phasing of data that has not passed through the PDSP16112 Complex Multiplier.

The 16-bit outputs from the PDSP16318 are derived from the 20-bit result generated by the Adders. The three bit S2:0 input selects eight different shifted output formats ranging from the most significant 16 bits of the 20-bit data, to the least significant 13 bits of the 20-bit data. In this mode the 14th, 15th and 16th bits of the output are set to zero. The shift selected is applied to both adder outputs, and determines the function of the OVR flag. The OVR flag becomes active when either of the two adders produces a result that has more significant digits than the MSB of the 16-bit output from the device. In this manner all cases when invalid data appears on the output are flagged.

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PIN DESCRIPTIONS

Symbol	Type	Description
A15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. A15 is the MSB.
B15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. B15 is the MSB and has the same weighting as A15.
C15:0	Output	New **data** appears on this output after the rising edge of CLK. C15 is the MSB.
D15:0	Output	New **data** appears on this output after the rising edge of CLK. D15 is the MSB.
CLK	Input	**Common Clock** to all internal registers
$\overline{CEA}$	Input	**Clock enable:** when low the clock to the A input register is enabled.
$\overline{CEB}$	Input	**Clock enable:** when low the clock to the B input register is enabled.
$\overline{OEC}$	Input	**Output enable:** Asynchronous 3-state output control: The C outputs are in a high impedance state when this input is high.
$\overline{OED}$	Input	**Output enable:** Asynchronous 3-state output control: The D outputs are in a high impedance state when this input is high.
OVR	Output	**Overflow flag:** This flag will go high in any cycle during which either the output data overflows the number range selected or either of the adder results overflow. A new OVR appears after the rising edge of the CLK.
ASR1:0	Input	**Add/subtract Real:** Control input for the 'Real' adder. This input is latched by the rising edge of clock.
ASI1:0	Input	**Add/subtract Imag:** Control input for the 'Imag' adder. This input is latched by the rising edge of clock.
$\overline{CLR}$	Input	**Accumulator Clear:** Common accumulator clear for both Adder/Subtractor units. This input is latched by the rising edge of CLK.
MS	Input	**Mux select:** Control input for both adder multiplexers. This input is latched by the rising edge of CLK. When high the feedback path is selected.
S2:0	Input	**Scaling control:** This input selects the 16-bit field from the 20-bit adder result that is routed to the outputs. This input is latched by the rising edge of CLK.
DEL	Input	**Delay Control:** This input selects the delayed input to the real adder for operations involving the PDSP16112. This input is latched by the rising edge of CLK.
VCC	Power	**+5V supply:** Both Vcc pins must be connected.
GND	Ground	**0V supply:** Both GND pins must be connected.

LC Pin	AC Pin	Function	LC Pin	AC Pin	Function	LC Pin	AC Pin	Function	LC Pin	AC Pin	Function
75	B2	D7	12	K2	C7	33	K10	A1	54	B10	B10
76	C2	D8	13	K3	C6	34	J10	A2	55	B9	B9
77	B1	D9	14	L2	C5	35	K11	A3	56	A10	B8
78	C1	D10	15	L3	C4	36	J11	A4	57	A9	B7
79	D2	GND	16	K4	C3	37	H10	A5	58	B8	B6
80	D1	VCC	17	L4	C2	38	H11	A6	59	A8	B5
81	E3	D11	18	J5	C1	39	F10	A7	60	B6	B4
82	E2	D12	19	K5	$\overline{C0}$	40	G10	A8	61	B7	B3
83	E1	D13	20	L5	$\overline{OED}$	41	G11	A9	62	A7	B2
84	F2	D14	21	K6	$\overline{OEC}$	42	G9	A10	63	C7	B1
1	F3	D15	22	J6	S2	43	F9	A11	64	C6	B0
2	G3	C15	23	J7	S1	44	F11	A12	65	A6	$\overline{CLK}$
3	G1	C14	24	L7	S0	45	E11	A13	66	A5	$\overline{CEB}$
4	G2	C13	25	K7	MS	46	E10	A14	67	B5	OVR
5	F1	C12	26	L6	ASI1	47	E9	$\overline{A15}$	68	C5	D0
6	H1	VCC	27	L8	ASI0	48	D11	$\overline{CEA}$	69	A4	D1
7	H2	GND	28	K8	$\overline{DEL}$	49	D10	B15	70	B4	D2
8	J1	C11	29	L9	$\overline{CLR}$	50	C11	B14	71	A3	D3
9	K1	C10	30	L10	ASR1	51	B11	B13	72	A2	D4
10	J2	C9	31	K9	ASR0	52	C10	B12	73	B3	D5
11	L1	C8	32	L11	A0	53	A11	B11	74	A1	D6

ASR or ASI ASX1	ASR or ASI ASX0	ALU Function
0	0	A + B
0	1	A
1	0	A - B
1	1	B - A

DEL	Delay Mux Control
0	A port input
1	Delayed A port input

MS	Real and Imag' Mux Control
0	B port input/Del mux output
1	C accumulator/D accumulator

S2:0			Adder result																			
S2	S1	S0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
0	0	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
0	1	0			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	1	1				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	0					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1						15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	1	0							15	14	13	12	11	10	9	8	7	6	5	4	3	2
1	1	1								15	14	13	12	11	10	9	8	7	6	5	4	3

NOTE
This table shows the portion of the adder result passed to the D15:0 and C15:0 outputs. Where fewer than 16 adder bits are selected, the output data is padded with zeros.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN}	-0.9V to Vcc +0.9V
Output voltage V_{OUT}	-0.9V to Vcc +0.9V
Clamp diode current per pin I_K (see Note 2)	18mA
Static discharge voltage (HMB) V_{STAT}	500V
Storage temperature range T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Junction temperature	150°C
Package power dissipation P_{TOT}	1000mW

NOTES
1 Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2 Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3 Exposure to absolute maximum ratings for extended periods may affect device reliability

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
LC	12	35
AC	12	36

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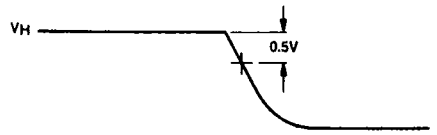
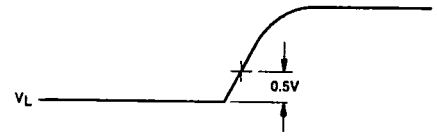
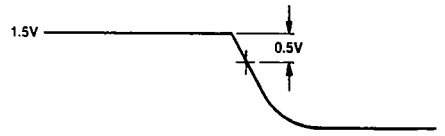
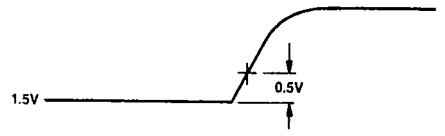
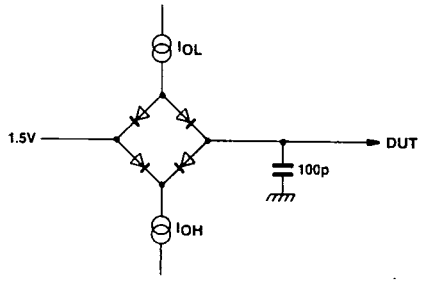
Test	Waveform - measurement level
Delay from output high to output high impedance	
Delay from output low to output high impedance	
Delay from output high impedance to output low	
Delay from output high impedance to output high	

NOTES
1 V_H - Voltage reached when output driven high.
2 V_L - Voltage reached when output driven low.



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ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} (Industrial) = -40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V
T_{amb} (Military) = -55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 3.2mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -3.2mA
Input high voltage	V_{IH}	2.0		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IL}	-10		+10	μA	$GND \le V_{IN} \le V_{CC}$
Output leakage current	I_{OZ}	-50	-	+50	μA	$GND \le V_{OUT} \le V_{CC}$:
Output S/C current	I_{OS}	20	-	200	mA	V_{CC} = Max
Input capacitance	C_{IN}	-	9	-	pF	

Switching Characteristics

Characteristic	Value Industrial				Value Military		Units	Conditions
	PDSP16318		PDSP16318A		PDSP16318			
	Min.	Max.	Min.	Max.	Min.	Max.		
Clock period	100	-	50	-	100	-	ns	
Clock High Time	20	-	15	-	20	-	ns	
Clock Low Time	20	-	15	-	20	-	ns	
A15:0, B15:0 setup to clock rising edge	8	-	5	-	8	-	ns	
A15:0, B15:0 hold after clock rising edge	2	-	2	-	2	-	ns	
MS, S2:0, ASI setup to clock rising edge	10	-	10	-	10	-	ns	
DEL, ASR, $\overline{CLR}$ setup to clock rising edge	8	-	5	-	8	-	ns	
DEL, ASR, $\overline{CLR}$, MS, S2:0, ASI hold after clock rising edge	2	-	2	-	2	-	ns	
$\overline{CEA}$, $\overline{CEB}$ setup to clock falling edge	2	-	2	-	2	-	ns	
$\overline{CEA}$, $\overline{CEB}$ hold after clock rising edge	8	-	8	-	8	-	ns	
Clock rising edge to OVR, C15:0, D15:0	5	40	5	30	5	40	ns	2 x LSTTL + 20pF
$\overline{OEC}$/$\overline{OED}$ low to C15:0/D15:0 high data valid	-	40	-	30	-	40	ns	2 x LSTTL + 20pF
$\overline{OEC}$/$\overline{OED}$ low to C15:0/D15:0 low data valid	-	40	-	30	-	40	ns	2 x LSTTL + 20pF
$\overline{OEC}$/$\overline{OED}$ high to C15:0/D15:0 high impedance	-	40	-	30	-	40	ns	2 x LSTTL + 20pF
Vcc current	-	70	-	110	-	70	mA	Vcc = max, TTL input levels Outputs unloaded, f_{CLK} = max
Vcc current	-	30	-	60	-	30	mA	Vcc = max, CMOS input levels Outputs unloaded, f_{CLK} = max

NOTES
1 LSTTL is equivalent to I_{OH} = 20 microamps, I_{OL} = -0.4mA.
2 Current is defined as positive into the device.
3 CMOS input levels are defined as
V_L = 0.5
V_H = V_{DD} - 0.5

ORDERING INFORMATION

Industrial (-40°C to +85°C)

PDSP16318 B0 AC **PDSP16318 B0 LC**
PDSP16318A B0 AC **PDSP16318A B0 LC**

Military (-55°C to+125°C)

PDSP16318 A0 AC **PDSP16318 A0 LC**

Call for availability on High Reliability parts and MIL 883C screening.

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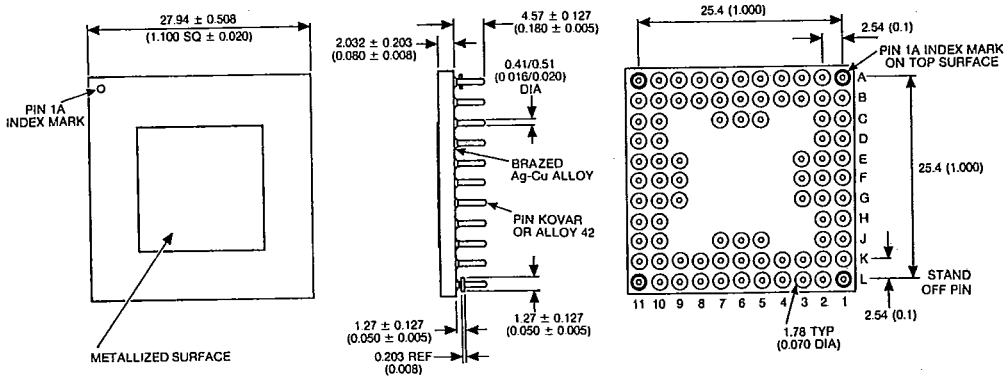
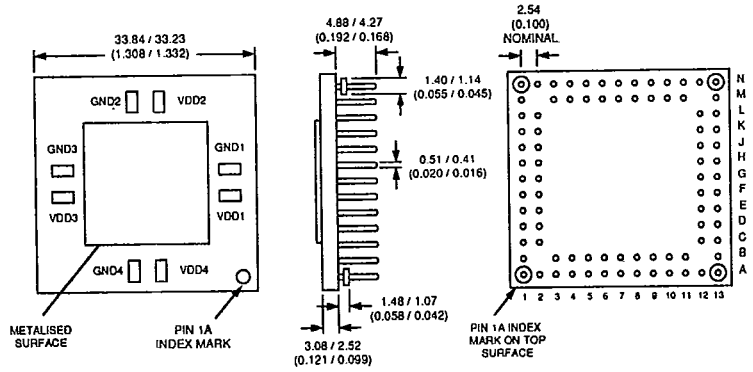
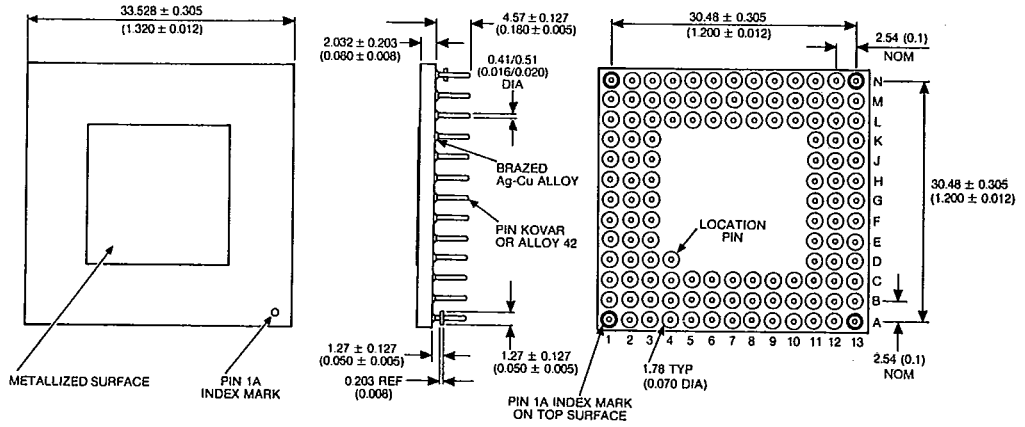


84-PIN GRID ARRAY PACKAGE — AC84

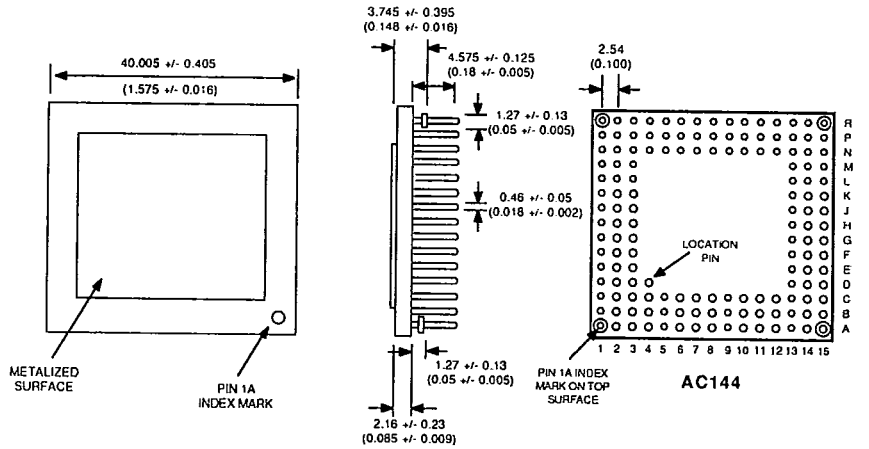


84-PIN GRID ARRAY POWER PACKAGE - AC84

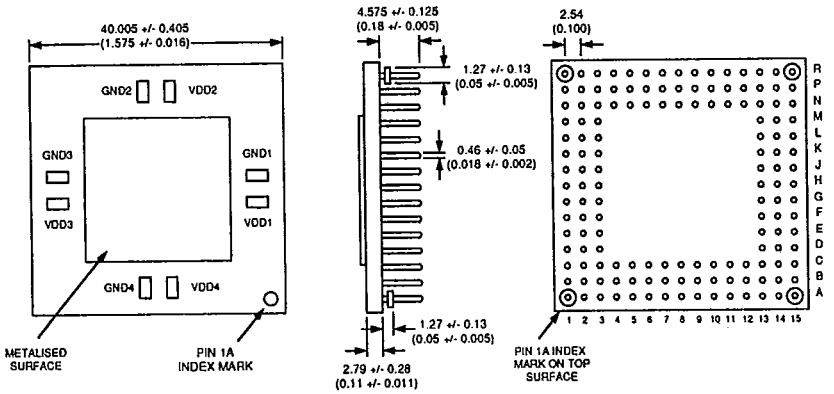
(Used for the PDSP 16340, PDSP16350, PDSP16488 and PDSP16510)



120-PIN GRID ARRAY PACKAGE — AC120

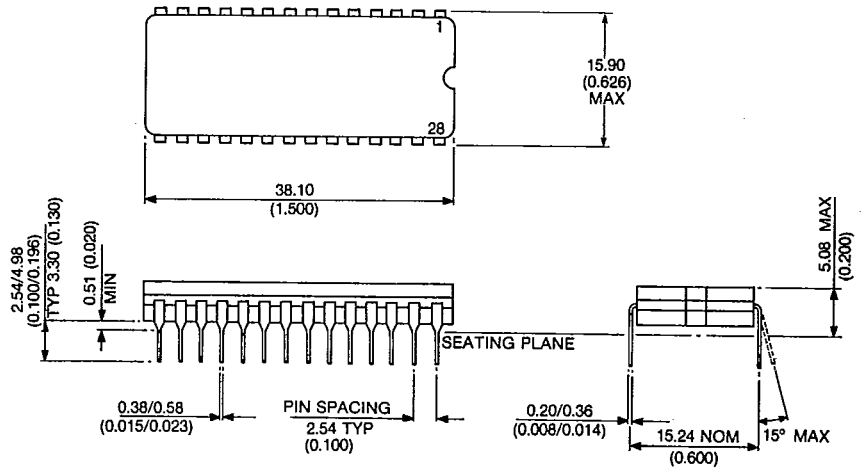


144-PIN GRID ARRAY PACKAGE - AC144

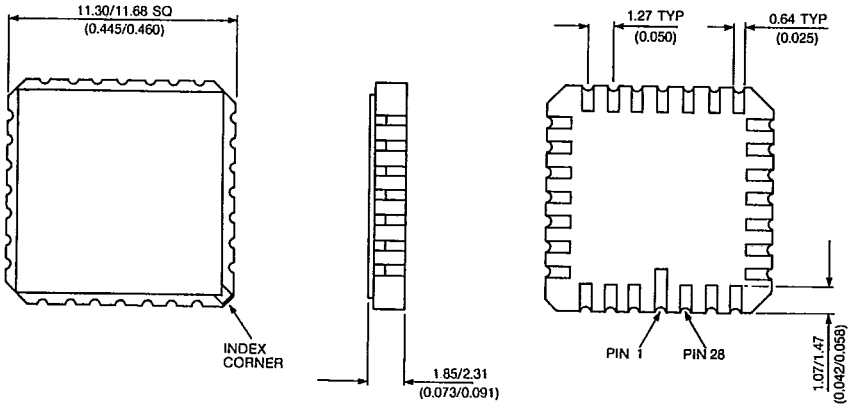


144-PIN GRID ARRAY POWER PACKAGE - AC144

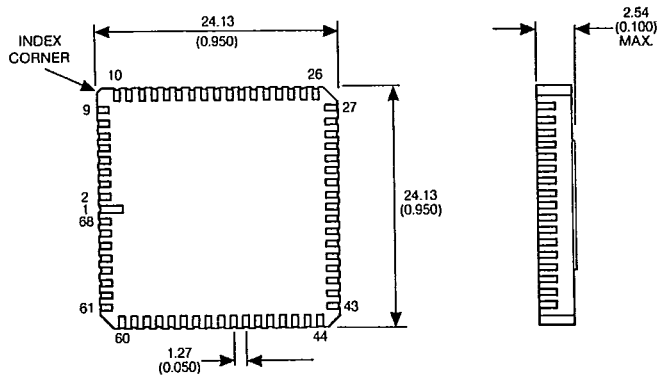
(Used for the PDSP 16256)



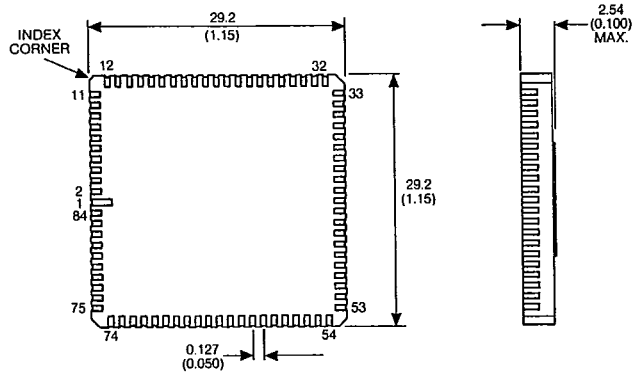
28-LEAD CERAMIC DIL - DG28



28-PIN LEADLESS CHIP CARRIER - LC28
(HERMETIC)



68 CONTACT LCC PACKAGE — LC68



84-PIN LEADLESS CHIP CARRIER - LC84 (HERMETIC)