



Integrated Device Technology, Inc.

256K x 32
BiCMOS/CMOS STATIC RAM
MODULE

IDT7MP4045

T-46-23-14

FEATURES:

- High density 8 megabit static RAM module
- Low profile 64 pin ZIP (Zig-zag In-line vertical Package) or 64 pin SIMM (Single In-line Memory Module)
- Ultra fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

PIN CONFIGURATION⁽¹⁾

PD0	2	1	GND	
I/O0	4	3	PD1	PD0 – GND
I/O1	6	5	I/O8	PD1 – GND
I/O2	8	7	I/O9	
I/O3	10	9	I/O10	
Vcc	12	11	I/O11	
A7	14	15	A0	
A8	16	17	A1	
A9	18	19	A2	
I/O4	20	21	I/O12	
I/O5	22	23	I/O13	
I/O6	24	25	I/O14	
I/O7	26	27	I/O15	
WE	28	29	GND	
A14	30	31	A15	
CS1	32	33	CS2	
CS3	34	35	CS4	
A16	36	37	A17	
GND	38	39	OE	
I/O16	40	41	I/O24	
I/O17	42	43	I/O25	
I/O18	44	45	I/O26	
I/O19	46	47	I/O27	
A10	48	49	A3	
A11	50	51	A4	
A12	52	53	A5	
A13	54	55	Vcc	
I/O20	56	57	A6	
I/O21	58	59	I/O28	
I/O22	60	61	I/O29	
I/O23	62	63	I/O30	
GND	64	63	I/O31	

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NOTE:

1. Pins 2 and 3 (PD0 and PD1) are read by the user to determine the density of the module. If PD0 reads GND and PD1 reads GND, then the module had a 256K depth.

DESCRIPTION:

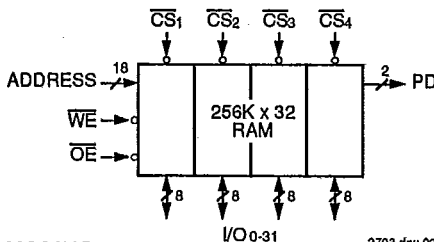
The IDT7MP4045 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. Extremely fast speeds can be achieved due to the use of 1 megabit static RAMs fabricated in IDT's high performance, high reliability BiCMOS™ technology. The IDT7MP4045 is available with access time as fast as 10ns with minimal power consumption.

The IDT7MP4045 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64 pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.35 inches wide. At only 0.60 inches high, this low profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4045 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD0 and PD1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD0 and PD1 to determine a 256K depth.

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

I/O0-31	Data Inputs/Outputs
A0-17	Addresses
CS1-4	Chip Selects
WE	Write Enable
OE	Output Enable
PD0-1	Depth Identification
Vcc	Power
GND	Ground
NC	No Connect

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COMMERCIAL TEMPERATURE RANGE

APRIL 1992

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DSC-7061/3

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data)	V(IN) = 0V	12	pF
CIN(A)	Input Capacitance (Address & Control)	V(IN) = 0V	70	pF
COUT	Output Capacitance	V(OUT) = 0V	12	pF

NOTE: 2703 tbl 02

1. This parameter is guaranteed by design but not tested.

TRUTH TABLE

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Mode	CS	OE	WE	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATAOUT	Active
Write	L	X	L	DATAIN	Active
Read	L	H	H	High-Z	Active

2703 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE: 2703 tbl 03

1. VIL (min) = -1.5V for pulse width less than 10ns.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2703 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2703 tbl 04

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
ILI	Input Leakage (Address and Control)	Vcc = Max.; VIN = GND to Vcc	—	80	µA
ILI	Input Leakage (Data)	Vcc = Max.; VIN = GND to Vcc	—	10	µA
ILO	Output Leakage	Vcc = Max.; CS = VIH, VOUT = GND to Vcc	—	10	µA
VOL	Output Low	Vcc = Min., IOL = 8mA	—	0.4	V
VOH	Output High	Vcc = Min., IOH = -4mA	2.4	—	V

2703 tbl 07

Symbol	Parameter	Test Conditions	10ns - 17ns ⁽¹⁾ Max.	20ns - 45ns Max.	Unit
Icc	Dynamic Operating Current	f = fMAX; CS = VIL Vcc = Max.; Output Open	1600	1200	mA
Isb	Standby Supply Current	CS ≥ VIH, Vcc = Max. Outputs Open, f = fMAX	480	480	mA
Isb1	Full Standby Supply Current	CS ≥ Vcc - 0.2V; f = 0 VIN > Vcc - 0.2V or < 0.2V	320	80	mA

NOTE:

1. Preliminary specifications only.

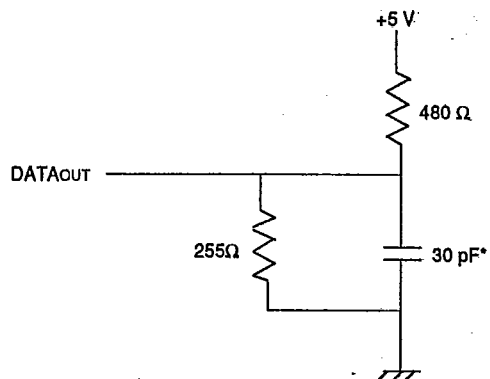
2703 tbl 08

AC TEST CONDITIONS

T-46-23-14

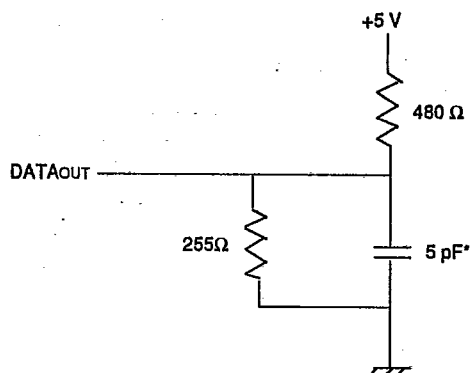
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2703 tbi 09



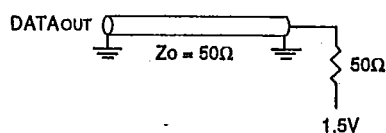
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*Includes scope and jig.
Figure 1. Output Load



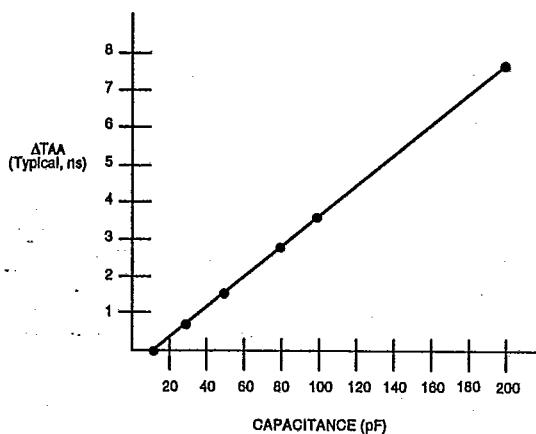
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Figure 2. Output Load
(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)



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Figure 3. Alternate Output Load



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Figure 4. Alternate Lumped Capacitive Load,
Typical Derating

AC ELECTRICAL CHARACTERISTICS

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(VCC = 5V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	7MP4045SxxZ, 7MP4045SxxM								Unit
		-10 ⁽²⁾		-12 ⁽²⁾		-15 ⁽²⁾		-17 ⁽²⁾		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	17	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	17	ns
tACS	Chip Select Access Time	—	7	—	8	—	10	—	12	ns
tOLZ ⁽¹⁾	Chip Select to Output in Low Z	2	—	2	—	2	—	2	—	ns
tOE	Output Enable to Output Valid	—	5	—	5	—	6	—	8	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low Z	2	—	2	—	2	—	2	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	10	ns
tOHZ ⁽¹⁾	Output Disable to Output in High Z	—	3	—	4	—	5	—	6	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	17	—	ns
tCW	Chip Select to End of Write	8	—	8	—	9	—	10	—	ns
tAW	Address Valid to End of Write	8	—	9	—	10	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	9	—	10	—	12	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High Z	—	5	—	5	—	6	—	7	ns
tDW	Data to Write Time Overlap	5	—	5	—	6	—	8	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	2	—	2	—	2	—	2	—	ns

NOTES:

1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

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AC ELECTRICAL CHARACTERISTICS

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(VCC = 5V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	7MP4045SxxZ, 7MP4045SxxM										Unit
		-20		-25		-30		-35		-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	12	—	15	—	18	—	23	ns
tCLZ ⁽¹⁾	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High Z	—	10	—	12	—	15	—	18	—	20	ns
tOHZ ⁽¹⁾	Output Disable to Output in High Z	—	10	—	10	—	10	—	10	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	5	—	5	—	ns
tPU ⁽¹⁾	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power-Down Time	—	20	—	25	—	30	—	35	—	45	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Select to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High Z	—	13	—	15	—	18	—	20	—	23	ns
tDW	Data to Write Time Overlap	12	—	15	—	17	—	20	—	25	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

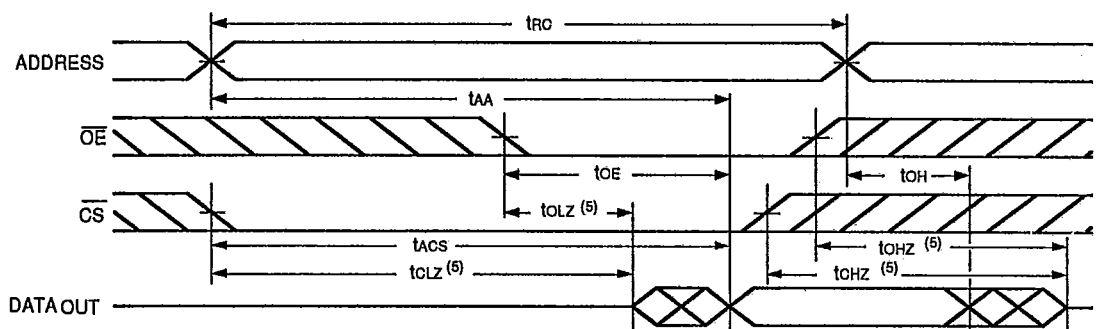
NOTES:

1. This parameter is guaranteed by design, but not tested.

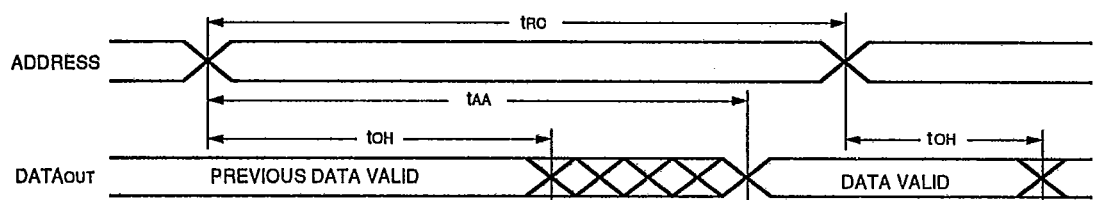
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TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾

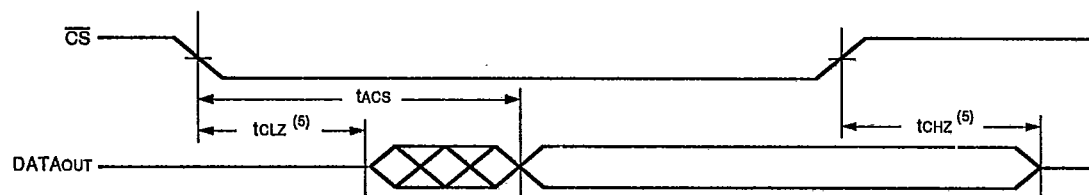
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TIMING WAVEFORM OF READ CYCLE NO. 2^(1,2,4)

2703 drw 08

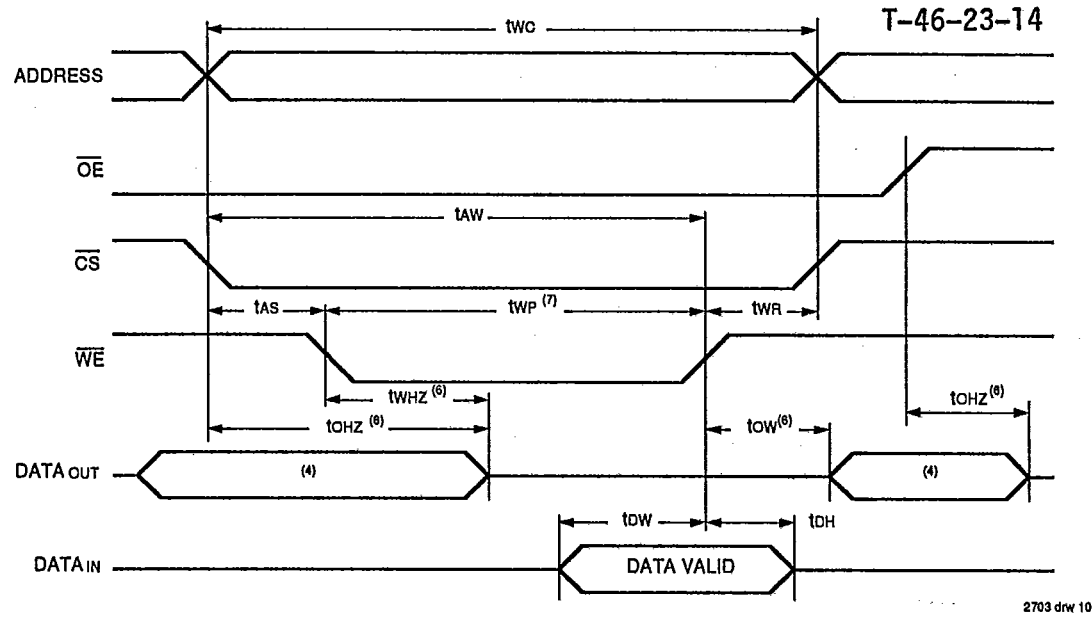
TIMING WAVEFORM OF READ CYCLE NO. 3^(1,3,4)

2703 drw 06

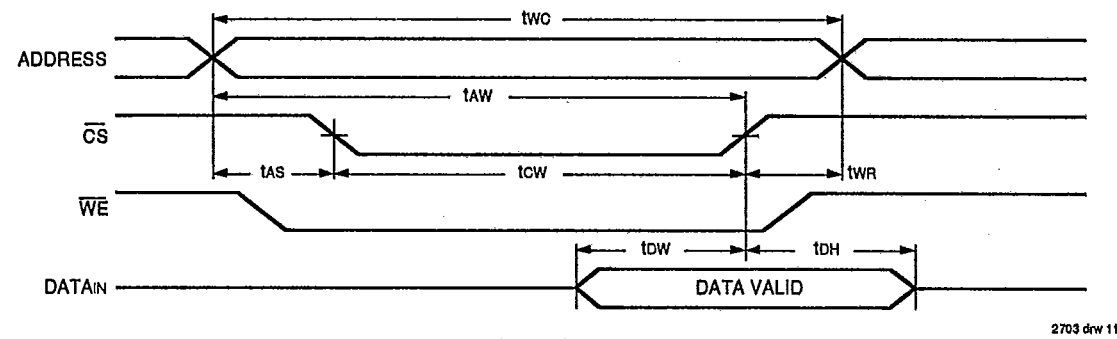
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 200mV$ from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (1, 2, 3, 5)



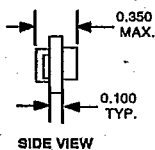
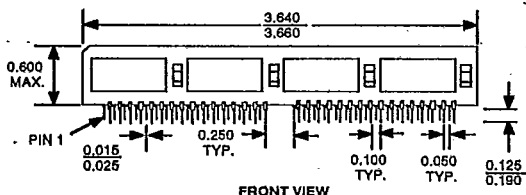
NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{OW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

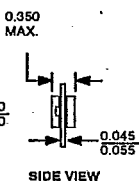
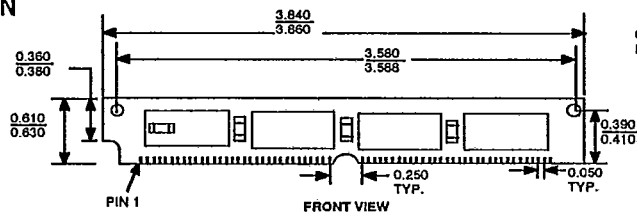
PACKAGE DIMENSIONS

T-46-23-14

ZIP VERSION



SIMM VERSION



2703 drw 12

2703 drw 13