Integrated Device Technology, Inc.

3.3V CMOS ADDRESS/ CLOCK DRIVER

IDT54/74FCT163344/A/C
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

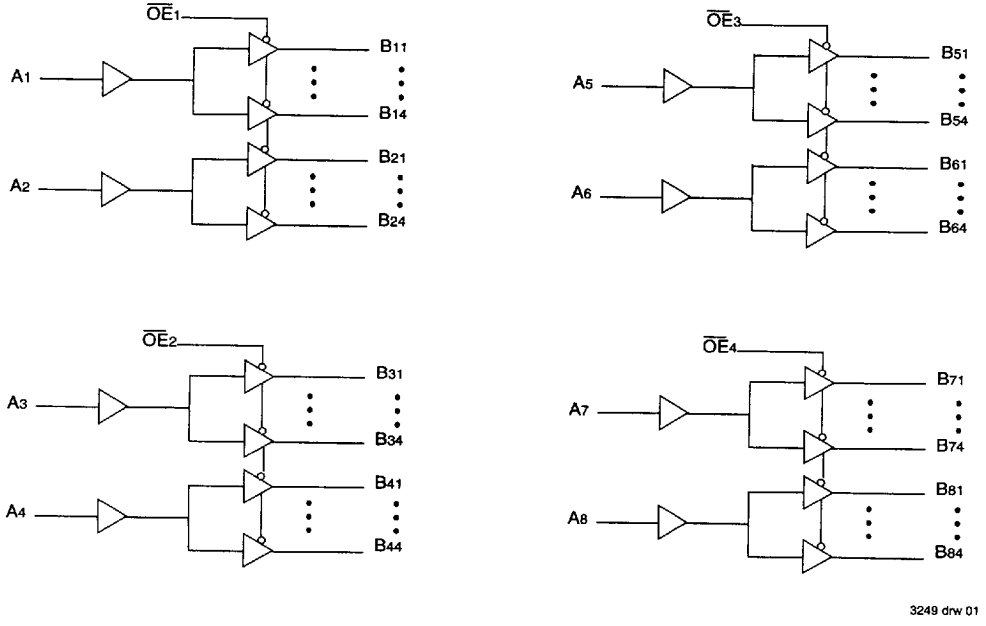
The FCT163344/A/C is a 1:4 address line driver built using advanced dual metal CMOS technology. This high-speed, low power device provides the ability to fanout to memory arrays. Eight banks, each with a fanout of 4, and 3-state control provide efficient address distribution. One or more banks may be used for clock distribution.

The FCT163344/A/C have series current limiting resistors. These offer low ground bounce, minimal undershoot and controlled output fall times, reducing the need for external series terminating resistors.

A large number of power and ground pins ensure reduced noise levels. All inputs are designed with hysteresis for improved noise margins.

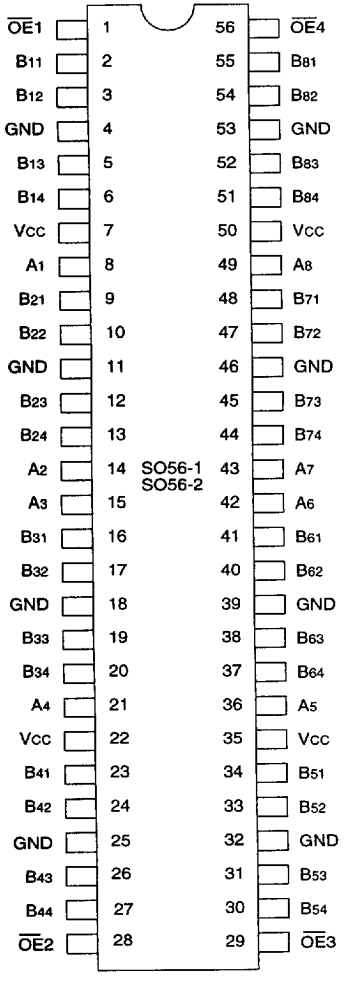
The inputs of the FCT163344/A/C can be driven from either 3.3V or 5V device. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM



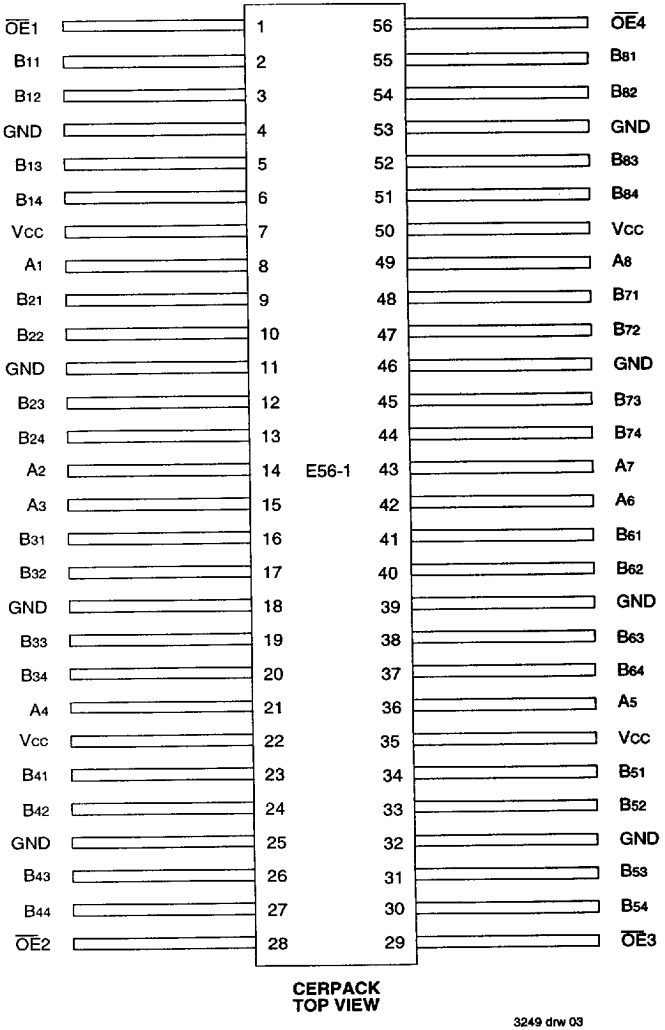
3249 drw 01

PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

3249 drw 02



CERPACK
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
$\overline{OE}x$	3–State Output Enable Inputs (Active LOW)
Ax	Inputs
Bxx	3-State Outputs

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Output and I/O terminals.

FUNCTION TABLE(1)

Inputs		Outputs
$\overline{OE}x$	Ax	Bxx
L	L	L
L	H	H
H	X	Z

3249 tbl 02

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	Vcc+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = Vcc	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = Vcc	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	Vcc–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	—	—	0.2	V
			I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or Vcc	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = Vcc –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} -0.6V[3]		—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_x$ = GND One Input Bit Toggling Four Output Bits Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—			µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE}_x$ = GND One Input Bit Toggling Four Output Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—			mA
			V_{IN} = V_{CC} -0.6V V_{IN} = GND	—			
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}_x$ = GND Eight Input Bits Toggling Thirty Two Output Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—			
			V_{IN} = V_{CC} -0.6V V_{IN} = GND	—			

3249 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[5]

Symbol	Parameter	Condition[1]	FCT163344				FCT163344A				FCT163344C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Ax to Bxx	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.6	ns
tPZH tPZL	Output Enable Time $\overline{OE}$x to Bx		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$x to Bx		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns
tSK1(o)	Skew between outputs of same bank and same package (same transition)[3,4]		—	0.75	—	0.75	—	0.5	—	0.5	—	0.35	—	0.35	ns
tSK2(o)	Skew between outputs of all banks of same package (A1 thru A8 tied together)[3,4]		—	1.0	—	1.0	—	0.5	—	0.5	—	0.5	—	0.5	ns

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NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.
5. Propagation Delays and Enable/Disable times are with VCC = 3.3V ±0.3V, Normal Range. For VCC = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

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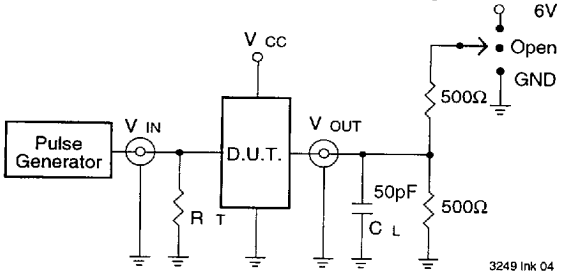
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

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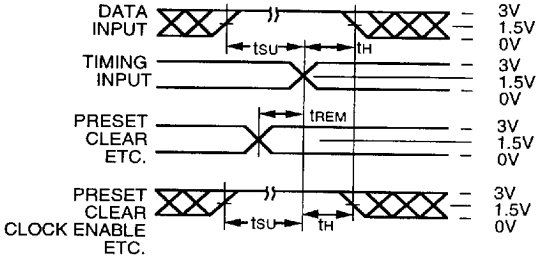
SET-UP, HOLD AND RELEASE TIMES



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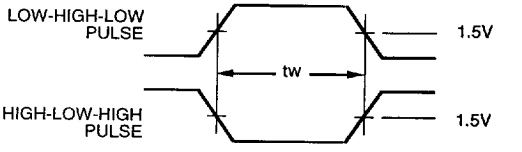
PULSE WIDTH



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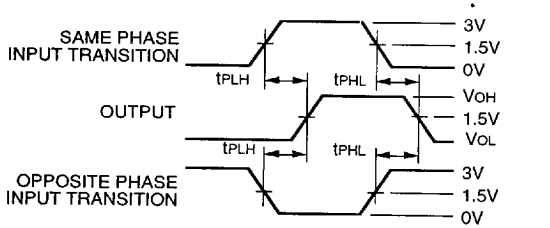
PROPAGATION DELAY



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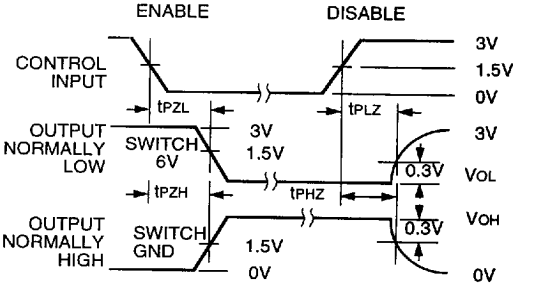
ENABLE AND DISABLE TIMES



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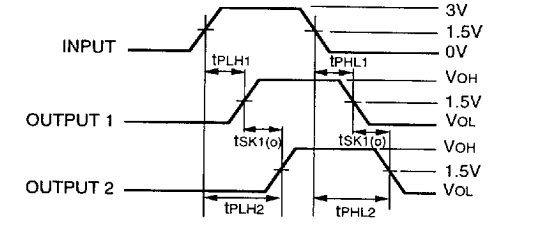
NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns.
3. If Vcc is below 3V, input voltage swings should be adjusted not to exceed Vcc.

OUTPUT SKEW - tSKn(o)



$t_{SKn(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PLH1}|$

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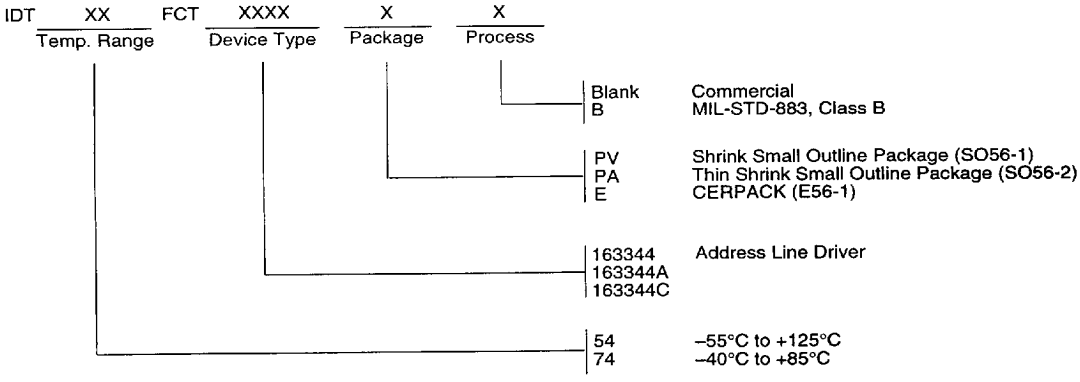
NOTE:
1. For $t_{SK1}(o)$ OUTPUT1 and OUTPUT 2 are in the same bank. For $t_{SK2}(o)$ OUTPUT1 and OUTPUT 2 are in different banks on the same part.

ORDERING INFORMATION



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